Voltage-variable attenuator MMIC using phase cancellation

C.E. Saavedra and B.R. Jackson

Abstract: A new microwave voltage-variable attenuator integrated circuit operating from 1.0 GHz to 3.5 GHz with a large attenuation range is demonstrated in this work. The input signal enters an active balun circuit, which generates an in-phase (0°) signal and an out-of-phase (180°) signal of equal amplitudes. The signals then pass through a pair of source-follower buffer circuits and then through two common-gate (CG) NMOS devices. The drains of the two CG circuits are connected together at the load. While one CG transistor is kept fully on, the gate bias of the second CG device is varied and the amplitude of the signal passing through it changes. Therefore, when the two signals emerging from the CG transistors are added at the output, variable attenuation occurs. The circuit exhibits a measured attenuation range of approximately 30 dB. The 1 dB compression point occurs at an input power of −13 dBm when the attenuation is set to 12 dB. The second harmonic is suppressed by at least 20 dB up to the 1 dB compression point and the measured IIP3 is 3 dBm. The IC was implemented using 0.18 μm CMOS technology. The circuit measures 575 μm by 275 μm including bonding pads and it consumes 18 mW of DC power.

1 Introduction

Voltage-variable attenuator (VVA) circuits are found in a variety of communications applications that include, for example, gain control in transmitters and receivers, RF source power control, beam forming networks, and vector modulators [1]. There are several ways of implementing VVA circuits in IC form. Most microwave monolithic integrated circuit (MMIC) variable attenuators reported in the literature are derived from one of the three basic lumped-element resistive attenuators: the Π network, the T network, or the bridged-T network. For instance, in [2] a CMOS attenuator was designed using two cascaded Π networks with the transistors operating in the triode region as variable resistors. That circuit had an attenuation range of 28 dB from DC to 900 MHz. Another CMOS-based attenuator using a Π network was recently demonstrated in [3]. The reported attenuation range was 35 dB over a 10 GHz span. In both [2, 3], a complex linearisation loop is required to make the attenuation a linear function of control voltage. An attenuator using GaAs MESFETs is discussed in [4], with attenuation range of 13 dB for frequencies from DC to 8 GHz. A MMIC version of the common reflection-type attenuators found in hybrid circuits was demonstrated in [5], and they obtained a 1 dB to 15 dB attenuation range at 10 GHz. There also exist so-called digital attenuators in which the attenuation occurs in discrete steps by designing several attenuators, and using a switch to select between them, or combinations thereof. The digital attenuators can have a very flat frequency response, but one of their drawbacks is that they can occupy a very large area. In [6], an attenuation range of 15 dB was realised from DC to 12 GHz, and the die size was 1.2 mm by 0.8 mm. Another digital attenuator was reported in [7], and that circuit exhibits an attenuation range of 20.5 dB from 2.5 to 2.66 GHz with a die size of 5 mm by 2.5 mm.

In this paper, a novel voltage-variable attenuator MMIC is presented using 0.18 μm CMOS technology. The VVA exhibits an attenuation range between approximately 3 dB and 30 dB from 1.0 to 3.5 GHz. The IC has a good input reflection coefficient over the entire operating band and it consumes only 18 mW of DC power. The circuit operates by converting an unbalanced signal into a balanced signal using an active balun. After passing through a pair of buffers, the antipodal signals enter two common-gate (CG) NMOS devices whose drains are connected together at the output. By keeping one CG device fully on and varying the gate bias of the other transistor, the amplitude of the 180° signal component changes and variable attenuation is obtained at the output load through phase cancellation.

This paper is organised as follows: Section 2 discusses the principle of operation of the circuit and provides analytic equations to predict the attenuation versus control voltage. Section 3 presents the theoretical and measured results, and Section 4 concludes the work.

2 Voltage-variable attenuator circuit

A simplified block diagram of the proposed VVA is shown in Fig. 1. The incoming microwave signal first enters a transistor-based active balun, a unilateral circuit that converts an unbalanced waveform into a pair of balanced signals with equal amplitudes but opposite phase. The balanced signals then pass through a set of buffers before reaching the NMOS common-gate transistors, M_1 and M_2. The in-phase signal enters device M_1, which is fully turned on by applying a constant voltage of V_{dd} (1.8 V) at the gate. Thus, this transistor represents a small series resistance in the signal path. The 180° signal enters the other

IEE Proceedings online no. 20060018

doi:10.1049/ip-cds:20060018

Paper first received 16th January and in revised form 4th April 2006

The authors are with the Department of Electrical and Computer Engineering, 410 Walter Light Hall, Queen's University, Kingston, Ontario, Canada K7L 3N6

E-mail: carlos.saavedra@queensu.ca

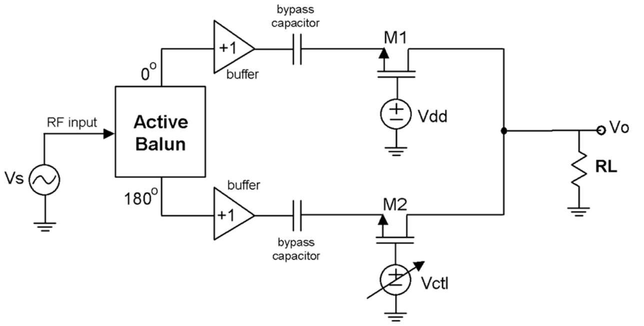

Fig. 1 *Voltage-variable attenuator concept*

common-gate NMOS device, M_2, but the gate voltage (V_{ctl}) in this case is variable. Transistor M_2 can be viewed as a voltage-variable series resistance because the transistor is in the triode region, and thus the signal passing through the device will change in amplitude as V_{ctl} changes. When the two out-of-phase drain currents of M_1 and M_2 are added together at the load resistor, R_L, a cancellation (i.e. attenuation) occurs at the load. By changing the gate voltage of M_2, the amplitude of the signal through that transistor will change and this results in variable attenuation. Minimum attenuation occurs when M_2 is fully turned off ($V_{ctl} = 0\,\mathrm{V}$) and, conversely, maximum attenuation happens when M_2 is fully on ($V_{ctl} = V_{dd}$). Owing to parasitic reactances in the device, there is a non-zero phase shift as the signal passes through transistor M_2 when it is fully turned on. This phase shift reduces the maximum possible attenuation because the signal cancellation is not complete. This explains the need for transistor M_1: by having an identical transistor in the other path fully turned on, there will be an identical phase shift in M_1 as there is in M_2, and this significantly improves the attenuation range of the circuit. This attenuator integrated circuit is a much more compact version of the hybrid VVA presented in [8] and it has a much broader bandwidth owing to the use of active baluns as opposed to passive ring hybrids and power combiners, which exhibit a resonant behaviour.

An analytic expression can be derived for the attenuation against control voltage, V_{ctl}, by using the simplified circuit model in Fig. 2. Since the active balun and the buffer circuits generate two signals with equal amplitude but opposite phase, this can be represented as two signal sources, V_s and $-V_s$. The bypass capacitors are not assumed to be infinite and instead have a finite value of C. The resistance R_{ds1} is the resistance in the channel of transistor M_1, which is in the triode region and it is given by

$$R_{ds1} = \left(\frac{\partial i_D}{\partial V_{DS}} \bigg|_{V_{DS}=0} \right)^{-1} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{tn})} \tag{1}$$

where V_{GS} is the gate-to-source voltage, and for this transistor it is equal to $V_{dd} = 1.8\,\mathrm{V}$. Similarly for transistor M_2, which is also operating in triode, the drain-to-source resistance can be written as

$$R_{ds2} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{ctl} - V_{tn})} \tag{2}$$

This is a variable resistance, which is controlled by the voltage V_{ctl}. In (1) and (2), $\mu_n C_{ox}$ is $3.95 \times 10^{-4}\,\mathrm{A/V^2}$, V_{tn} is 0.475 V, and the values of W and L are 25 μm and 0.18 μm

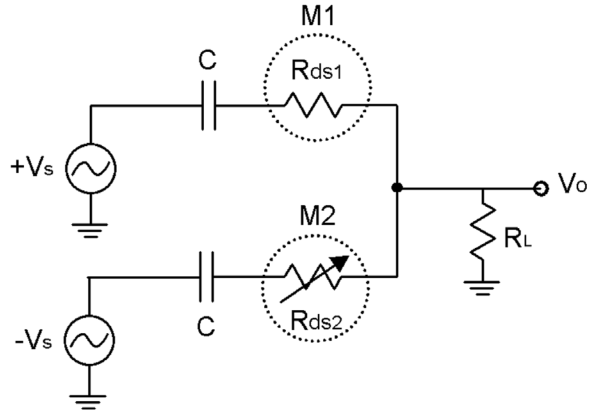

Fig. 2 *Attenuator circuit model*

respectively. Using the circuit in Fig. 2 to determine the output voltage, V_o, as a function of the input voltages, V_s and $-V_s$, we find

$$\frac{V_o}{V_s} = \frac{R_L \| (R_{ds2} + 1/sC)}{(R_L \| (R_{ds2} + 1/sC)) + R_{ds1} + 1/sC} - \frac{R_L \| (R_{ds1} + 1/sC)}{(R_L \| (R_{ds1} + 1/sC)) + R_{ds2} + 1/sC} \tag{3}$$

where $R_L = 50\,\Omega$ and $C = 2\,\mathrm{pF}$. The attenuation in dB is given by

$$\alpha = 20 \log_{10} \left| \frac{V_o}{V_s} \right| \tag{4}$$

Many active balun circuits have been reported and are employed in a variety of applications. The most straightforward active balun uses a single FET with resistors in the source and drain and the input applied to the gate [9]. The resulting signal at the drain will have a 180° phase shift relative to the signal at the source, and with an appropriate selection of resistance values the output amplitudes can be equal. Other common active balun circuits include the differential pair [10], and the common-source/common-gate pair [11]. Ideally the two outputs of a balun circuit should be exactly 180° out of phase and have equal amplitudes. However, at high frequencies, the intrinsic parasitics in the active devices degrade amplitude and phase balance. Furthermore, achieving an acceptable impedance match without off-chip components or physically large integrated inductors can be challenging.

A schematic of the active balun used in this work is shown in Fig. 3. It consists of a common-gate/common-source combination similar to the balun used in [11]. However, impedance matching in [11] is achieved by using

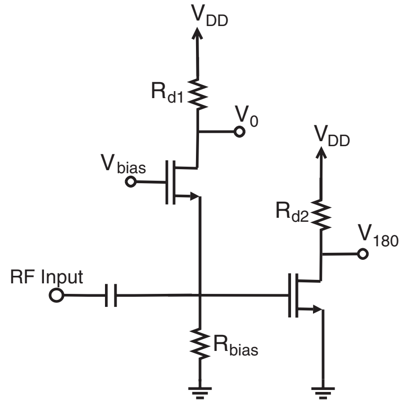

Fig. 3 *Active balun circuit*

spiral inductors and microstrip transmission lines, whereas in the current implementation no such matching network is required, thus saving substantial chip area. The input impedance of the balun is predominantly determined by the input impedance of the common-gate amplifier. Since the input resistance to this circuit is $1/g_m$, an appropriate selection of device size and bias current can yield an acceptably low reflection coefficient. Resistor R_{bias} is large enough not to cause significant attenuation to the signal or to greatly affect the input impedance. The signal is split into two components with the common-source device providing the phase-reversal. By matching the gain of the common-gate and common-source amplifiers, the two outputs, V_0 and V_{180}, have equal amplitudes and are 180° out of phase.

A post-layout simulation of the balun was performed using Cadence Spectre and the phase and amplitude balance of the circuit are shown in Fig. 4*a*. The phase difference between the two outputs (V_0 and V_{180}) is within 1 degree of the ideal (180°) from 1.0 GHz to 3.5 GHz and the amplitude difference is less than 0.1 dB. The insertion loss through the balun is about 1 dB over most the band of interest and the reflection coefficient is below −9 dB, as seen in Fig. 4*b*.

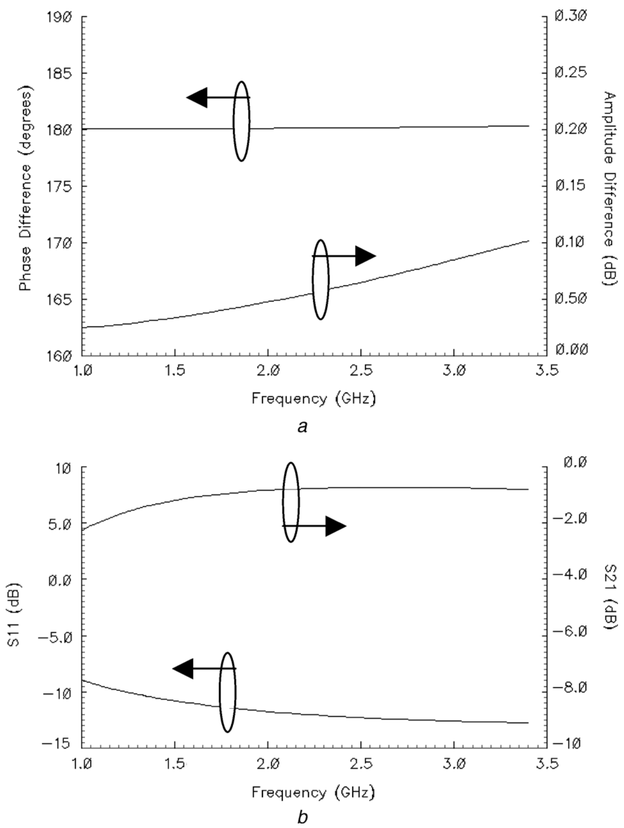

Fig. 4 *Extracted layout simulations of the active balun circuit*
a Phase and magnitude balance
b Reflection coefficient and insertion loss through the balun

A circuit diagram of the attenuator circuit is shown in Fig. 5 (bias networks not shown). A pair of source-follower circuits are used between the active balun and the CG transistors, M_1 and M_2. In the ON state, the CG circuits have a very small input impedance looking into the source, while in the OFF state the impedance is very large. This wide variation input impedance adversely affects amplitude balance of the balun circuit because the drain impedances of M_5 and M_6 would change significantly as a function of V_{ctl} if the two stages were connected directly. Thus the need for

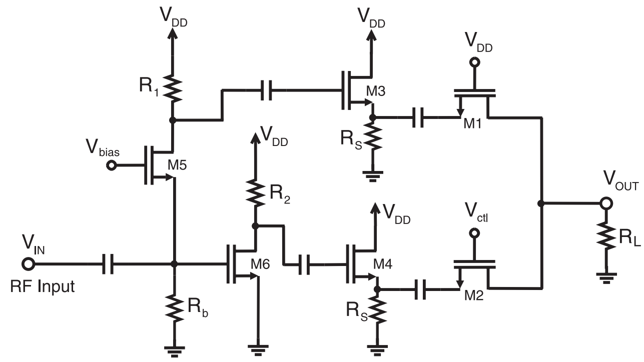

Fig. 5 *CMOS variable attenuator circuit*

the source followers. Since the followers have a gain less than unity, this is a contributing factor to the minimum non-zero loss observed in the attenuator, as will be discussed in the next Section.

3 Experimental results

The measured attenuation against control voltage is shown in Fig. 6 at a representative frequency of 1.4 GHz. From this graph it is observed that the minimum measured attenuation of 2.6 dB occurs for control voltages less than 0.4 V and the maximum measured attenuation is at a control voltage of 1.3 V. That the circuit exhibits a constant attenuation below $V_{ctl} = 0.4$ V is to be expected, since the threshold voltage of the NMOS devices is about 0.45 V. Below 0.45 V, transistor M_2 is in the OFF state and no signal passes through this device, so there is minimum attenuation at the output. Also shown in this figure is the simulated results in addition to the theoretical result using (3) and (4). The simulation results were obtained using the circuit simulator advanced design system (ADS). There is excellent correspondence between the measured and the simulated results, and also very good agreement between the measured and theoretical results. This indicates that the simplified circuit model shown in Fig. 2, from which the attenuation equation was derived, accurately describes this circuit.

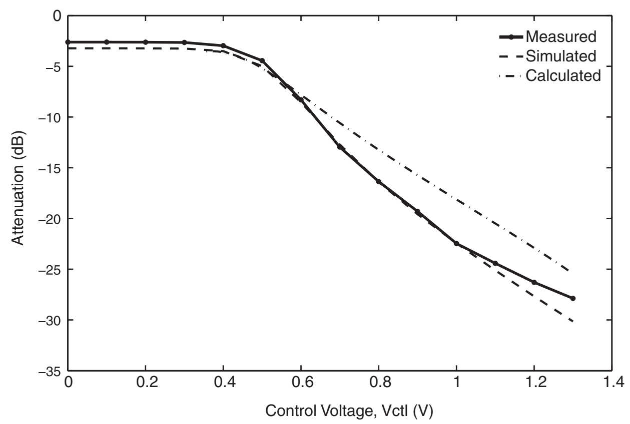

Fig. 6 *Attenuation against control voltage at a fixed frequency of 1.4 GHz*

Figure 7 shows the measured attenuation of the IC against frequency from 1.0 to 3.5 GHz and also as a function of the applied control voltage, V_{ctl}. The minimum attenuation is approximately 2.6 dB while the maximum attenuation is close to 30 dB for most of the band. The attenuator can reach even higher attenuation values, such as −38 dB at 3.5 GHz, but not over the entire band. This is

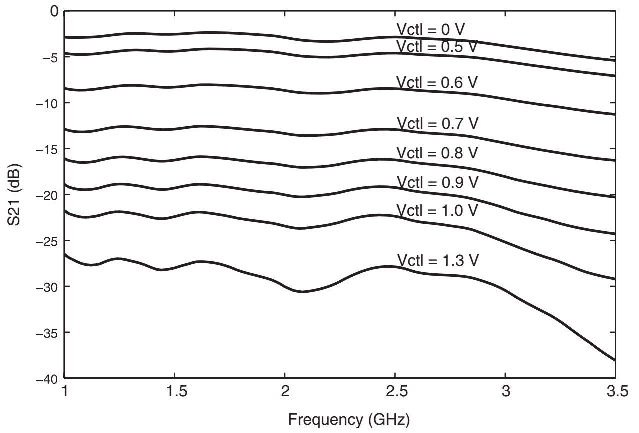

Fig. 7 *Attenuation from 1.0 to 3.5 GHz at various control voltages (V_{ctl})*

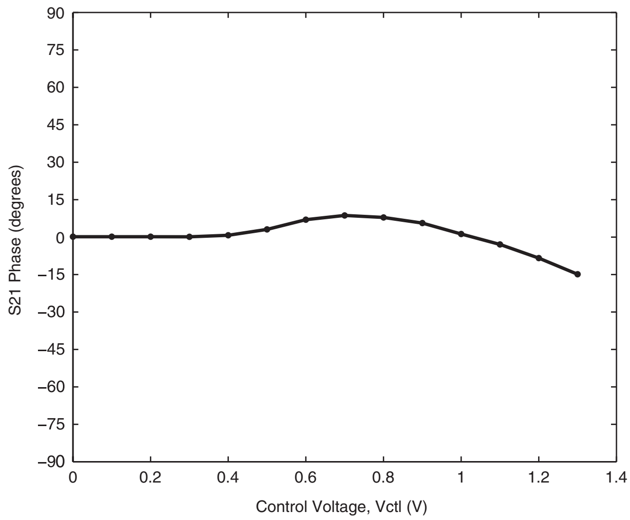

Fig. 8 *S21 phase response at different attenuation levels*

because the phase balance of the signal paths through the CG transistors is exact only over part of the band owing to the bias dependency of some of the parasitic components in the transistors.

Figure 8 shows the phase of the transmission coefficient through the circuit, S_{21}, as the control voltage is varied (which changes the attenuation level). There is less than a 15° variation in phase over the entire attenuation range indicating that the phase is not strongly dependent on attenuation level. The output power performance and harmonic distortion of the VVA is shown in Fig. 9 at an input frequency of 1.4 GHz and an attenuation level of 12 dB. The input 1-dB compression point occurs at $P_{in} = -13$ dBm, which is primarily determined by the active balun circuit. Below the 1 dB compression point, the second harmonic at 2.8 GHz is suppressed by at least 20 dB at the output compared to the fundamental signal. To determine the third-order intercept point, a two-tone pair of input signals at 1.4 GHz and 1.402 GHz were used, and the power levels at the resulting third-order intermodulation products of 1.398 GHz and 1.404 GHz were observed as input power was increased. The measurement and simulation results at a constant attenuation level of 12 dB are shown in Fig. 10 and indicate a measured IIP3 of 3 dBm. Again, there is very good agreement between simulated and experimental results.

The input reflection coefficient is shown in Fig. 11 versus frequency at different control voltages. The input match is

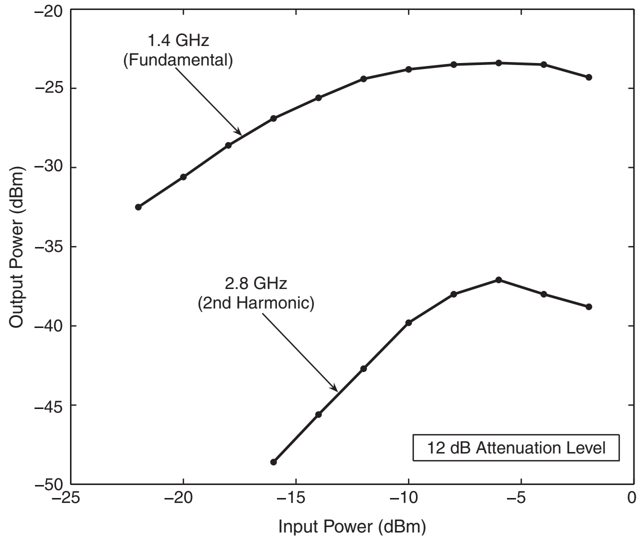

Fig. 9 *Output power performance and harmonic distortion*

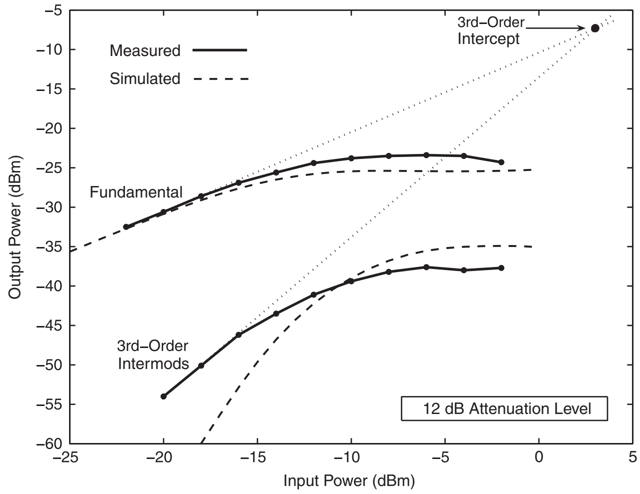

Fig. 10 *Third-order intercept point determination*

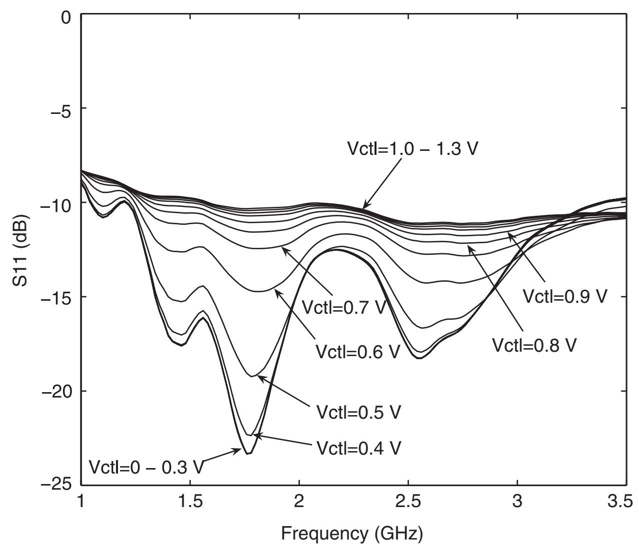

Fig. 11 *Attenuator input impedance match at various control voltages (V_{ctl})*

better than about -10 dB over the band of interest and at all attenuation levels, although somewhat improved input matching can be obtained at lower control voltages. This low return loss is attributed to the fact that we are using an

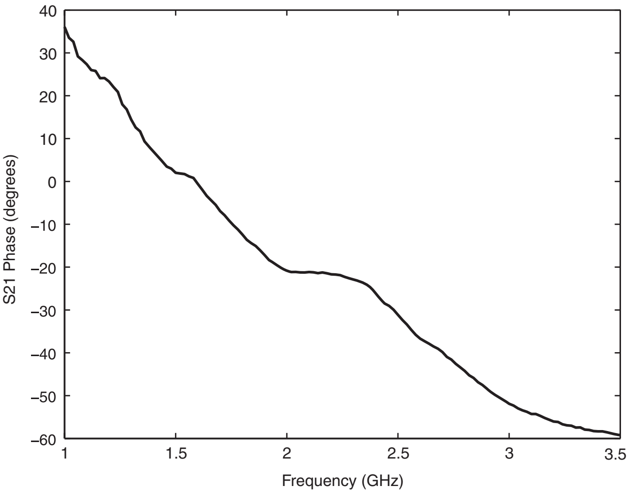

Fig. 12 *S21 phase response at 10 dB attenuation*

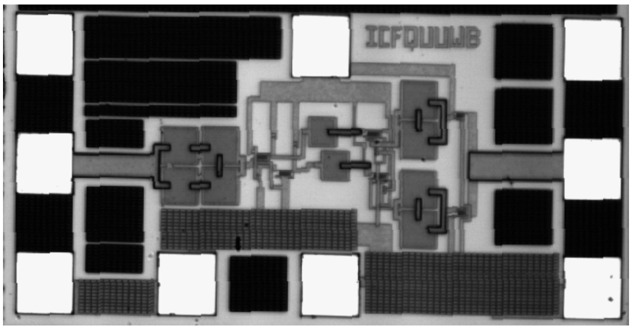

Fig. 13 *Attenuator microphotograph*

active balun as opposed to a passive structure. The presence of the active balun and source-followers isolate the input from the large variations in impedance occurring at the CG transistor, M_2, which could have a significant impact on input match if a passive balun were used. Further improvements on the return loss can be achieved by adding a lumped-element matching network at the VVA input. The phase response of the VVA is displayed in Fig. 12, taken at an attenuation value of 10 dB. The insertion phase is well-behaved over frequency with an approximately linear response.

A microphotograph of the VVA chip is shown in Fig. 13. The IC occupies an area of approximately $0.05\,mm^2$ and the overall chip dimensions are $575\,\mu m \times 275\,\mu m$ including bonding pads. The power consumption is reasonably low at 18 mW from a 1.8 V power supply.

4 Conclusion

A novel CMOS variable attenuator has been proposed, designed, simulated, and experimentally tested. An analytic model was developed to predict the attenuation range of the attenuator against control voltage, and the agreement with experiment is very good. To facilitate the proposed attenuator's need for balanced signals, an active balun was employed as opposed to a passive balun, which greatly reduces the area of the IC. The trade-off of using an active balun is that the input power level has to be decreased to prevent the generation large intermodulation products.

5 References

1 Ashtiani, A.E., Nam, S., d'Espona, A., Lucyszyn, S., and Robertson, I.D.: 'Direct multilevel carrier modulation using millimeter-wave balanced vector modulators', *IEEE Trans. Microw. Theory Tech.*, 1998, **46**, (12), pp. 2611–2619

2 Kaunisto, R., Korpi, P., Kiraly, J., and Halonen, K.: 'A linear-control wide-band CMOS attenuator'. IEEE Int. Symp. on Circuits and Systems, Sydney, Australia, May 2001, pp. 458–461

3 Dogan, H., Meyer, R.G., and Niknejad, A.M.: 'A DC-10 GHz linear in dB attenuator in 0.13 μm CMOS technology'. IEEE Custom Integrated Circuits Conf., Orlando, FL, USA, Oct. 2004, pp. 609–612

4 Maoz, B.: 'A novel, voltage variable MMIC attenuator', *IEEE Trans. Microw. Theory Tech.*, 1990, **38**, (11), pp. 1675–1683

5 Lucyszyn, S., and Robertson, I.D.: 'Analog reflection topology building blocks for adaptive microwave signal processing applications', *IEEE Trans. Microw. Theory Tech.*, 1995, **43**, (3), pp. 601–611

6 McGrath, F.J., and Pratt, R.G.: 'An ultra broadband DC-12 GHz 4 bit GaAs monolithic digital attenuator'. IEEE GaAs IC Symp., Monterey, CA, USA, Oct. 1991, pp. 247–250

7 Takasu, H., Sakakibara, C., Okumura, M., and Kamihashi, S.: 'S-band MMIC attenuator with small phase variation'. IEEE Asia-Pacific Microwave Conf., Singapore, December 1999, pp. 421–424

8 Saavedra, C.E., and Zheng, Y.: 'Ring-hybrid voltage variable attenuator using HFET transistors', *IEEE Trans. Microw. Theory Tech.*, 2005, **53**, (7), pp. 2430–2434

9 Koizumi, H., Nagata, S., Tateoka, K., Kanazawa, K., and Ueda, D.: 'A GaAs single balanced mixer MMIC with built-in active balun for personal communication systems'. IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp., Orlando, FL, USA, May 1995, pp. 77–80

10 Lin, J., Zelley, C., Boric-Lubecke, O., Gould, P., and Yan, R.: 'A silicon MMIC active balun/buffer amplifier with high linearity and low residual phase noise'. IEEE MTT-S Digest, Boston, MA, USA, June 2000, pp. 1289–1292

11 Tsai, M.C., Schindler, M.J., Struble, W., Ventresca, M., Binder, R., Waterman, R., and Danzilio, D.: 'A compact wideband balanced mixer'. IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp., San Diego, CA, USA, May 1994, pp. 135–138