

# A CMOS Ku-Band 4x Subharmonic Mixer

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**Abstract**—In this work, the design and measurement of a new 4x subharmonic mixer circuit is presented using CMOS 0.18  $\mu\text{m}$  technology. With an RF input signal at 12.1 GHz, and an LO signal at 3.0 GHz, an intermediate frequency of 100 MHz is produced ( $f_{\text{IF}} = f_{\text{RF}} - 4f_{\text{LO}}$ ). The mixer uses a modified Gilbert-cell topology with octet-phase LO switching transistors to perform the quadruple subharmonic mixing. Included in the design is an active balun for the RF signal and a circuit that generates an octet-phase LO signals from a differential input. The mixer has a conversion gain of approximately 6 dB, 1-dB compression point of  $-12$  dBm, IIP3 of  $-2$  dBm, and IIP2 of 17 dBm. The circuit also exhibits excellent isolation between its ports (e.g. LO-RF: 71 dB, 4LO-RF: 59 dB).

**Index Terms**—Direct-conversion receivers, frequency multipliers, microwave mixers, MMICs, RF CMOS, subharmonic mixers.

## I. INTRODUCTION

THERE HAS BEEN considerable interest in RF CMOS circuits over the past decade due in part to the desire to realize complete systems-on-a-chip (SoC). There are significant potential advantages to integrating entire systems on a single die, such as reduced cost and increased functionality. One major obstacle in achieving a SoC that has a transceiver integrated on-chip is the intermediate frequency (IF) filters required in typical heterodyne topologies. These filters can be physically large and can eliminate any possibility of integrating the entire system on a single die. An alternative technique that can potentially eliminate the IF filter is through the use of a direct-conversion receiver. With this technique, the RF signal is converted directly to baseband, thus eliminating the IF stage. There are, however, challenges with the direct-conversion technique. Since the RF signal is converted to DC, any DC offsets that are created by the mixer itself can interfere with the desired signal. Given that the LO is generally a strong signal, it can easily couple to various circuits on the chip, which can result in a DC offset from self-mixing. There are several possible paths for LO self-mixing, as shown in Fig. 1(a) [1]. Path 1 represents the LO signal that is coupled to the RF port of the mixer, which will then mix with itself and produce a DC offset. Path 2 represents LO coupling to the input of the LNA, which can be particularly problematic since it will then be amplified along with the RF signal before entering the RF port. Path 3 in Fig. 1(a) represents the LO signal coupling to the antenna where it is radiated and reflections of this signal by nearby objects are received by the

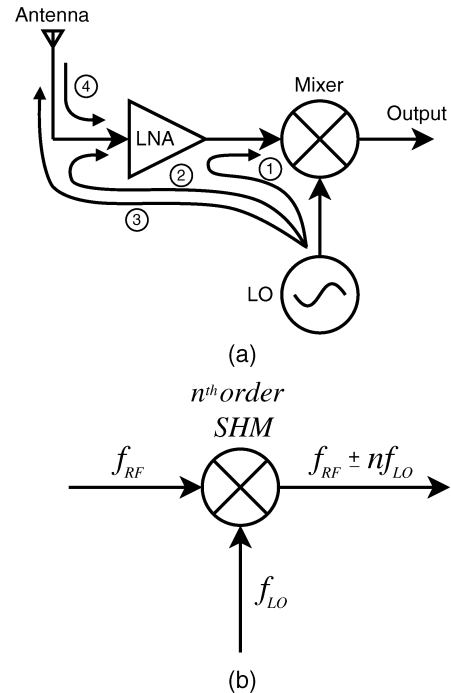


Fig. 1. (a) Potential self-mixing paths. (b) An  $n^{\text{th}}$  order subharmonic mixer.

antenna and are shown in Path 4. Path 4 can also represent a strong nearby interfering signal that is received by the antenna and could couple to the LO port and self-mix, also producing a DC offset. Whereas Paths 1 and 2 would generate static DC offsets, the results of paths 3 and 4 would be dynamic due to the changing operating environment. CMOS technology, in particular, is very susceptible to LO self-mixing due to the relatively low substrate resistivity that easily allows energy to couple to other sub-circuits on the chip. Techniques that have been suggested to alleviate the LO self-mixing problem include the use of a frequency doubler at the output of the LO [2] and the use of a subharmonic mixer (SHM) [3]–[7]. With a subharmonic mixer, the LO frequency is internally multiplied, thus producing mixing components from the RF frequency and a multiple of the LO frequency. If  $f_{\text{RF}}$  is the RF input frequency and  $f_{\text{LO}}$  is the LO input frequency then the output signals will have frequency

$$f_{\text{IF}} = |f_{\text{RF}} \pm nf_{\text{LO}}| \quad (1)$$

where  $n$  is the order of the subharmonic mixer, as shown in Fig. 1(b). The use of a subharmonic mixer with order  $n = 4$ , for example, permits the use an LO with *one-quarter* the frequency that would be required with a fundamental-mode mixer. The reduction in LO frequency can potentially simplify the LO design and improve the phase noise performance. At high-frequencies, in particular, it may be difficult to design an LO with the required output power and phase noise, which also makes the

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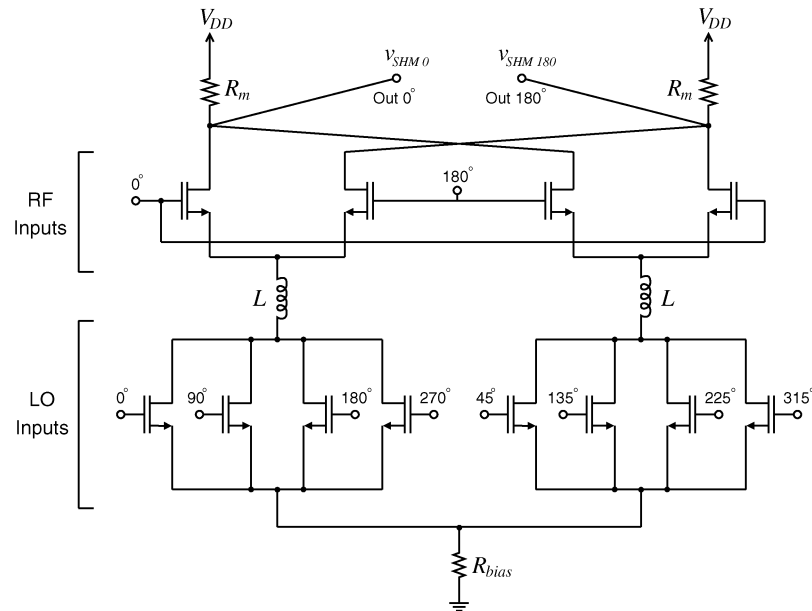


Fig. 2. Mixer core of the proposed 4x SHM.

subharmonic mixing technique attractive for applications other than direct-conversion receivers.

2x SHMs have been proposed in [3], [5], [8]–[22]. In most cases (e.g. [3], [5], [9], [17], [18], [20], [21]), modifications to the Gilbert-cell mixer were made in order to generate the double frequency LO component to mix with the RF. Also very common is the requirement of quadrature LO signals for SHMs ([3], [5], [9]–[11], [14]). Furthermore, in [15]–[18], octet-phase signals of the LO were required to implement the 2x SHM. There have also been several 4x SHMs previously demonstrated [23]–[28]. Of these circuits, the vast majority use diodes in order to perform the mixing, which eliminates the possibility of achieving conversion gain. In [23], GaAs MESFETs are used in addition to several stubs for filtering and a conversion gain of 3.4 dB was achieved. Generally, and as would be expected, 4x SHMs have more loss than 2x SHMs and in most cases do not exhibit a conversion gain.

In this work, a new 4x SHM is presented in CMOS technology. An RF frequency in the Ku-band was used to demonstrate this circuit, which is a very commonly used band for satellite communications. To the best of the authors' knowledge, this is the first 4x subharmonic mixer demonstrated in CMOS technology. Furthermore, it obtains the highest conversion gain for any 4x SHM to date.

Although it would be possible to realize an LO that operates directly at Ku-band in CMOS technology, the resulting fundamental mixer would likely have increased self-mixing and therefore degrade the performance of a direct-conversion receiver compared to a subharmonic mixer. Similarly, while it would be possible to use a separate LO frequency multiplier along with a fundamental or a 2x SHM, the resulting power consumption and required chip area could potentially increase and the port-to-port isolation could suffer, resulting in an increase in self-mixing.

The proposed circuit could easily be moved to higher frequencies (mm-wave) where subharmonic mixing may be a necessity, and in this regard it can be viewed as a lower frequency demonstration circuit.

## II. CIRCUIT DESIGN

### A. Mixer Core

The core of the 4x SHM is based on the Gilbert-cell topology [29]. As shown in Fig. 2, the proposed SHM has the RF and LO ports exchanged compared to a traditional Gilbert-cell. Furthermore, the two transistors typically at the bottom of the Gilbert-cell have been replaced by two sets of four transistors that will generate the fourth harmonic of the LO signal, thus allowing the mixer to operate as a x4 SHM. The inputs to these transistors are octet-phase LO signals, with  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ , and  $270^\circ$  applied to the gates of one set of four FETs and  $45^\circ$ ,  $135^\circ$ ,  $225^\circ$ ,  $315^\circ$  applied to the gates of the other set of FETs. In previous 2x SHM circuits (e.g. [3], [5], [21]) a similar topology is used, but with two pairs of LO transistors instead of four, and they use only quadrature LO signals.

To examine the operation of the mixer, consider one set of four transistors, as shown in Fig. 3(a), with LO signals applied to the gates with relative phase shifts of  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ ,  $270^\circ$ , as shown in Fig. 3(b). The four quadrature LO signals applied to the gates generate a  $4f_{LO}$  signal, as opposed to differential gate signals which only generate a  $2f_{LO}$  signal as in [3], [5], [21]. The quadrature signals applied to the gates of the other set of four transistors are shifted by  $45^\circ$ . This topology generates a  $4f_{LO}$  signal that is  $180^\circ$  out of phase with the other  $4f_{LO}$  signal. Therefore, this mixer topology is double-balanced,

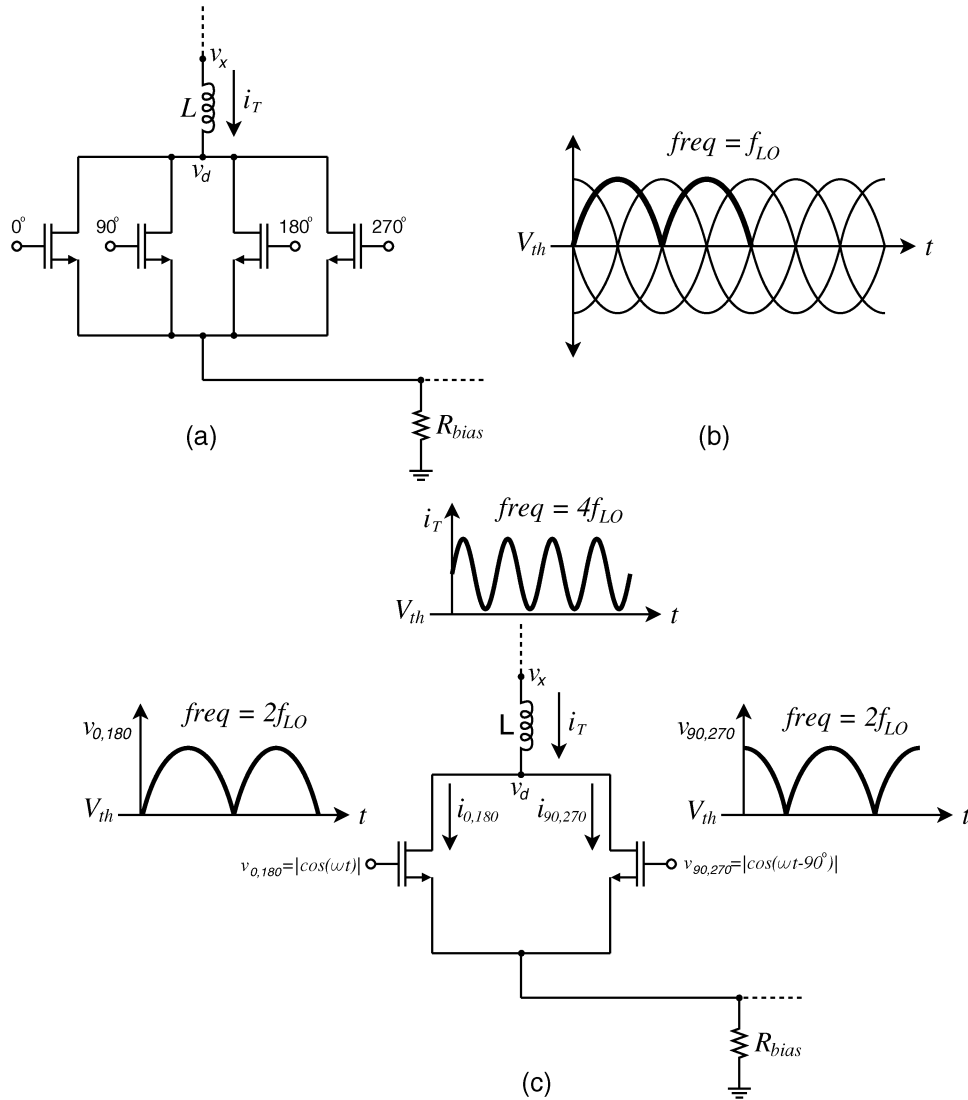


Fig. 3. (a) One of the two 4x LO generation circuits. (b) quadrature LO time-domain signals. (c) Modeling the 4x LO circuit.

which should allow this topology to achieve high-levels of isolation between the ports. If the LO signals have a DC bias at the transistor threshold voltage,  $V_t$ , the signals are given by

$$\begin{aligned} v_{LO0} &= A \cos(\omega t) + V_t \\ v_{LO90} &= A \cos(\omega t - \pi/2) + V_t \\ v_{LO180} &= A \cos(\omega t - \pi) + V_t \\ v_{LO270} &= A \cos(\omega t - 3\pi/2) + V_t \end{aligned}$$

where  $A$  is the amplitude of the LO signal. If it is assumed that the transistors are completely cutoff when the gate voltage is below the threshold voltage (i.e. ignoring sub-threshold current), the  $LO_0$  and  $LO_{180}$  pair of transistors can be modeled by one transistor with LO gate voltage of

$$v_{0,180} = |A \cos(\omega t)| + V_t \quad (2)$$

since only one of the two transistors is on during each half-cycle. Clearly, this waveform contains the double frequency, or

second harmonic. Similarly, the  $LO_{90}$  and  $LO_{270}$  transistors can be replaced by one transistor with LO gate voltage of

$$v_{90,270} = |A \cos(\omega t - \pi/2)| + V_t. \quad (3)$$

This model is shown in Fig. 3(c). Using the short-channel model, the currents generated by the LO voltages are given by

$$i_{0,180} = \frac{WC_{ox} V_{sat} (v_{0,180} - V_t)}{1 + LE_{sat}/(v_{0,180} - V_t)} \quad (4)$$

$$i_{90,270} = \frac{WC_{ox} V_{sat} (v_{90,270} - V_t)}{1 + LE_{sat}/(v_{90,270} - V_t)}. \quad (5)$$

To simplify the analysis and to clearly see the generation of the fourth harmonic, the approximation can be made that  $(v_{gs} - V_t)/L$  is large compared to  $E_{sat}$  such that the denominator  $1 + LE_{sat}/(V_{gs} - V_t) \approx 1$ . A numerical analysis shows that when the amplitude of the gate signal,  $A$ , is large, the results of the simplified equations based on this approximation are very close to the results obtained using (4) and (5). Since the LO signal amplitude will generally be large, it follows that this assumption is reasonable for this circuit. The benefit of using the

simplified drain current formula is that more insight can be obtained from the resulting equations. With this approximation, the drain currents are given by

$$i_{0,180} \approx \frac{1}{2} \mu_n C_{ox} W E_{sat} |A \cos(\omega t)| \quad (6)$$

$$i_{90,270} \approx \frac{1}{2} \mu_n C_{ox} W E_{sat} |A \cos(\omega t - \pi/2)|. \quad (7)$$

The total current,  $i_T$ , is simply given by  $i_T = i_{0,180} + i_{90,270}$ , therefore,

$$i_T \approx \frac{1}{2} \mu_n C_{ox} W E_{sat} A (|\cos(\omega t)| + |\sin(\omega t)|). \quad (8)$$

Since

$$|\cos(\omega t)| + |\sin(\omega t)| = \sqrt{|\sin(2\omega t)| + 1} \quad (9)$$

the following Taylor series expansion can be applied:

$$\sqrt{x+1} = \sum_{n=0}^{\infty} \frac{(-1)^n (2n)!}{(1-2n)(n!)^2 4^n} x^n \quad |x| \leq 1. \quad (10)$$

Therefore,  $i_T$  expanded to three terms is given by

$$i_T \approx \frac{1}{2} \mu_n C_{ox} W E_{sat} A \left( \frac{15}{16} + \frac{1}{2} |\sin(2\omega t)| + \frac{1}{16} \cos(4\omega t) \right). \quad (11)$$

The two terms  $|\sin(2\omega t)|$  and  $\cos(4\omega t)$  both clearly show the fourth harmonic. The total output current signal,  $i_T$ , is dominated by the  $|\sin(2\omega t)|$  term since it is the strongest. Therefore, the frequency of the output current is at four times the input LO frequency, or,  $4f_{LO}$ , as desired. A similar analysis can be performed on the other set of four transistors to show the generation of the fourth harmonic and the anti-phase relationship with (11).

The purpose of the inductors in the mixer core (Figs. 2 and 3(a)) are to increase the LO voltage swing at the source terminal of the RF transistors as discussed in [12], which ultimately provides higher conversion gain for the mixer at lower LO powers than would be required without the enhancement inductors. The voltage at node  $v_x$  shown in Fig. 3(a) is given by

$$v_x = v_d + (R_{ind} + j\omega L)i_T \quad (12)$$

where  $v_d$  is the common drain node of the LO transistors as shown in Fig. 3(a), and  $R_{ind}$  and  $L$  are the series resistance and the inductance of the on-chip spiral inductor, respectively. Since the desired LO frequency is *four times* the LO input frequency, this inductor provides a large impedance, which increases the voltage swing at  $v_x$  and improves the resulting conversion gain. It also provides filtering for any parasitic  $f_{LO}$  and  $2f_{LO}$  signals that are present since the impedance of the inductor is lower for these signals.

### B. Input RF Balun

In many cases, single-ended signals are used as opposed to balanced signals. In order to convert the single-ended RF signal to a balanced signal, an active balun was used in this work. The use of an active balun as opposed to a passive balun enables this circuit to be conveniently implemented on chip since the

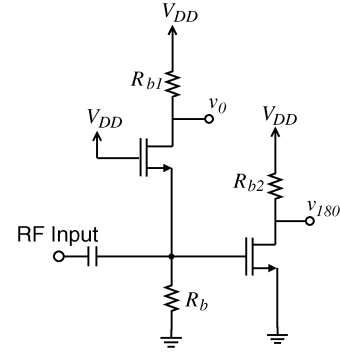


Fig. 4. Common-source common-gate active balun.

required size is vastly reduced. The topology of the active balun used is shown in Fig. 4. The circuit uses a common-source path to produce a  $180^\circ$  phase shift and a common-gate path to produce the  $0^\circ$  signal with equal amplitudes [30]. An advantage to this technique is the ability to achieve a reasonably good input impedance match to  $50 \Omega$  since the input to this balun is approximately that of the common-gate circuit,  $Z_{in} \approx 1/g_m$  (the resistor  $R_b$  is large). Therefore, with appropriate selection of device size and biasing, the input of the balun can produce wide-band matching. While this topology may be somewhat more sensitive to fabrication process variations than a differential pair configuration, the elimination of matching inductors that would likely be required with a differential pair balun saves significant chip area.

Simulation results of the active balun at an input frequency around 12 GHz show that the phase error is approximately  $6^\circ$  and the amplitude imbalance is approximately 0.5 dB. The voltage loss through the balun at 12 GHz when the load is the input to the SHM is  $-3$  dB. Obviously, if a balanced RF signal was already available then the RF balun would not be necessary and the resulting conversion gain would be increased. Since the RF signal is not perfectly balanced, the RF-IF isolation may be degraded somewhat. However, since the RF frequency is in the Ku-band and the IF frequency is quite low, this should not pose a significant problem since it could easily be removed by a simple filter.

### C. LO Phase Shifters

In order to realize the 4x SHM discussed in the previous section, octet-phase LO signals are required. Octet-phase LO signals were also required in the SHMs presented in [15]–[17], [20], however, all of these circuits were only 2x SHMs. RC polyphase filters were used to generate the required phase shifts in [1]. This technique, although the simplest, can generate phase and amplitude errors due to fabrication tolerances in the resistors. Similarly, the  $45^\circ$  phase shifter in [20] was also a passive network consisting of resistors and capacitors. The technique used to generate the octet signals in this work is similar to the technique used in [15]. This method essentially uses an active summer to add a  $0^\circ$  and a  $90^\circ$  signal to realize a  $45^\circ$  signal

$$A \cos(\omega t) + A \cos(\omega t + \pi/2) = \sqrt{2} A \cos(\omega t + \pi/4). \quad (13)$$

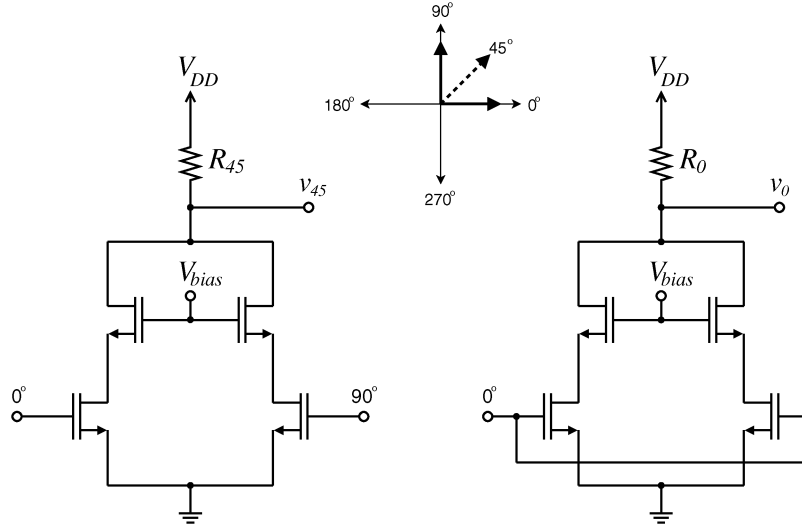


Fig. 5. 45° phase shifter circuit. 0° and 90° signals are added producing a signal at  $v_{45}$  that is 45° out of phase with the output of the in-phase adder,  $v_0$ .

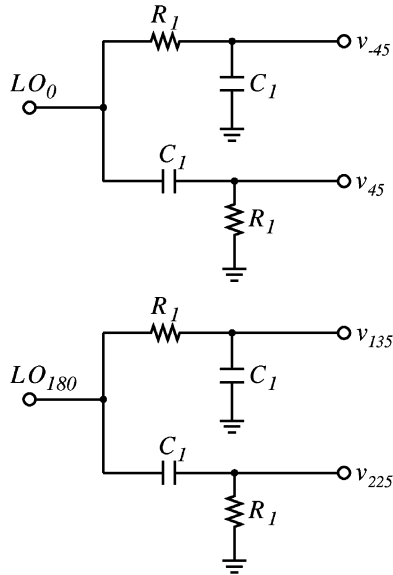


Fig. 6. 90° RC-CR phase shifter.

This 45° phase shift is relative to a similar in-phase (0°) adder circuit that adds two signals with the same phase. The purpose of the in-phase adder is to equalize parasitics in the two paths so that a more accurate 45° phase relationship can be obtained. The circuit schematics of the 45° phase shifter and the in-phase adder are shown in Fig. 5. By the proper scaling of resistors,  $R_{45}$  and  $R_0$ , the amplitudes of the 45° phase shifter and the in-phase adders can be made equal.

Clearly, to use the aforementioned technique, quadrature LO signals must be available. In many cases, this is not a problem since a quadrature oscillator can simply be used. To verify the proposed 4x SHM in this work, a differential LO input signal was used along with a passive RC 90° phase shifter, as shown in Fig. 6.

Simulation results on the complete octet-phase generator circuit show a phase error of approximately 1° and a amplitude

imbalance of less than 1 dB using this technique. The main concern with using this technique is that the tolerance in the various components in the fabrication process can lead to larger phase and amplitude errors than are shown in simulations (particularly in the RC-CR 90° phase shifters) and the resulting mixer performance will be degraded. A detailed analysis of the effects of potential phase and amplitude errors using this technique were presented in [15]. It was found that by following the polyphase filter with the active 45° phase shifting circuit shown in Fig. 5 the resulting octet-phase outputs are actually desensitized to phase errors in the polyphase filters. Furthermore, it was determined that even with significant process variations of the resistance in the RC-CR 90° phase shifters the resulting accuracy of the octet-phase signal was still within acceptable limits [15].

D. Output Balun

In order to convert the differential amplifier output back to single-ended for measurement, another active balun was used. Since the IF output will be at a relatively low frequency (100 MHz, in this case), it makes the use of an active balun very attractive compared to passive techniques, given the large wavelength of the signal. Furthermore, since the frequency is low, it makes the design of this balun very straightforward. The output balun is shown in Fig. 7 which includes a differential pair with the output take single-endedly and connected to a source-follower buffer. The output balun was designed such that the differential voltage amplitude at the mixer output equals the buffer output,  $v_{SHM0} - v_{SHM180} = v_{OUT}$ . Therefore, there was no gain in this stage that would contribute to the conversion gain of the mixer.

III. EXPERIMENTAL RESULTS

To characterize the 4x CMOS SHM, co-planar waveguide (CPW) probes were used for on-chip probing. An Agilent E4446A PSA Series spectrum analyzer was used to observe the output spectrum of the mixer. The DC supply voltage was set to 2.75 V, the RF input signal was -20 dBm at 12.1 GHz, and the LO signal was 10 dBm at 3.0 GHz. Therefore, the

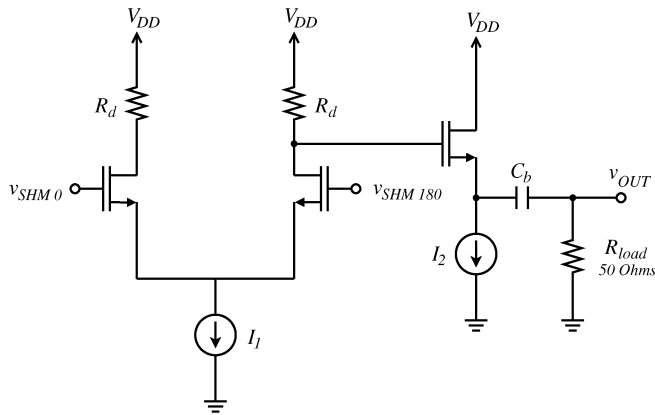
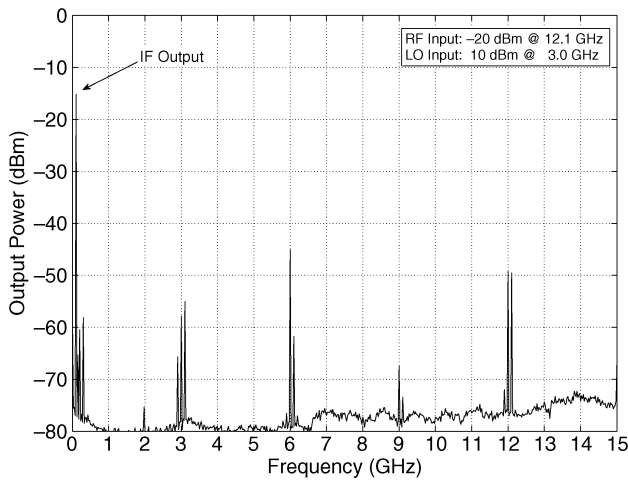


Fig. 7. Output balun circuit.

Fig. 8. Measured mixer output spectrum with  $-20$  dBm RF power and 10 dBm LO power.

desired IF output signal was at 100 MHz ( $f_{RF} - 4f_{LO}$ ). A typical output spectrum is shown in Fig. 8. The conversion gain is approximately 5.8 dB and all other spectral components are below  $-45$  dBm (more than 30 dB below the IF). In order to determine the 1-dB compression point of the mixer, the input power was swept and the IF output power was measured. The measurement and simulation results are shown in Fig. 9. The measured input 1-dB compression point is  $-12$  dBm. The simulation results are very similar to the measured results, however, the measurements show an earlier saturation than in simulation. The 1-dB compression point would be improved somewhat if a differential RF input signal was fed directly to the mixer without going through the balun circuit. Nevertheless, an input  $P_{1dB}$  of  $-12$  dBm is very similar to the subharmonic mixers reported in [10], [11], [14], [15], [22], [27], [28]. A plot of the conversion gain at various LO input power levels is shown in Fig. 10. From this figure, conversion gain is achieved when the LO power is above 8.4 dBm with a maximum conversion gain of approximately 6.5 dB occurring at 11 dBm LO input power. An optimal conversion gain was determined to occur for an LO input power of 10 dBm while still having very strong suppression of undesired spectral components (more than 30 dB below the IF). Note that these conversion gain values were obtained

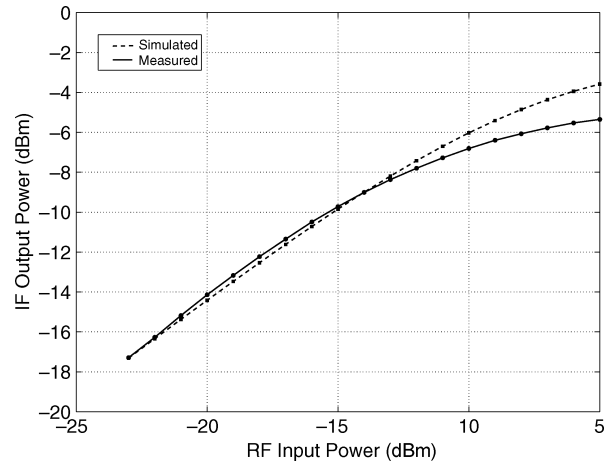


Fig. 9. 1-dB compression point measurement (LO power = 10 dBm).

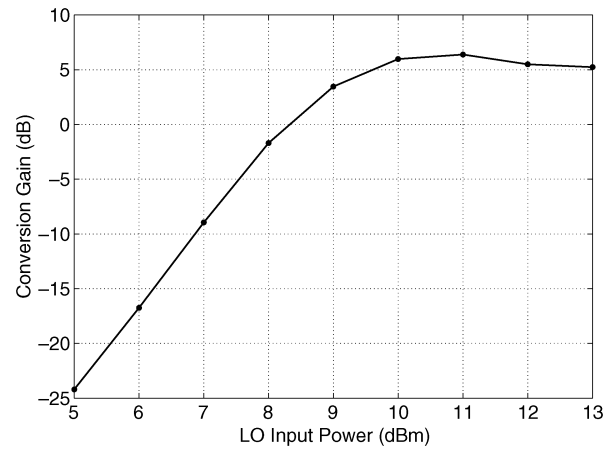


Fig. 10. Conversion gain at various LO power levels.

while having a 3 dB loss through the RF balun, and therefore higher conversion gains would be possible if a differential RF signal is already available. A conversion gain of approximately 6 dB is highest that could be found in the literature for a 4x SHM, e.g. [23]–[28] (most of which exhibit a conversion loss).

The possibility of a lower RF interfering signal mixing with a subharmonic of the LO was also considered. For example, a 6.1 GHz RF interfering signal could mix with the 2x LO component at 6 GHz, which would interfere with the desired IF signal. From the Taylor series expansion of the LO signal in (11), there is, ideally, no component at  $2f_{LO}$ , so the conversion gain from a 6.1 GHz RF to a 100 MHz IF should be very low (ideally zero). Simulations show that this conversion gain is 40 dB below that of the desired mixing products, and therefore this is not a serious concern (in addition there would likely be an RF filter that would attenuate out of band RF signals anyways).

The third-order intercept point and the second-order intercept point were measured to determine the linearity of the mixer. To measure the IP3, a two-tone RF signal was applied at 12.10 GHz and 12.11 GHz (LO power was 10 dBm at 3.0 GHz). This produced third-order distortion signals at 90 MHz and 120 MHz. The results are shown in Fig. 11. The IIP3 is approximately  $-2$  dBm and the OIP3 is approximately 4 dBm. To determine the IP2, the same two RF tones were applied (12.10 GHz and

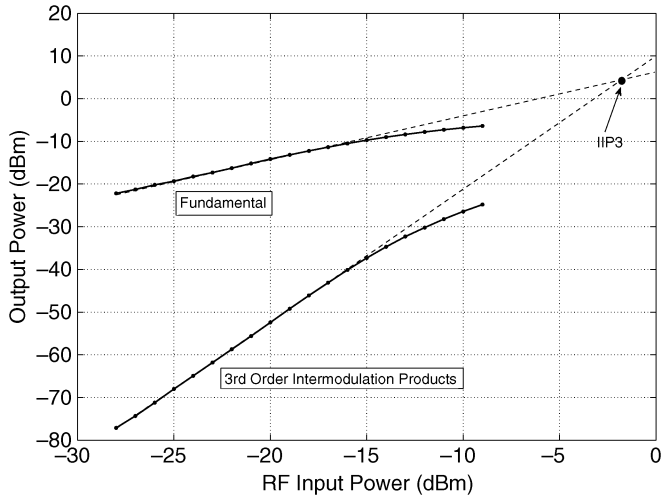


Fig. 11. Third-order intercept point measurement (LO power = 10 dBm).

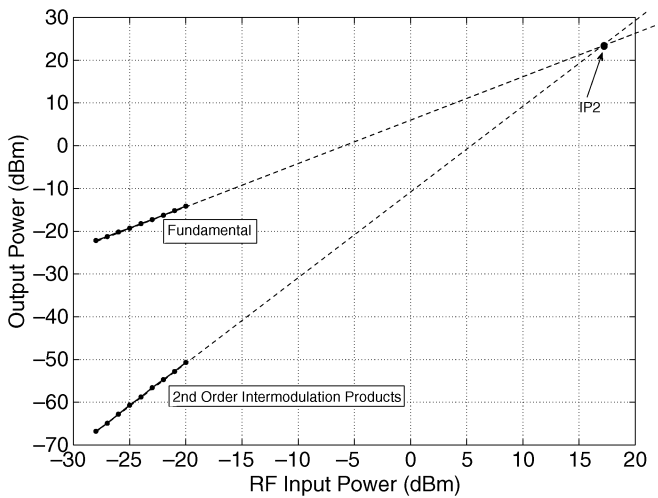


Fig. 12. Second-order intercept point measurement (LO power = 10 dBm).

12.11 GHz), but the spectral component at 10 MHz was observed as the RF input power increased. The plot of this measurement is shown in Fig. 12. The IIP2 was determined to be approximately 17 dBm. It was found through simulations that the output active balun seriously degrades the IP2. Simulations with an ideal IF output balun show that the IP2 is increased by 14 dB, and therefore, the IIP2 of the mixer itself is greater than 30 dBm.

The input reflection coefficient to the RF port was also measured using an Agilent 8510C network analyzer. A full-two port calibration was performed using a calibration substrate and the measured  $S_{11}$  is shown in Fig. 13. Due to the common-gate device in the RF balun there is relatively wideband input matching. The input reflection coefficient is better than  $-10$  dB between 10 GHz and 15 GHz.

To evaluate the susceptibility of the proposed SHM topology to DC offsets, the procedure discussed in [1] was used. Specifically, the DC level at the output was measured with three different setups: 1) Under DC bias only (RF and LO signals not applied), 2) DC bias and LO signal applied (no RF signal), and 3) DC bias with the LO signal and RF input. While performing

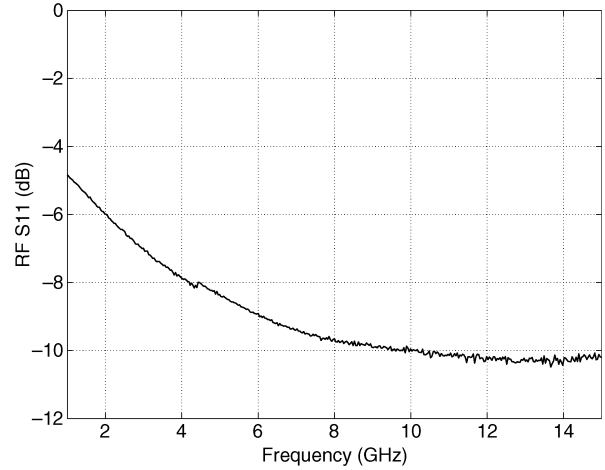


Fig. 13. Measured RF input reflection coefficient.

TABLE I  
PORT-TO-PORT ISOLATION MEASUREMENTS

Ports	Isolation
RF-LO	43 dB
LO-RF	71 dB
2LO-RF	52 dB
4LO-RF	59 dB
RF-IF	30 dB
LO-IF	68 dB
2LO-IF	55 dB
4LO-IF	59 dB

the measurement in Step 1) both the RF and LO ports were terminated in  $50 \Omega$  loads and in Step 2) the RF port was terminated in a  $50 \Omega$  load. The difference between the measured DC output values in Steps 1) and 2) indicate the amount of LO self-mixing. In the case of the proposed 4x SHM, this value was measured to be 4.2 mV at an LO power of 10 dBm. The measurement in Step 3) includes the effects of the DC offsets produced by second-order nonlinearities. The measured DC offset for this case was 1.2 mV.

The isolation between the ports of the mixer was measured and the results are compiled in Table I. Very high isolations between the ports were measured, with all isolations being greater than 43 dB with the exception of the RF-IF isolation (30 dB), which is predominately due to the amplitude and phase imbalance from the RF balun. The LO-RF and the 4LO-RF suppressions, in particular are very high at 71 dB and 59 dB, respectively. These isolation measurements are very competitive and in most cases improvements over previous SHMs (e.g., [8], [11], [13], [15], [18], [23], [24], [28]).

The double sideband (DSB) noise figure for the entire circuit was measured to be 15 dB (SSB NF  $\approx$  18), which includes the noise generated in the input RF balun. To determine the noise of the mixer alone, simulations were performed with an ideal input RF balun and the results show that the noise figure decreased by approximately 3 dB. Therefore, if a differential RF

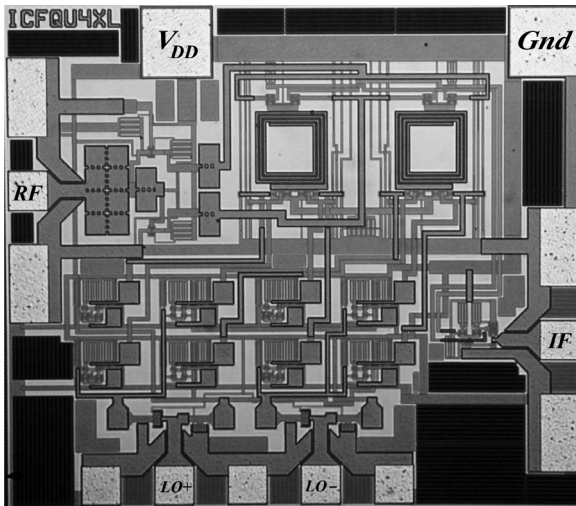


Fig. 14. Microphotograph of the proposed 4x SHM.

is already available, the DSB noise figure would be approximately 12 dB, which is similar to, or an improvement upon, the subharmonic mixers described in [10], [12]–[14], [18], [19], [22]. Flicker noise measurements were not performed due to an output DC-blocking capacitor. It is expected that the flicker noise will be increased somewhat compared to the traditional Gilbert-cell due to the additional LO switching noise, as discussed in [31].

The DC power consumption for the mixer core was approximately 5 mW and for the entire chip including the RF balun, LO octet-phase generation, mixer core, output balun, and buffer, the power consumption was measured to be 113 mW. The chip dimensions were  $850\ \mu\text{m} \times 850\ \mu\text{m}$  including pads. A photograph of the fabricated chip is shown in Fig. 14.

#### IV. CONCLUSION

A new 4x subharmonic mixer has been presented using CMOS 0.18  $\mu\text{m}$  technology that accepts a 12.1 GHz RF input signal and a 3.0 GHz LO signal and produces a 100 MHz IF output ( $f_{\text{RF}} - 4f_{\text{LO}}$ ). The circuit requires octet-phase LO signals, which are generated in this work through a polyphase filter and an active  $45^\circ$  phase shifting circuit. An active balun was used for the RF port to convert the single-ended 12.1 GHz signal to a differential signal and another active balun is used at the output to convert the differential output signal back to single-ended for measurement. A conversion gain of approximately 6 dB and a 1-dB compression point of  $-12$  dBm was obtained. Very high isolations between the ports were measured with LO-RF isolation of 71 dB and 4LO-RF isolation of 59 dB. The measured IIP3 and IIP2 are  $-2$  dBm and 17 dBm, respectively. The circuit dimensions are  $850\ \mu\text{m} \times 850\ \mu\text{m}$ . To the best of the authors' knowledge, this is the first 4x subharmonic mixer demonstrated in CMOS technology and it achieves the highest conversion gain for any 4x SHM to date. This circuit could be used to reduce the LO self-mixing in a direct conversion receiver, or in any mixer application where the reduction of the local oscillator frequency by a factor of four is beneficial.

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