Feedforward-Regulated Cascode OTA for Gigahertz Applications

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***Abstract*—A very high-frequency operational transconductance amplifier (OTA) with a new feedforward-regulated cascode topology is demonstrated in this paper. Experimental results show a bandwidth of 10 GHz and a large transconductance of 11 mS. A theoretical analysis of the OTA is provided which is in very good agreement with the measured results. We also carry out a Monte Carlo simulation to determine the effect of transistor mismatches and process variations on the transconductance and input/output parasitic capacitances of the OTA. The linearity and intermodulation distortion properties of the OTA, which are of particular interest in microwave applications, are experimentally determined using a purpose-built single-stage amplifier. For high-frequency demonstration purposes we built a larger circuit: an inductorless microwave oscillator. The fabricated oscillator operates at 2.89 GHz and has a significantly larger output voltage swing and better power efficiency than other inductorless oscillators reported in the literature in this frequency range. It also has a very good phase noise for this type of oscillators: −116 dBc/Hz at 1-MHz offset.**

***Index Terms*—Active filters, microwave integrated circuits, operational transconductance amplifiers (OTAs), oscillators, phase shifters.**

I. Introduction

WHILE numerous CMOS operational transconductance amplifiers (OTAs) with bandwidths exceeding several hundred MHz have been reported [1]–[10], there are comparatively few OTA designs that have broken into the GHz range. There are several important microwave applications that are well-suited for implementation with high-speed OTAs, such as phase shifters [11] and oscillators [12], [13]. It is also of major interest to design microwave tunable active filters using OTAs [14] to significantly reduce the use of passive transmission-line filters which are physically large since their dimensions are proportional to the wavelength of the signal in the substrate.

In this paper, we present an innovative very high-frequency fully differential OTA using a feedforward-regulated cascode topology. In contrast to OTAs using feedback-regulated cascode topologies [1], [15], [16], the feedforward approach proposed here can diminish time delay in the cascode regulation and thereby significantly increase its operating speed. The proposed OTA has a measured bandwidth of 10 GHz while simultaneously exhibiting a high amount of transconductance over this frequency span. Given that microwave circuits are predominantly characterized using S-parameter test sets and spectral domain techniques, we have conducted a set of specially designed experiments on the OTA to determine its microwave performance including its transconductance, output power 1-dB compression point, and third-order intercept point (IP3), which is a metric for the amplifier's intermodulation distortion performance. We have also designed and tested a basic oscillator circuit operating at 2.89 GHz using the OTA in order to demonstrate its high-frequency capabilities. We begin this paper with a description of the OTA circuit plus an in-depth theoretical treatment of the amplifier's gain, frequency response, and noise properties followed by simulation and experimental results.

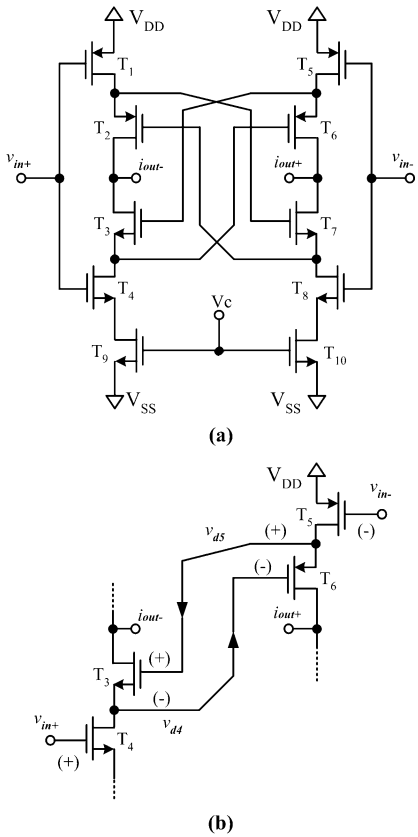

Fig. 1. (a) Proposed CMOS fully differential OTA using negative feedforward-regulated cascodes. (b) One pair of cross-connected cascodes.

II. Feedforward-Regulated Cascode OTA

The proposed CMOS OTA is presented in Fig. 1(a), which we first described in [17]. It has differential inputs and differential outputs, which allows the circuit to be used in both positive and

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negative feedback system configurations [18]. The OTA contains two pMOS regulated cascodes ($\mathrm{T}_1/\mathrm{T}_2$ and $\mathrm{T}_5/\mathrm{T}_6$) and two nMOS regulated cascodes ($\mathrm{T}_3/\mathrm{T}_4$ and $\mathrm{T}_7/\mathrm{T}_8$), where the pMOS cascodes have the same configuration as the nMOS cascodes and their DC currents are controlled by the two DC current sources at the bottom (T_9 and T_{10}). Instead of local negative feedback, this OTA uses a negative feedforward method for its four regulated-cascodes to speed up the regulating process. They are realized by two pairs of cross connections between the pMOS cascodes and the nMOS cascodes, which also work as the coupling between the two differential paths. To simplify the explanation of the feedforward configuration, Fig. 1(b) shows only one pair of the connections between the right pMOS cascode and the left nMOS cascode. Here we assume that a large differential signal ($v_{\mathrm{in}+}$ and $v_{\mathrm{in}-}$) is fed to the OTA, e.g., $v_{\mathrm{in}+}$ is at its high voltage with its signal polarity of $(+)$ and $v_{\mathrm{in}-}$ is at its low voltage with its signal polarity of $(-)$ in Fig. 1(b). If the cross connections did not exist, this large differential signal would cause a decrease of the drain voltage v_{d4} of the transistor T_4 and an increase of the drain voltage v_{d5} of the transistor T_5, which are marked with their signal polarities. The changes of the drain voltages would decrease the transconductance's linearity of the transistors T_4 and T_5 [15], [19]. With the cross connections, however, these drain-voltage changes can simultaneously cause an increase of the gate–source voltages of transistors T_3 and T_6, or an increase of their drain–source currents. The increase of their drain-source currents reduces the above changes of the drain voltages v_{d4} and v_{d5}. Therefore, the drain voltages v_{d4} and v_{d5} are kept stable through this process even if there is a large input signal. The other two cascode pMOS and nMOS transconductors not shown in Fig. 1(b) work in the same way as the ones just described. Because the regulating voltage of each cascode transconductor does not come from the output but instead from the other differential input, these regulating voltages are called negative feedforward rather than negative feedback.

In OTAs using feedback-regulated cascodes [1], [15], [16], the feedback network always introduces a delay during the voltage regulation process. However, in the proposed OTA, the feedforward topology can completely remove the regulating delay if v_{d4} and v_{d5} in Fig. 1(b) change at the same time, which can be attained by properly selecting the width ratio between the pMOS and the nMOS transistors. The use of the complementary field-effect transistor (FET) configuration has additional benefits such as enabling a symmetric output voltage swing and high transconductance. It also eliminates the need for any DC block and additional biasing circuitry when this OTA is cascaded with copies of itself, which greatly simplifies overall system design.

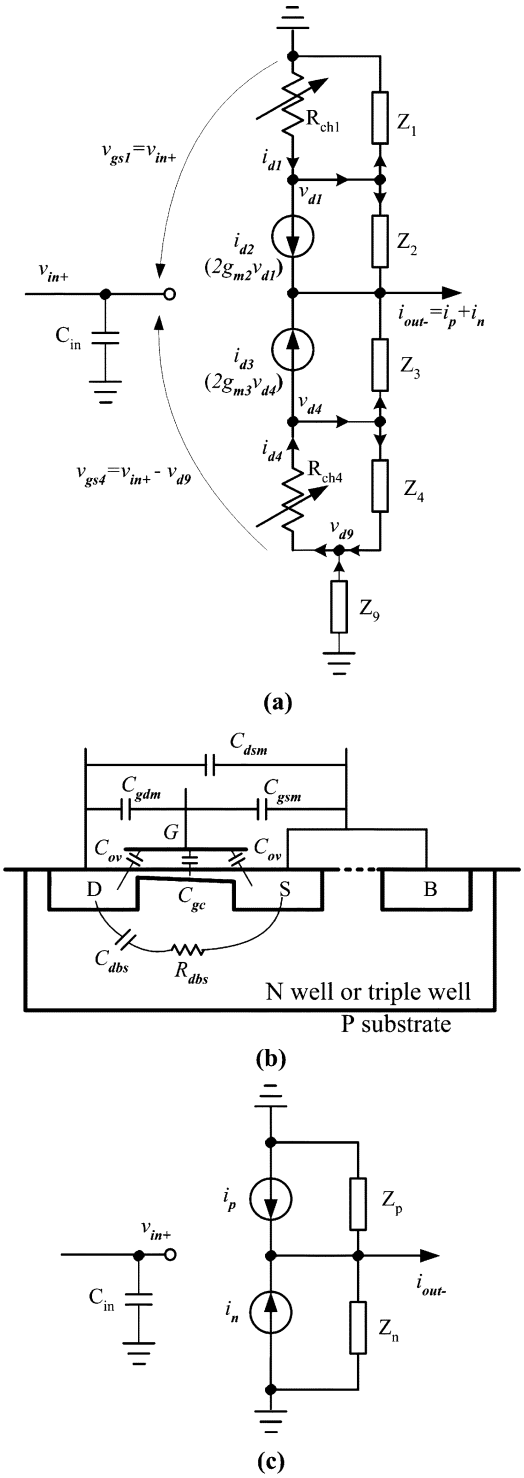

Fig. 2. (a) High-frequency half equivalent circuit model of the OTA in Fig. 1. (b) High-frequency MOSFET transistor model. (c) Simplified circuit model of the proposed OTA.

III. OTA Theoretical Analysis

Fig. 2(a) shows a high-frequency equivalent circuit of the left-half of the OTA in Fig. 1(a), where the transistor parasitics are modeled with an input capacitance C_{in} and impedances $Z_{1\sim4}$ and Z_9. The parasitics are determined using the generic MOSFET transistor model shown in Fig. 2(b). The transistor's body is isolated from the substrate by an N well for a pMOS or a triple well for an NMOS, to allow for a source–body connection. The equivalent circuit model in Fig. 2(a) can be simplified to the one shown in Fig. 2(c) to obtain the OTA's high-frequency transconductance and input/output impedances.

In the circuit of Fig. 1(a) and its 1/2 equivalent in Fig. 2(a), the top transistor T_1 is modeled by a variable channel resistance R_{ch1} because it operates in triode. Its RF current i_{d1} is given by

$$i_{d1} = -g_{m1}v_{\mathrm{in}+} \tag{1}$$

where $v_{\text{in}+}$ is one of the differential RF input signals and the transconductance g_{m1} can be calculated using the following expression derived from the short-channel drain current in the linear region [20]:

$$g_m \equiv \frac{dI_d}{dV_{\text{gs}}} = \mu C_{\text{ox}} \frac{W}{L} \frac{V_{\text{ds}}}{1 + V_{\text{ds}}/(E_{\text{sat}}L)}. \tag{2}$$

Transistor T_2 in the pMOS cascode works in the saturation region and its RF current is given by

$$i_{d2} \equiv -g_{m2} v_{\text{gs2}} \tag{3}$$

where v_{gs2} is the gate–source voltage, and the transconductance g_{m2} is calculated using the equation

$$g_m \equiv \frac{dI_d}{dV_{\text{gs}}} = v_{\text{sat}} C_{\text{ox}} W \left(1 - \left(\frac{E_{\text{sat}}L}{V_{\text{gs}} - V_t + E_{\text{sat}}L}\right)^2\right). \tag{4}$$

As described in Section II, the gate voltage of this PMOS device has an inverse polarity relative to its source voltage v_{d1}. If they are assumed to be exactly offset from each other, its gate–source voltage v_{gs2} becomes $-2v_{d1}$, and therefore (3) can be changed to

$$i_{d2} = 2g_{m2} v_{d1} \tag{5}$$

as illustrated in Fig. 2(a).

In a similar fashion, the RF currents in the nMOS cascode in Fig. 1(a) and its 1/2 equivalent model of Fig. 2(a) are given by

$$i_{d3} = 2g_{m3} v_{d4} \tag{6a}$$
$$i_{d4} = -g_{m4}(v_{in+} - v_{d9}) \tag{6b}$$

where v_{d4} and v_{d9} are the drain voltages of T_4 and T_9, respectively. g_{m3} can be calculated from (4) and g_{m4} from (2). Equation (6b) is different than (1) because of the bottom transistor T_9 used for dc biasing purposes, which is modeled by impedance Z_9.

The four shunt impedances, Z_1 to Z_4, are used to model the high-frequency parasitics of the cascode transistors. These impedances, together with Z_9, are given by

$$Z_1 = C_{\text{ds1}} // [R_{\text{dbs1}} + (j\omega C_{\text{dbs1}})^{-1}] \tag{7a}$$
$$Z_2 = R_{\text{ch2}} // C_{\text{ds2}} // [R_{\text{dbs2}} + (j\omega C_{\text{dbs2}})^{-1}] \tag{7b}$$
$$Z_3 = R_{\text{ch3}} // C_{\text{ds3}} // [R_{\text{dbs3}} + (j\omega C_{\text{dbs3}})^{-1}] \tag{7c}$$
$$Z_4 = C_{\text{ds4}} // [R_{\text{dbs4}} + (j\omega C_{\text{dbs4}})^{-1}] \tag{7d}$$
$$Z_9 = R_{\text{ch9}} // C_{\text{ds9}} // [R_{\text{dbs9}} + (j\omega C_{\text{dbs9}})^{-1}] \tag{7e}$$

where $C_{\text{ds1}\sim4}$ and $C_{\text{ds9}}$are the drain–source parasitic capacitances due to the interconnects and the gate oxide. From the transistor model in Fig. 2(b), these capacitances can be calculated from

$$C_{\text{ds}} = C_{\text{dsm}} // \frac{1}{1/C_{\text{gdm}} + 1/C_{\text{gsm}}} // \frac{1}{1/C_{\text{gdo}} + 1/C_{\text{gso}}} \tag{8}$$

where C_{dsm}, C_{gdm}, and C_{gsm} are parasitic capacitances due to the interconnects. C_{gdo} and C_{gso} are the gate–drain and gate–source capacitances due to the gate oxide, and each is a combination of gate–channel capacitance (C_{gc}) and the gate–drain/gate–source overlap capacitance (C_{ov}) in Fig. 2(b)[21]. $R_{\text{dbs1}\sim4}$, R_{dbs9}, $C_{\text{dbs1}\sim4}$ and C_{dbs9} in (7a)–(7e) are the drain–source parasitics through the body as illustrated in Fig. 2(b). $R_{\text{ch1}\sim4}$ and R_{ch9} are the transistor channel resistances. In the case of R_{ch2} and R_{ch3}, they are usually large in the saturation region and can be ignored for the first-order approximation. The channel resistances R_{ch1}, R_{ch4}, and R_{ch9} can be derived using

$$R_{\text{ch}} \equiv \left(\frac{dI_d}{dV_{\text{ds}}}\right)^{-1} = \frac{L}{\mu C_{\text{ox}} W} \frac{[1 + V_{\text{ds}}/(E_{\text{sat}}L)]^2}{(V_{\text{gs}} - V_t) - V_{\text{ds}} - \frac{V_{\text{ds}}^2}{2E_{\text{sat}}L}}. \tag{9}$$

Fig. 2(c) is a final simplified circuit model derived from Fig. 2(a). It has two RF output currents from the PMOS/NMOS cascodes (i_p and i_n), two output impedances (Z_p and Z_n), and one input capacitance C_{in}.

The output currents can be derived (see the Appendix) from the equivalent circuit model in Fig. 2(a) as

$$i_p = \frac{-g_{m1} v_{\text{in}+}(Z_1 + 2g_{m2} Z_1 Z_2)}{Z_1 + Z_2 + 2g_{m2} Z_1 Z_2} \tag{10a}$$
$$i_n \approx \frac{-g_{m4} v_{\text{in}+}(Z_4 + 2g_{m3} Z_3 Z_4)}{Z_4 + Z_3 + 2g_{m3} Z_3 Z_4} \tag{10b}$$

and, from these current equations, the overall OTA transconductance is found to be

$$\begin{aligned} g_{m,\text{OTA}} &= \frac{i_{\text{out}+} - i_{\text{out}-}}{v_{\text{in}+} - v_{\text{in}-}} \\ &= \frac{-(i_p + i_n)}{v_{\text{in}+}} \\ &= \frac{g_{m1}(Z_1 + 2g_{m2} Z_1 Z_2)}{Z_1 + Z_2 + 2g_{m2} Z_1 Z_2} + \frac{g_{m4}(Z_4 + 2g_{m3} Z_3 Z_4)}{Z_4 + Z_3 + 2g_{m3} Z_3 Z_4}. \end{aligned} \tag{11}$$

Clearly, the OTA transconductance has an imaginary part due to the complex impedances and the significance of this will be discussed later. As a check, if all of the impedances in (11) are set to infinity, the transconductance reduces to $g_{m,\text{OTA}} = g_{m1} + g_{m4}$, which is the expected result without parasitics.

As illustrated in Fig. 1(a), the OTA's input $v_{\text{in}+}$ is connected to the gates of the transistors T_1 and T_4, so the input impedance of the OTA seen at $v_{\text{in}+}$ is mainly capacitive (represented by C_{in}) and is given by

$$C_{\text{in}} = C_{g1} + C_{g4}. \tag{12}$$

The capacitances C_{g1} and C_{g4} can be calculated using

$$C_g = (C_{\text{gs}} + C_{\text{gsm}}) + (C_{\text{gd}} + C_{\text{gdm}})(1 - K) \tag{13}$$

where C_{gs} and C_{gd} are the gate–source and gate–drain MOS capacitances, and C_{gsm} and C_{gdm} are the parasitic capacitances of the interconnects. K is a coefficient due to the Millereffect, and is given by the ratio of the drain voltage and the gate voltage [22]

$$K = \text{Re}\left(\frac{v_d}{v_{\text{in}+}}\right) \tag{14}$$

where v_d refers to the drain voltage of T_1 or T_4 and can be computed using (A2)–(A6) in the Appendix.

The total output admittance of the OTA using the equivalent circuit in Fig. 2(c) is

$$Y_{\text{out}} = 1/Z_p + 1/Z_n \tag{15}$$

where Z_p and Z_n are the output impedances of the pMOS and nMOS cascodes, respectively, and they are given by (see the Appendix)

$$Z_p = 2g_{m2}Z_2(Z_1//R_{\text{ch1}}) + (Z_1//R_{\text{ch1}}) + Z_2 \tag{16a}$$

$$Z_n = 2g_{m3}Z_3(Z_4//R_{\text{ch4}} + Z_9) + (Z_4//R_{\text{ch4}} + Z_9) + Z_3. \tag{16b}$$

Equation (16a) suggests that the output impedance of the regulated cascode at microwave frequencies is increased approximately by a factor of $(A+1)g_{m2}Z_2$ compared to its common-source stage, where A is the regulation gain. The linearity of the OTA is increased by a similar factor, which has positive implications for large-signal operation. The 3-dB cutoff frequency of the OTA can be estimated from the model in Fig. 2(c) using the open-circuit time-constants (OCτs) method [23]

$$\begin{aligned}\omega_h &\approx \frac{1}{R_{\text{out}}(C_{\text{out}} + C_L)} \\ &= \frac{1}{\frac{1}{\text{Re}(Y_{\text{out}})}\left[\text{Im}(Y_{\text{out}})/\omega + C_L\right]}\end{aligned} \tag{17}$$

where the OTA output is assumed to be connected to a capacitive load C_L.

The output noise of a basic cascode is mainly determined by its common-source stage [24], [25], while a regulated cascode has different noise contributions due to the feedback or feedforward mechanism. Little work has been devoted to the noise analysis of the regulated cascodes, thus it is essential here to carry out an analysis of the proposed feedforward-regulated OTA, which can be used to analyze other feedback-regulated cascodes with minor changes. Fig. 3 gives a thermal noise model of the OTA, where only the left nMOS cascode and the right pMOS cascode are shown and each transistor is accompanied with a channel thermal noise current, ignoring gate induced noise for simplicity. The high-frequency parasitics ($Z_1 \sim Z_9$) are also ignored. The channel thermal noise current of each transistor is given by

$$\overline{i_{n,x}^2} = 4kT\gamma_x g_{d0,x}\Delta f \tag{18}$$

where the subscript x denotes the specific transistor in question and γ and g_{d0} refer to its bias-dependent factor and zero-bias drain conductance respectively. To determine the noise current output from the left nMOS cascode, the two noise voltages at nodes v_{d4} and v_{d5} are computed first as

$$\overline{v_{n,d4}^2} \approx \left(\overline{i_{n,3}^2} + \overline{i_{n,4}^2}\right)/g_{m3}^2 \tag{19a}$$

$$\overline{v_{n,d5}^2} \approx \left(\overline{i_{n,5}^2} + \overline{i_{n,6}^2}\right)/g_{m6}^2. \tag{19b}$$

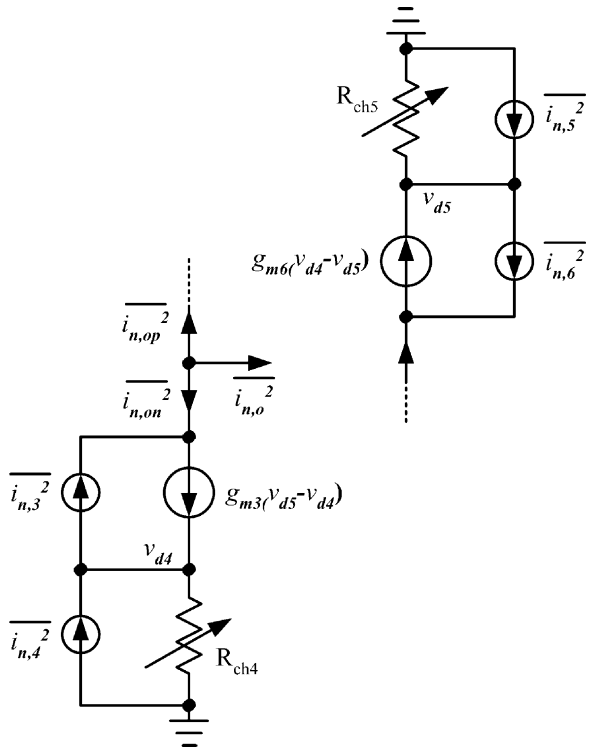

Fig. 3. Thermal noise model of the proposed OTA.

In the above, it is assumed that $R_{\text{ch4}} \ll 1/g_{m3}$ and $R_{\text{ch5}} \ll 1/g_{m5}$. The noise current output of the left nMOS cascode is then

$$\begin{aligned}\overline{i_{n,\text{on}}^2} &= g_{m3}^2\left(\overline{v_{n,d5}^2} + \overline{v_{n,d4}^2}\right) - \overline{i_{n,3}^2} \\ &\approx \overline{i_{n,4}^2} + \frac{g_{m3}^2}{g_{m6}^2}\left(\overline{i_{n,5}^2} + \overline{i_{n,6}^2}\right)\end{aligned} \tag{20}$$

where the noise current $\overline{i_{n,3}^2}$ is cancelled out due to its correlation with the current source $g_{m3}(v_{d5} - v_{d4})$ via v_{d4}, which is denoted with a minus sign in (20). This is consistent with the case of the basic cascode [24], [25]. Similarly the output noise current from the left pMOS cascode (not shown in Fig. 3) is

$$\overline{i_{n,\text{op}}^2} \approx \overline{i_{n,1}^2} + \frac{g_{m2}^2}{g_{m7}^2}\left(\overline{i_{n,7}^2} + \overline{i_{n,8}^2}\right) \tag{21}$$

resulting in a total output noise current on the left half of the circuit of

$$\begin{aligned}\overline{i_{n,o}^2} &= \overline{i_{n,\text{on}}^2} + \overline{i_{n,\text{op}}^2} \\ &\approx \overline{i_{n,1}^2} + \overline{i_{n,4}^2} + \frac{g_{m2}^2}{g_{m7}^2}\left(\overline{i_{n,7}^2} + \overline{i_{n,8}^2}\right) \\ &\quad + \frac{g_{m3}^2}{g_{m6}^2}\left(\overline{i_{n,5}^2} + \overline{i_{n,6}^2}\right).\end{aligned} \tag{22}$$

Using (18), (22), and the simplified OTA transconductance without parasitics $g_{m,\text{OTA}} = g_{m1} + g_{m4}$, the noise excess factor [26] of the OTA can be determined as

$$\begin{aligned}\text{NEF} &\equiv \overline{i_{n,o}^2}/(4kTg_{m,\text{OTA}}\Delta f) \\ &\approx \left[\gamma_1 g_{d0,1} + \gamma_4 g_{d0,4} + \frac{g_{m2}^2}{g_{m7}^2}(\gamma_7 g_{d0,7} + \gamma_8 g_{d0,8})\right. \\ &\quad \left. + \frac{g_{m3}^2}{g_{m6}^2}(\gamma_5 g_{d0,5} + \gamma_6 g_{d0,6})\right] \Big/ (g_{m1} + g_{m4}).\end{aligned} \tag{23}$$

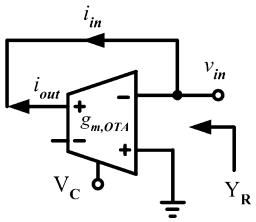

Fig. 4. Block diagram of the OTA synthetic resistor.

The first two terms in the numerator of (23) are the noise contributions without regulation, which is the case of the basic cascode, and the remaining two terms model the extra noise contributions from the feedforward regulation. The extra noise contributions also exist in other feedback-regulated cascodes.

IV. Microwave Performance: Simulated and Experimental Results

Several circuits were fabricated in order to characterize the performance of the OTA and to demonstrate its microwave capabilities. The basic OTA cell, implemented in a standard 0.18-μm CMOS process, measured 145 μm $\times$ 67 μm and used a dc supply voltage of ± 1.4 V.

A. Transconductance and Frequency Response

Because an OTA has a voltage input and a current output, it is not possible to do a direct microwave measurement of its transconductance $(g_{m,\mathrm{OTA}})$ using an S-parameter test set. Therefore, the OTA was used to make a synthetic resistor [18] as shown in Fig. 4 and, by measuring the resistor's reflection coefficient (S_{11}) with an S-parameter test set, we are able to find its input admittance using

$$Y_R = Y_0 \left(\frac{1 - S_{11}}{1 + S_{11}} \right) \tag{24}$$

and, from this, the OTA transconductance can be approximated using $|g_{m,\mathrm{OTA}}| \approx \mathrm{Re}(Y_R)$. The justification for this approach to find the transconductance is that a synthetic resistor is the simplest possible OTA circuit. The imaginary part of Y_R can be used to determine the OTA input/output parasitic capacitances.

Figs. 5 and 6 show the calculated, simulated, and experimental results for the transconductance and the input/output parasitic capacitances of the OTA, and the agreements are excellent. The theoretical curves are obtained using the analysis in Section III and the simulated results are using the Agilent ADS package. As revealed in Fig. 5, the OTA can achieve a large transconductance of about 11 mS throughout an ultra-wide band of 10 GHz. From Fig. 6, the input/output parasitic capacitance C_P of the fabricated OTA is about 0.13 pF.

A Monte Carlo simulation [27]–[29] was carried out to examine the effects of device mismatches and process variations on the OTA's transconductance and parasitic capacitances. In the simulation, 1% deviations with a Gaussian distribution in the transistor W/L ratio are applied to all devices. Both mismatch and process variation models were used. Fig. 7 shows

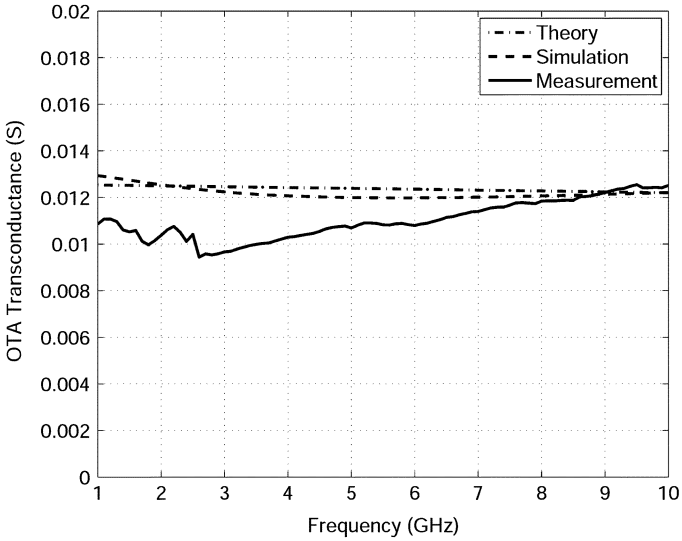

Fig. 5. Proposed OTA's transconductance ($\mathrm{V_C} = -0.55$ V).

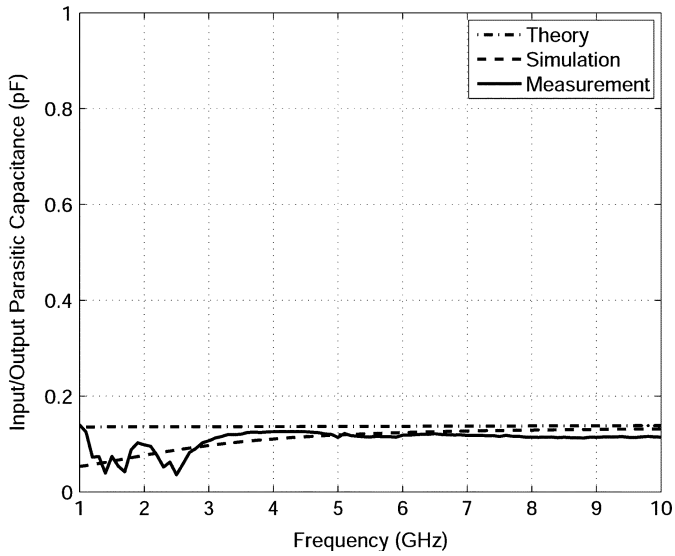

Fig. 6. Input/output parasitic capacitance of the proposed OTA ($\mathrm{V_C} = -0.55$ V).

the Monte Carlo results and a comparison of the two distributions indicates that the OTA's transconductance is less sensitive to mismatches and process variations than the input/output parasitic capacitance.

Power-supply noise can also affect the performance of the OTA, especially at microwave frequencies. A power supply sensitivity simulation was carried out on the OTA at different frequencies and the results are listed in Table I. As indicated, at low frequencies, this OTA has a high power-supply- rejection-ratio (PSRR) of over 86 dB while at microwave frequencies the PSRR drops to 30–40 dB. This degradation is due to the increased power-supply noise coupling to the OTA's output at microwave frequencies by means of the parasitic reactance. To alleviate the impact of the high-frequency PSRR degradation, on-chip shunt capacitors are usually introduced at the dc power supply nodes in microwave ICs to create virtual RF grounds at those points. This approach was used in the circuits that follow.

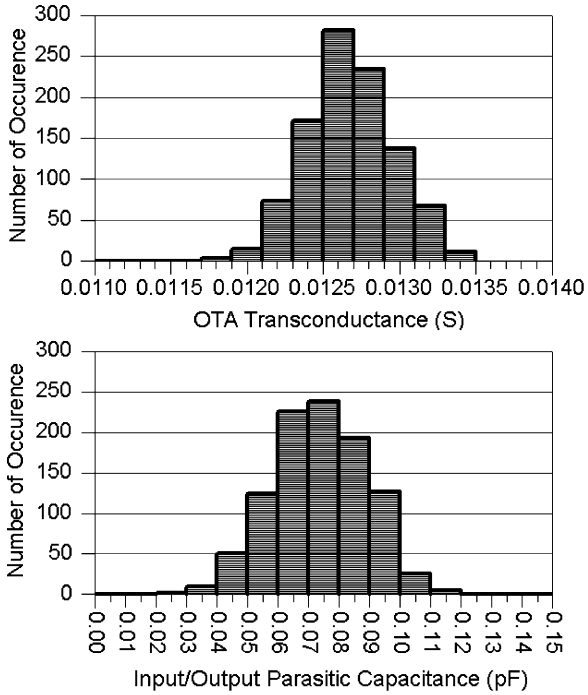

Fig. 7. The distributions of the transconductance and the input/output parasitic capacitance with 1% deviations of W/L for all transistors in the Monte Carlo simulation (@2GHz).

TABLE I
PSRR FROM THE SIMULATION

PSRR (dB)	@10MHz	@4GHz
PSRR+ (for V_{DD})	90.4	41.5
PSRR- (for V_{SS})	86.2	36.9

B. Power and Intermodulation Distortion Performance

A single-stage fully differential microwave amplifier shown in Fig. 8(a) was specially designed to test the power and intermodulation distortion behavior of the OTA. Fig. 8(b) gives a microphotograph of the fabricated amplifier. The IC measures 0.14 mm^2 and dissipates 56 mW of dc power. In the schematic, a resistor feedback network consisting of R_2 and R_3 is used to convert the current output of the OTA to a voltage output $\mathrm{V_A}$. Two identical resistors, R_1, were used for wideband input impedance matching to the external 50-Ω measurement system and a pair of voltage followers was used at the output also for impedance matching. The gain G of this test amplifier can be easily obtained by exploiting the symmetry of the circuit

$$G = \frac{V_O+}{V_I+} = \frac{V_A}{V_I+} = \frac{1-|g_{m,\mathrm{OTA}}|R_3}{1+|g_{m,\mathrm{OTA}}|R_2}. \tag{25}$$

Note that the voltage followers are assumed to be ideal in the derivation of (25), i.e., $V_O+ = V_A$. In the physical implementation, $R_2 = 300\ \Omega$, $R_3 = 1500\ \Omega$, and $|g_{m,\mathrm{OTA}}| = 11$ mS, which gives a gain of $|G| = 3.6$ V/V in theory. Now taking into account the actual voltage loss through the followers, the total gain of the test amplifier is about 4.25 dB (see Fig. 9).

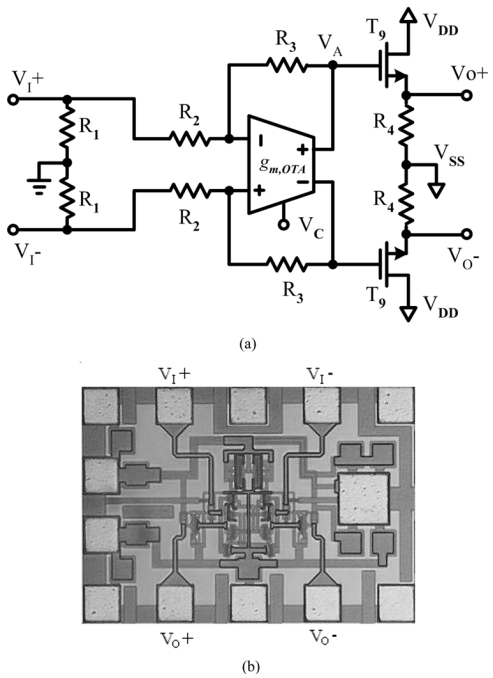

Fig. 8. (a) Schematic and (b) microphotograph of the single-stage differential amplifier.

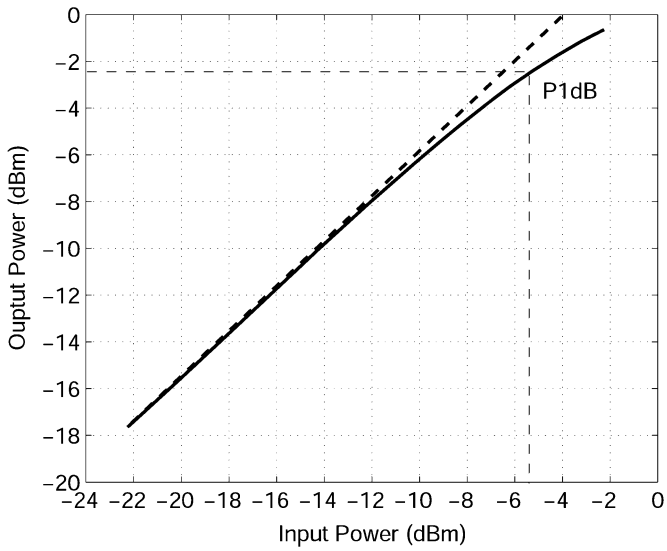

Fig. 9. Measured P1 dB compression point of the test amplifier in Fig. 8(a).

An output power $(\mathrm{P_{out}})$ versus input power $(\mathrm{P_{in}})$ measurement was performed on the test amplifier at 2.0 GHz in order to determine the output 1-dB compression point $(\mathrm{P_{1\ dB}})$ of the OTA, which is a key linearity metric in microwave circuits along with the IP3. The $\mathrm{P_{out}}$ versus $\mathrm{P_{in}}$ curve is shown in Fig. 9 and it reveals an output $\mathrm{P_{1\ dB}}$ of -2.5 dBm.

A two-tone test was done to measure the intermodulation distortion of the OTA and to determine its IP3. The input tones were $f_1 = 1.99$ GHz and $f_2 = 2.01$ GHz and the results are plotted in Fig. 10. The graph shows a high input IP3 of $+6$ dBm and a high output IP3 of $+8$ dBm. In fact, the output IP3 of the OTA itself can be even better than this because the single-transistor voltage followers in the test amplifier limit the output IP3.

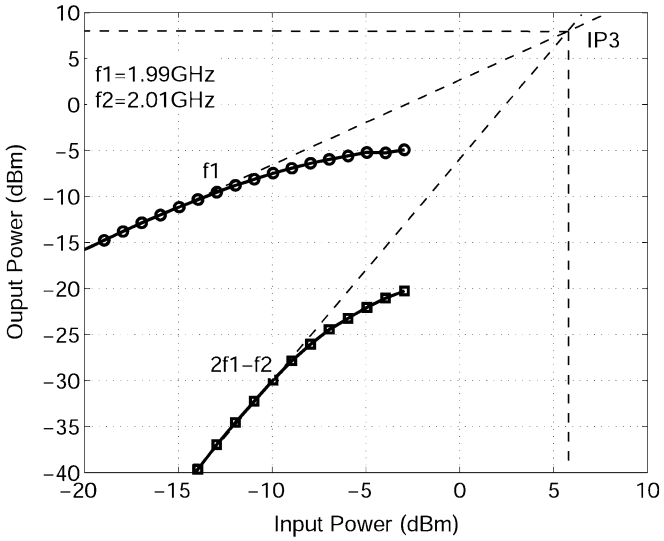

Fig. 10. Measured IP3 intermodulation of the test amplifer in Fig. 8(a) with two-tone signal inputs.

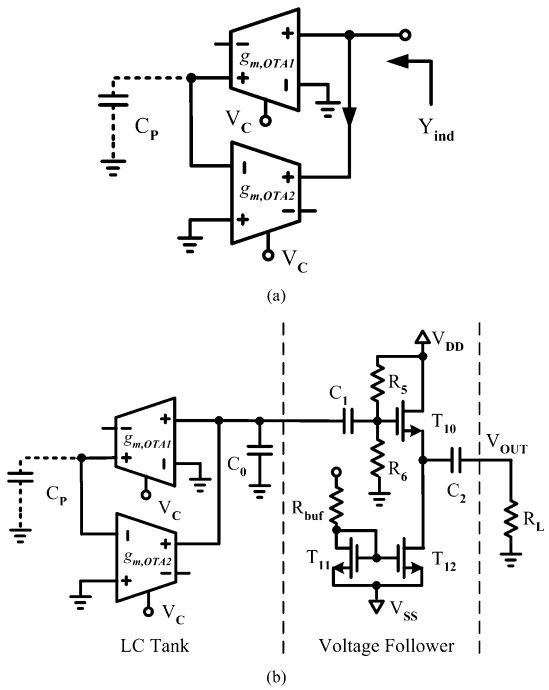

Fig. 11. Schematics of (a) the active inductor and (b) the active-inductor-based oscillator.

C. Demonstration Circuit: A Microwave Oscillator

To demonstrate the superior microwave capabilities of the OTA presented in this work, a larger circuit was designed and fabricated. The circuit is an oscillator using a well-known active-inductor configuration and it is shown in Fig. 11. The active inductor is created using the impedance inverter illustrated in Fig. 11(a). The ideal input impedance looking into this inverter circuit is [18]

$$Z_{\text{ind}} = \frac{j\omega C_P}{g_{m,\text{OTA1}} \cdot g_{m,\text{OTA2}}} = j\omega L'. \tag{26}$$

It is clear that the OTA's transforms the parasitic capacitance, C_p, into an inductance of value $L' = C_p/(g_{m,\text{OTA1}}.g_{m,\text{OTA2}})$. According to Section III, the transconductances have an imaginary part though due to the circuit parasitics at high frequencies. Writing the transconductances in exponential form with ϕ_1 and ϕ_2 as the phase angles, (26) can be rewritten as

$$\begin{aligned} Z_{\text{ind}} &= \frac{j\omega C_P}{g_{m,\text{OTA1}} \cdot e^{-j\phi_1} \cdot g_{m,\text{OTA2}} \cdot e^{-j\phi_2}} \\ &= \frac{-\omega C_P \sin(\phi_1+\phi_2) + j\omega C_P \cos(\phi_1+\phi_2)}{g_{m,\text{OTA1}} \cdot g_{m,\text{OTA2}}} \\ &= R' + j\omega L'. \end{aligned} \tag{27}$$

The real part in (27) represents a negative resistance if $\phi_1$and ϕ_2 are small. Note that this negative resistance can be used to compensate the losses in the active inductor to achieve a high-Q and if the negative resistance is large enough then it can also be used to implement an oscillator as described below. The imaginary part in (27) represents the modified reactance of the active inductance L'. Taking the other parasitic capacitance C_P on the right side of the impedance inverter into account, not shown in Fig. 11(a), the active inductance becomes

$$L = L' + \left(\frac{\omega^2 L' C_P}{1-\omega^2 L' C_P}\right) \cdot L' \tag{28}$$

where $L\prime$ is obtained from (27). The fabricated active inductor has a constant inductance of about 4.7 nH up to 2.5 GHz both in the simulation and in measurement, and the detailed results can be found in [17].

Fig. 11(b) shows the oscillator topology implemented here using the active inductor plus a small capacitor C_0 to create an *LC*-tank. A voltage follower is placed right after the *LC*-tank to drive the external 50-Ω load R_L. The follower is a common-drain transistor (T_{10}) with a current mirror (T_{11} and T_{12}) to bias T_{10}. The gain needed to start and sustain the oscillation comes directly from the negative resistance of the active inductor. This eliminates the need for additional gain blocks and makes the design of the oscillator simple and compact. The oscillation frequency is determined by the *LC*-tank

$$f_{\text{VCO}} = \frac{1}{2\pi\sqrt{\text{LC}_{\text{eq}}}} \tag{29}$$

where C_{eq} includes C_0 and the parasitic capacitance from the following follower.

A microphotograph of the fabricated oscillator is presented in Fig. 12, and it has a size of only 400 μm × 260 μm (excluding the bonding pads). It consumes 95 mW of dc power. Fig. 13 shows the spectral output of the oscillator at the fundamental tone and Fig. 14 shows a wideband spectral graph that includes the harmonic outputs. The fabricated oscillator operates at 2.89 GHz and it delivers -8 dBm of power at this frequency. Due to the high linearity of the OTAs, the oscillator exhibits 20- and 37-dB suppression of the second- and third-harmonic outputs, respectively, as shown in Fig. 14.

The oscillator fundamental output frequency can be tuned by almost 200 MHz from 2.7 to 2.89 GHz, as shown in Fig. 15 which depicts frequency versus OTA bias current control voltage (V_c). This control voltage changes the value of the

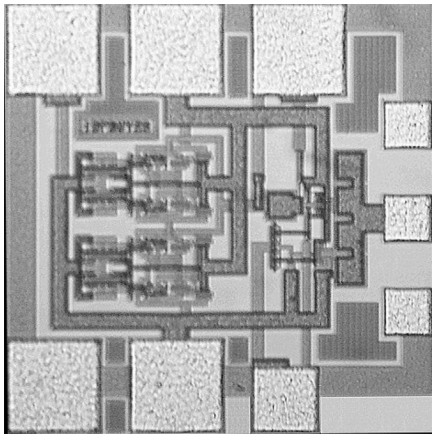

Fig. 12. Microphotograph of the fabricated oscillator.

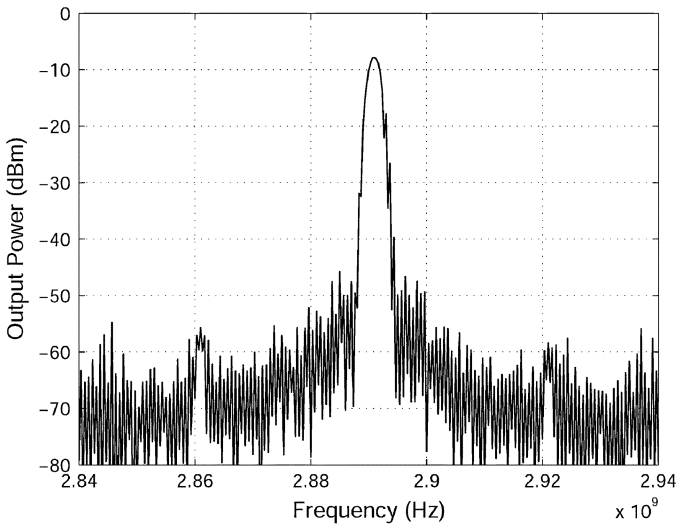

Fig. 13. Measured output fundamental spectrum of the oscillator at $V_C = -0.55$ V.

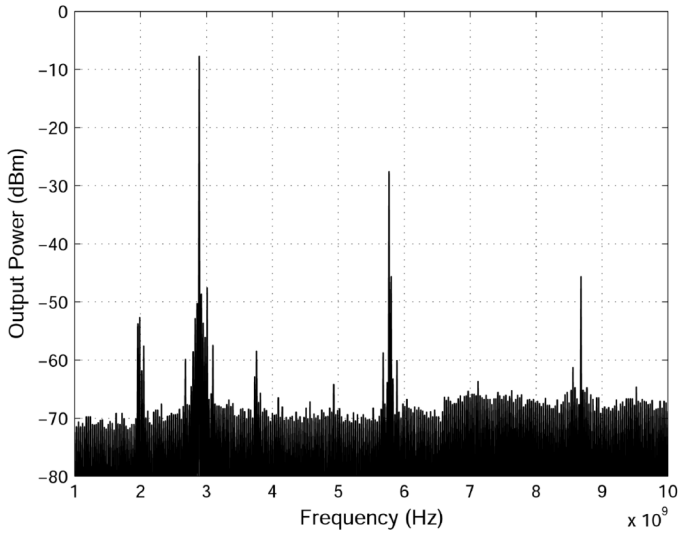

Fig. 14. Measured output harmonic spectra of the oscillator at $V_C = -0.55$ V.

active inductor and thereby tunes the *LC*-tank of the oscillator. Fig. 15 also shows the output power of the fundamental and

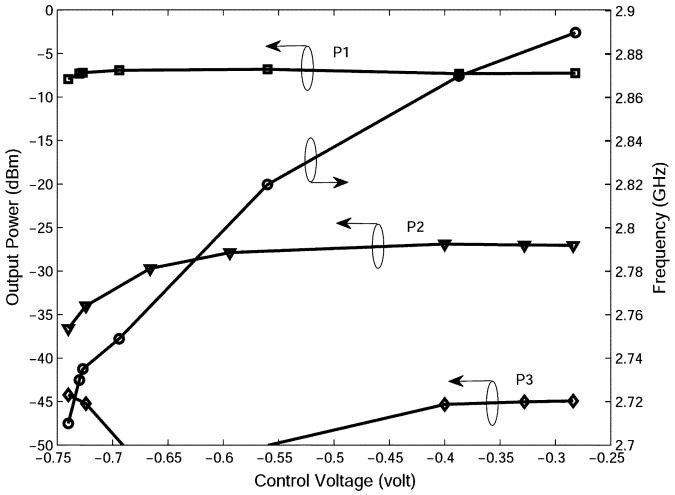

Fig. 15. Measured harmonic output powers and frequency versus the control voltage of the oscillator.

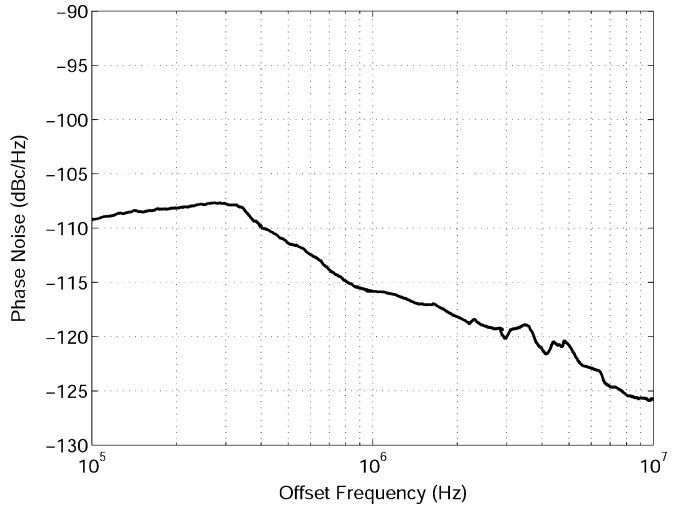

Fig. 16. Measured phase noise of the oscillator at 2.89 GHz.

second and third harmonics versus control voltage. The fundamental output power only varies between -7 and -8 dBm.

The measured phase noise of the oscillator at 2.89 GHz is presented in Fig. 16. Due to the high Q factor of the active inductor, a very low phase noise (in the inductorless oscillator category) of -109, -116, and -126 dBc/Hz is achieved at frequency offsets of 100 kHz, 1 MHz, and 10 MHz, respectively. This phase noise result is approaching the minimum achievable phase noise for inductorless oscillators [30]. A comparison between this oscillator and recent works [12], [13] reporting inductorless oscillators in the microwave range is shown in Table II, and it is clear that this oscillator outperforms the others.

V. Conclusion

A feedforward-regulated cascode OTA has been proposed, analyzed, and experimentally demonstrated in this paper that can operate at very high speeds. The OTA has a large transconductance, high linearity, and low intermodulation distortion, which makes it very suitable for implementing numerous types of microwave integrated circuits. An oscillator was designed

TABLE II
COMPARISONS BETWEEN THIS WORK AND THE RECENT WORKS

Oscillators using active inductor		**This work**	**[12]**	**[13]**
CMOS Technology		0.18 μm	0.18 μm	0.18 μm
Output Power (dBm)		-7 to -8	-14 to -22	-21 to -29
DC to RF Power Efficiency (%)		0.21%	0.14%	0.03%
Phase noise (dBc/Hz)	100 KHz offset	-109 @ 2.89 GHz	-78 @ 2.9 GHz	-60 @ 1.67 GHz
	1 MHz offset	-116 @ 2.89 GHz	-102 @ 2.9 GHz	-90 @ 1.67 GHz
	10 MHz offset	-126 @ 2.89 GHz	-122 @ 2.9 GHz	-90 @ 1.67 GHz

for demonstration purposes using the OTA in this work, and it can achieve a relatively large output voltage swing with a very low phase noise.

APPENDIX

A. Derivation of i_p and i_n

A derivation of the RF currents i_p and i_n in Fig. 2(c) follows. In the equivalent circuit of the pMOS cascode in Fig. 2(a), assuming the output node is grounded, an equation can be obtained by applying Kirchhoff's current law at the voltage node v_{d1}

$$i_{d1} - 2g_{m2}v_{d1} = \frac{v_{d1}}{(Z_1//Z_2)} \tag{A1}$$

which results in

$$v_{d1} = \frac{i_{d1}(Z_1//Z_2)}{1 + 2g_{m2}(Z_1//Z_2)}. \tag{A2}$$

Therefore, the RF current from the pMOS cascode to the output is given by

$$\begin{aligned} i_p &= i_{d1} - \frac{v_{d1}}{Z_1} = \frac{i_{d1}(Z_1 + 2g_{m2}Z_1Z_2)}{Z_1 + Z_2 + 2g_{m2}Z_1Z_2} \\ &= \frac{-g_{m1}v_{\text{in}+}(Z_1 + 2g_{m2}Z_1Z_2)}{Z_1 + Z_2 + 2g_{m2}Z_1Z_2}. \end{aligned} \tag{A3}$$

By applying the same law at the voltage nodes of v_{d4} and v_{d9}, two equations can be obtained for the nMOS cascode

$$i_{d4} - 2g_{m3}v_{d4} = \frac{v_{d4}}{Z_3} + \frac{v_{d4} - v_{d9}}{Z_4} \tag{A4}$$

$$i_{d4} = \frac{-v_{d9}}{Z_9} + \frac{v_{d4} - v_{d9}}{Z_4}. \tag{A5}$$

Substituting i_{d4} from (6b) in Section III into (A4) and (A5) and solving for v_{d9} yields

$$v_{d9} = \frac{g_{m4}v_{\text{in}+}Z_9(2g_{m3}Z_3Z_4 + Z_4)}{Z_4 + Z_3 + 2g_{m3}Z_3Z_4 + Z_9(1 + g_{m4}Z_4)(2g_{m3}Z_3 + 1)}. \tag{A6}$$

Thus, the RF current from the nMOS cascode to the output is given by

$$\begin{aligned} i_n &= \frac{-v_{d9}}{Z_9} \\ &= \frac{-g_{m4}v_{\text{in}+}(Z_4 + 2g_{m3}Z_3Z_4)}{Z_4 + Z_3 + 2g_{m3}Z_3Z_4 + Z_9(1 + g_{m4}Z_4)(2g_{m3}Z_3 + 1)}. \end{aligned} \tag{A7}$$

In the design of the proposed OTA, two transistors with a relatively-large size are used for the bottom DC current sources T_9 and T_{10}, so the impedance Z_9 is small compared to Z_3 and Z_4 and the term including it in the denominator in (A7) is negligible. Therefore, (A7) can be approximated by

$$i_n \approx \frac{-g_{m4}v_{\text{in}+}(Z_4 + 2g_{m3}Z_3Z_4)}{Z_4 + Z_3 + 2g_{m3}Z_3Z_4} \tag{A8}$$

which has a similar format as (A3).

B. Derivation of Z_p and Z_n

The output impedances Z_p and Z_n in Fig. 2(c) can be derived from the equivalent circuit model in Fig. 2(a) as follows. By applying an RF voltage v_x at the OTA's output in Fig. 2(a) and assuming it induces an RF current i_{xp} to the pMOS cascode, two equations can be obtained as

$$i_{\text{xp}} = \frac{v_x - v_{d1}}{Z_2} - 2g_{m2}v_{d1} \tag{A9}$$

$$i_{\text{xp}} = \frac{v_{d1}}{R_{\text{ch1}}//Z_1}. \tag{A10}$$

The output impedance of the pMOS cascode can be derived from the above two equations as

$$Z_p = \frac{v_x}{i_{\text{xp}}} = 2g_{m2}Z_2(Z_1//R_{\text{ch1}}) + (Z_1//R_{\text{ch1}}) + Z_2. \tag{A11}$$

Using the same way, the output impedance of the nMOS cascode can also be derived as

$$Z_n = 2g_{m3}Z_3(Z_4//R_{\text{ch4}} + Z_9) + (Z_4//R_{\text{ch4}} + Z_9) + Z_3. \tag{A12}$$

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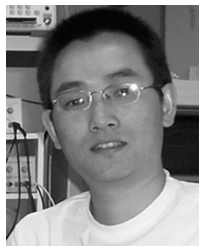

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