A Frequency Tripler Using a Subharmonic Mixer and Fundamental Cancellation

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***Abstract*—A new odd-order frequency multiplier topology is demonstrated in this work that uses a subharmonic mixer to realize a frequency tripler. A feedforward circuit is used for fundamental cancellation at the output and eliminates the need for filtering structures. For demonstrative purposes, and to validate the concept, a 1–3-GHz proof-of-concept frequency tripler circuit was fabricated. The tripler circuit achieved a measured output fundamental suppression of up to 30 dB below the third harmonic and a conversion gain of up to 3 dB. The circuit was implemented in CMOS 0.18-μm technology and the chip area was 0.8 mm^2 including bonding pads.**

***Index Terms*—CMOS analog integrated circuits, frequency conversion, frequency tripler, monolithic microwave integrated circuits (MMICs), subharmonic mixer (SHM).**

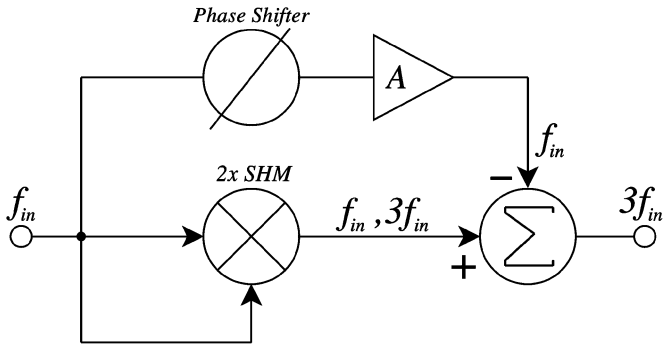

Fig. 1. Block diagram of the proposed frequency tripler.

I. Introduction

THERE ARE many frequency multiplier techniques for generating a harmonic frequency from a fundamental input frequency. Even-order multipliers that create harmonics of the type 2^n, where n is an integer, are conveniently designed by exploiting the square-law current–voltage characteristic of field-effect transistors (FETs) or by using antiparallel diodes. However, odd-order frequency multipliers such as triplers are more challenging to design because a simple cubic-law device is not readily available in standard FET or bipolar integrated circuit processes. Therefore, custom-built devices such as heterostructure and quantum barrier varactor diodes [1]–[3] with strongly nonlinear I–V curves are regularly used in frequency triplers. To circumvent the use of nonstandard semiconductor devices, triplers can be realized by over-driving a transistor with the sinusoidal input signal to generate a clipped waveform rich in odd-order harmonics [4]–[8]. This method, however, usually requires strong filtering at the output to remove the fundamental and other unwanted frequencies. Often the filtering has to be accomplished off-chip to improve signal rejection. Balanced frequency tripler circuits based on extracting the third harmonic generated by FET nonlinearities are presented in [9] and [10] with on-chip filtering and cancellation of unwanted harmonics, but the required chip area can be very large (e.g., 5.0 mm^2 in [9] and 2.32 mm^2 in [10]). Injection locking can also be used to implement a frequency tripler [11], [12], although the resonator used in the oscillator can consume a large chip area and can limit the bandwidth of the circuit. Recent advances in integrated circuit tripler design [13] have used waveform shaping techniques in order to generate the triple frequency and to relax the output filter requirements.

In this paper, an innovative fully integrated frequency tripler is presented. As shown in Fig. 1, the incident signal $f_{\rm in}$ is fed to both inputs of a $2\times$ subharmonic mixer (SHM) to generate the output frequencies $3f_{\rm in}$ and $f_{\rm in}$. The circuit includes a feedforward mechanism to cancel the $f_{\rm in}$ signal at the output, leaving only the $3f_{\rm in}$ signal. The use of an SHM has the additional advantage that it naturally suppresses the second, fourth, and other harmonics. A proof-of-concept circuit operating at a 3.0-GHz output frequency was fabricated using a standard 0.18-μm CMOS process and its performance was measured. While this new tripler concept is demonstrated at S-band, it could be employed at higher frequencies where the use of frequency multipliers may be inevitable.

II. Circuit Description

As shown in Fig. 1, there are four subcircuits in the proposed frequency tripler: a $2\times$ SHM, a subtractor circuit, and a feedforward circuit consisting of a phase shifter and an amplifier. At the output of the SHM are the up- and down-converted frequency components $(2f_{\rm in} \pm f_{\rm in})$ at $3f_{\rm in}$ and $f_{\rm in}$. The fundamental feedforward phase shifter and amplifier are designed to match the phase and amplitude of the fundamental component at the SHM output so that significant fundamental cancellation can occur in the subtractor circuit. Each subcircuit of the tripler will be discussed next in detail.

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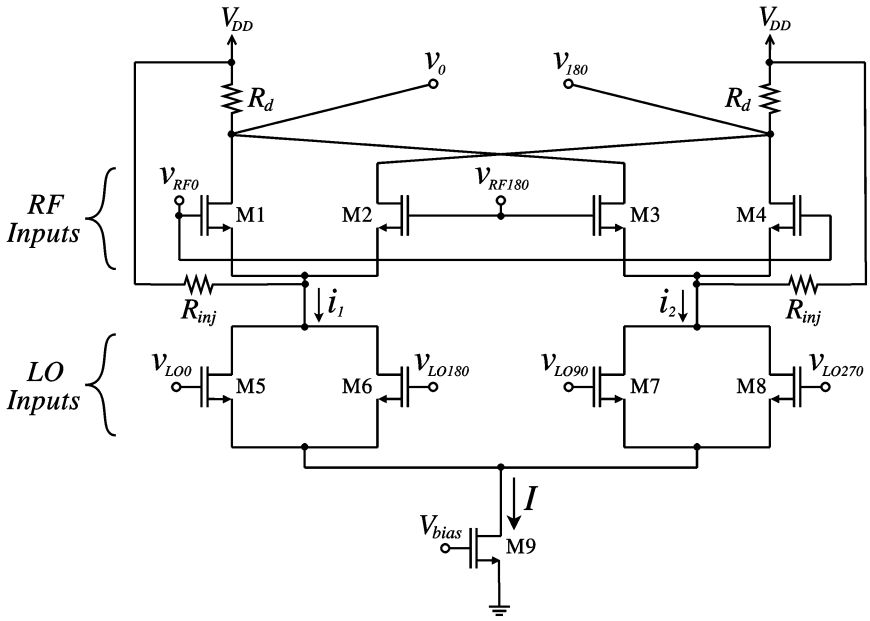

Fig. 2. SHM core.

A. SHM

The schematic of the SHM is shown in Fig. 2. This SHM uses a topology similar to the ones discussed in [14]–[16] with the RF and LO ports exchanged from the traditional Gilbert cell. There are two pairs of local oscillator (LO) switching transistors with 0° and 180° inputs and 90° and 270° inputs. These pairs of switching transistors generate the second harmonic of the LO that enables subharmonic mixing. The mixer also uses injection resistors $R_{\rm inj}$ connected between V_{DD} and the sources of the RF transistors (drains of the LO transistors). As discussed in [17], this injection method can increase the conversion gain of the mixer. Most of the dc-bias current in the mixer flows through the injection resistors, which permits a larger bias current for the LO transistors and generates a larger second harmonic signal current. Since $R_{\rm inj}$ is large, the RF current flows primarily into transistors $M1$–$M4$. An increased conversion gain can be achieved by using this technique since much larger drain resistors R_d can be used for the same LO transistor bias current.

The generation of the quadrature LO signals was accomplished with RC–CR phase shifters, as shown in Fig. 3 (R_1 and C_1). Of course, if the fundamental signal is generated by a quadrature oscillator, then the RC–CR phase shifters would not be required and the outputs of oscillator could be connected directly to the LO transistors $M5$ to $M8$. In order to increase the LO drive of the SHM, and counteract the loss in the RC–CR phase shifters, two inverter amplifiers were used before the phase shifters, as shown in Fig. 3. The overall voltage gain of the quadrature generation circuit was approximately 3 dB. The LO inputs to the SHM are given by

$$v_{\rm LO0} = A_{\rm LO}\cos(\omega_{\rm in}t)$$
$$v_{\rm LO90} = A_{\rm LO}\cos\left(\omega_{\rm in}t - \frac{\pi}{2}\right)$$
$$v_{\rm LO180} = A_{\rm LO}\cos(\omega_{\rm in}t - \pi)$$

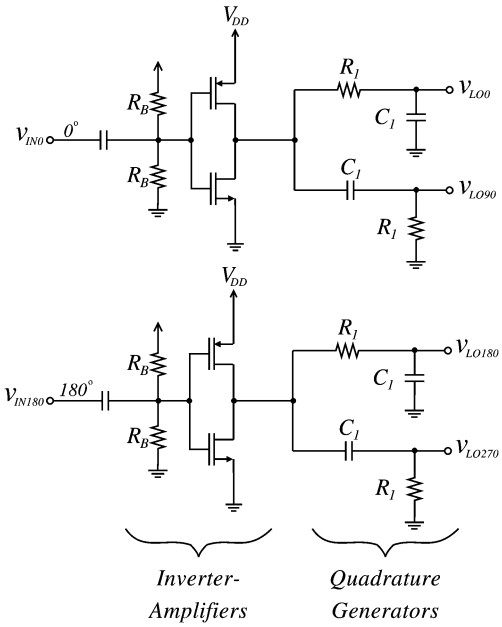

Fig. 3. Generation of the quadrature LO signals.

$$v_{\rm LO270} = A_{\rm LO}\cos\left(\omega_{\rm in}t - \frac{3\pi}{2}\right).$$

The input differential signal was connected to the RF port of the SHM without any amplification. These RF inputs are

$$v_{\rm RF0} = A_{\rm RF}\cos(\omega_{\rm in}t)$$
$$v_{\rm RF180} = A_{\rm RF}\cos(\omega_{\rm in}t - \pi).$$

Since this is a 2× SHM, the up- and down-converted components of the mixer output will be at $2f_{\rm in} \pm f_{\rm in}$ or $3f_{\rm in}$ and $f_{\rm in}$, respectively.

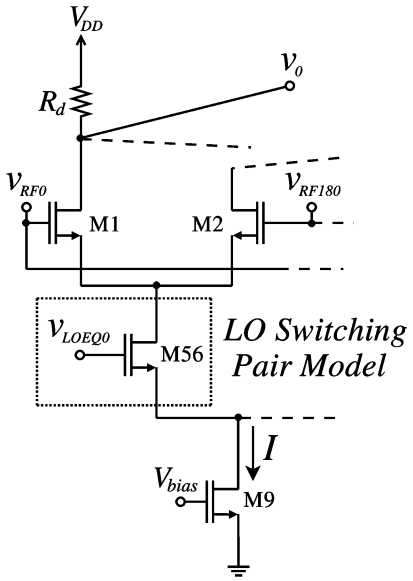

Fig. 4. Modeling of the LO switching transistors as one FET with input v_{LOEQ0}.

To gain deeper insight into the operation of the SHM, an analytic expression for the conversion gain of the mixer will be derived. The long-channel transistor model was used for simplicity. In the half-SHM circuit shown in Fig. 4, the LO switching pair transistors $M5$–$M6$ are modeled as one transistor, $M56$. Assuming that the fundamental currents generated by the differential gate voltage signals on $M5$ and $M6$ perfectly cancel each other, the nonlinear component at twice the input frequency is the only signal current that remains. Therefore, $M5$ and $M6$ are modeled as one transistor with an applied gate voltage signal at a frequency of $2\omega_{\mathrm{in}}$. This approach is similar to the modeling used in [18]. Transistors $M7$ and $M8$ in Fig. 2 can also be replaced by a single equivalent transistor $M78$.

If the currents through $M5$ and $M6$ are i_a and i_b, respectively, the total current from the switching pair with a differential input is

$$\begin{aligned} i_1 &= i_a + i_b \\ &= \mu_n C_{\mathrm{ox}} \frac{W_1}{L}(V_{\mathrm{GS(LO)}} - V_t)^2 \\ &\quad + \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W_1}{L}\left(v_{\mathrm{LO0}}^2 + v_{\mathrm{LO180}}^2\right) \end{aligned} \tag{1}$$

where $V_{\mathrm{GS(LO)}}$ is the dc voltage between the gates and sources of the LO transistors ($M5$–$M8$). Since $v_{\mathrm{LO0}}^2 = v_{\mathrm{LO180}}^2$,

$$i_1 = \mu_n C_{\mathrm{ox}} \frac{W_1}{L}(V_{\mathrm{GS(LO)}} - V_t)^2 + \mu_n C_{\mathrm{ox}} \frac{W_1}{L} v_{\mathrm{LO0}}^2. \tag{2}$$

This current can then be set equal to the current generated by the $M56$ model transistor (ignoring the nonlinear component)

$$\begin{aligned} i_1 = \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W_2}{L}(V_{\mathrm{GS(LO)}} - V_t)^2 \\ + \mu_n C_{\mathrm{ox}} \frac{W_2}{L}(V_{\mathrm{GS(LO)}} - V_t) v_{\mathrm{LOEQ0}}. \end{aligned} \tag{3}$$

Clearly, in order to have equal dc currents, the width of transistor $M56$ must be twice that of $M5$ and $M6$, $W_2 = 2W_1$. The equivalent applied gate signal voltages to the LO switching pair model transistors $M56$ and $M78$ are

$$\begin{aligned} v_{\mathrm{LOEQ0}} &= \frac{A_{\mathrm{LO}}^2}{2(V_{\mathrm{GS(LO)}} - V_t)} \cos^2(\omega_{\mathrm{in}} t) \\ &\approx \frac{A_{\mathrm{LO}}^2}{4(V_{\mathrm{GS(LO)}} - V_t)} \cos(2\omega_{\mathrm{in}} t) \end{aligned} \tag{4}$$

$$\begin{aligned} v_{\mathrm{LOEQ180}} &= \frac{A_{\mathrm{LO}}^2}{2(V_{\mathrm{GS(LO)}} - V_t)} \cos^2(\omega_{\mathrm{in}} t + \pi) \\ &\approx \frac{A_{\mathrm{LO}}^2}{4(V_{\mathrm{GS(LO)}} - V_t)} \cos(2\omega_{\mathrm{in}} t + \pi). \end{aligned} \tag{5}$$

The approximation made in (4) and (5) was to ignore the dc component of the $\cos^2$ term, the effect of which will be discussed below. With this simplification, the circuit can be analyzed as a standard Gilbert-cell topology with the addition of the injection resistors. The output voltage of the mixer $v_{\mathrm{OUT}} = v_0 - v_{180}$, as defined in Fig. 2, is given by

$$\begin{aligned} v_{\mathrm{OUT}} &= \frac{-R_d v_{\mathrm{idRF}}}{V_{\mathrm{GS(RF)}} - V_t}(i_1 - i_2) \\ &= \frac{-R_d I}{(V_{\mathrm{GS(RF)}} - V_t)(V_{\mathrm{GS(LO)}} - V_t)} v_{\mathrm{idRF}} v_{\mathrm{idLOEQ}} \end{aligned} \tag{6}$$

where $v_{\mathrm{idRF}} = v_{\mathrm{RF0}} - v_{\mathrm{RF180}}$, $v_{\mathrm{idLOEQ}} = v_{\mathrm{LOEQ0}} - v_{\mathrm{LOEQ180}}$, and $V_{\mathrm{GS(RF)}}$ is the dc voltage between the gates and sources of the RF transistors ($M1$–$M4$).

The conversion gain formula for this SHM for the up- and down-converted components ($3f_{\mathrm{in}}$ and f_{in}), including the effects of the injection resistors, is given by

$$CG_{\mathrm{dB}} = 20 \log\left(\frac{R_d I A_{\mathrm{LO}}^2}{4(V_{\mathrm{GS(RF)}} - V_t)(V_{\mathrm{GS(LO)}} - V_t)^2}\right) \tag{7}$$

where I is the bias current set by the gate voltage of transistor $M9$, A_{LO} is the amplitude of the quadrature signal at the gates of the LO transistors $M5$–$M8$, and all transistors are operating in the saturation region. The values for $V_{\mathrm{GS(RF)}}$ and $V_{\mathrm{GS(LO)}}$ can be found from a straightforward dc circuit analysis. From this equation, it is clear that the conversion gain will increase with increasing bias current I. Without the injection resistors, the bias current flowing through each drain resistor would be $I/2$, and R_d would be limited to values that maintain the saturation region for all FETs. However, since most of the dc current flows through the injection resistors, the bias current can be increased to improve the conversion gain while simultaneously having a large R_d.

The formula for the conversion gain in (7) does not include the effects of any parasitics, and thus, will overestimate the actual conversion gain. However, the simplification in (4) and (5) where the dc component of the $\cos^2$ term was not included mitigates the overestimation in (7) somewhat since there is an additional dc component in the currents that are generated by $M5$–$M8$ (or $M56$ and $M78$). The SHM was independently simulated and compared to the conversion gain given by (7) using a CMOS 0.18-μm process with $V_{DD} = 2.0$ V. Shown in Fig. 5 are the analytic [using (7)] and the simulated conversion gains at various LO voltage amplitudes A_{LO} for an input

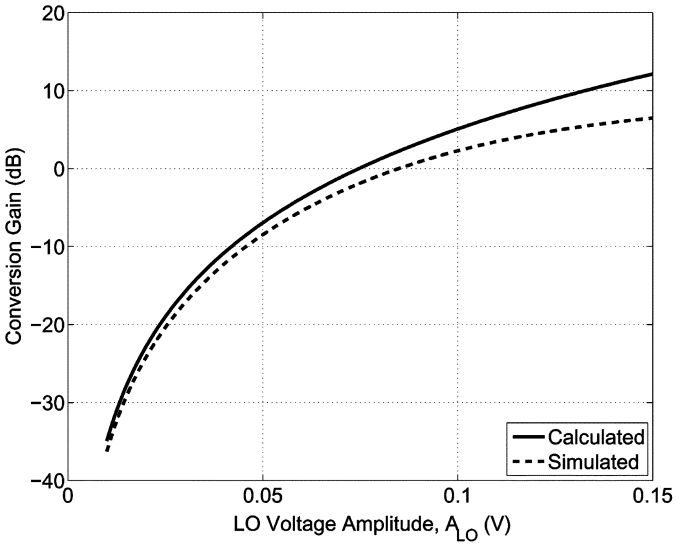

Fig. 5. Calculated and simulated conversion gain of the SHM at various LO voltage amplitudes $A_{\rm LO}$.

frequency of 1.0 GHz, which produces an upconverted component at 3.0 GHz. The calculated and simulated values are within 3 dB of each other up to LO voltage amplitudes of 0.1 V. At higher amplitudes, the transistors become saturated, which explains the increasing difference between the two. In this study, the operational range for the tripler has $A_{\rm LO} < 0.15$ V so the equation given in (7) can provide a useful first-order approximation for the conversion gain of the SHM.

Due to parasitics, the amplitude of the output signals at $f_{\rm in}$ and $3f_{\rm in}$ will not be equal with the $3f_{\rm in}$ component obviously being slightly lower. In this study, the SHM was designed to provide a conversion gain of approximately 3 dB for the SHM output signal at $3f_{\rm in}$. For the signal component at $f_{\rm in}$, the conversion gain was about 4 dB.

B. Fundamental Feedforward Circuit

As shown in the block diagram in Fig. 1, a feedforward technique is used along with a subtraction circuit to suppress the fundamental tone that is present at the output of the SHM. In order to have significant cancellation of the fundamental tone at the output of the tripler, the input signals into the subtraction circuit must have very similar amplitudes and phases. Therefore, the fundamental feedforward circuit has to match the amplitude and phase of the fundamental tone at the output of the SHM. To this end, a phase shifter circuit is used, followed by an amplifier, as shown in Fig. 6.

Only one of the two input differential signals was used for the feedforward circuit $(v_{\rm IN180})$, while the other input $(v_{\rm IN0})$ was terminated in an impedance closely matching the input impedance of the feedforward circuit to maintain equal amplitude input voltage signals to the rest of the circuit.

To implement the phase shifter, an R–C network was used (R_2 and C_2 in Fig. 6). A varactor was used for C_2 so that the phase shifter could be tuned for optimal fundamental cancellation. An inverter amplifier was used after the phase shifter and its gain was designed to be slightly larger than the conversion

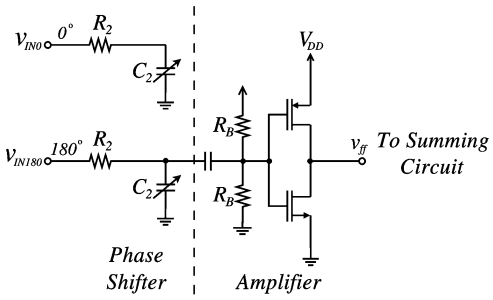

Fig. 6. Fundamental feedforward circuit.

gain of the SHM to account for the losses in the phase shifter. The output of the feedforward circuit is given by

$$v_{\rm ff} = \frac{-A_{\rm ff} v_{\rm IN180}}{1 + j\omega_{\rm in} C_2 R_2} \tag{8}$$

where $A_{\rm ff}$ is the gain of the feedforward amplifier. This output signal $v_{\rm ff}$ is then used as one of the inputs to the subtractor circuit that cancels the fundamental frequency signal present in the SHM output.

C. Fundamental Cancellation Circuit

The schematic of the circuit used at the output of the SHM to suppress the fundamental is shown in Fig. 7. An active balun, simply implemented as a differential pair with a single-ended output, is used to convert the differential output of the SHM to single ended. Any signals that are in the common mode at the output of the SHM will be suppressed due to the inherent signal subtraction that occurs in this differential pair active balun. Next, the single-ended active balun output $v_{\rm SHM}$ is used as the second input to another differential pair that is used for the subtraction circuit. The other input to the subtraction circuit is the output of the feedforward circuit $v_{\rm ff}$, shown in Fig. 6, and as discussed in Section II-B. The down- and up-converted components of the SHM output are given by

$$v_{\rm SHM} = A_1 \cos(\omega_{\rm in} t + \phi_1) + A_2 \cos(3\omega_{\rm in} t + \phi_2) \tag{9}$$

and the feedforward input to the subtraction circuit is given by

$$v_{\rm ff} = A_3(\cos(\omega_{\rm in} t + \phi_3)). \tag{10}$$

Whereas the phase of the feedforward signal is controlled by the phase shifter in the feedforward circuit, the amplitude of the feedforward signal is controlled by the gate bias of the subtractor differential pair (V_{S1} and V_{S2}). By adjusting these gate bias voltages, the amplitudes of the fundamental frequency components in the signal currents $i_{\rm SHM}$ and $i_{\rm ff}$ can be made equal for maximum cancellation.

Shown in Fig. 8 is a calculation of the amount of fundamental tone cancellation at the output that occurs for various amplitude and phase mismatches assuming an ideal differential pair subtractor circuit. The phase difference on the figure is given by $\Delta\phi = \phi_1 - \phi_3$, and the amplitude match is quantified as $\alpha = i_{\rm ff}/i_{\rm SHM}$ (the currents generated by $v_{\rm ff}$ and $v_{\rm SHM}$, as labeled in Fig. 7). The ideal case where $\Delta\phi = 0^\circ$ and $\alpha = 1$ provides a complete elimination of the fundamental, as shown

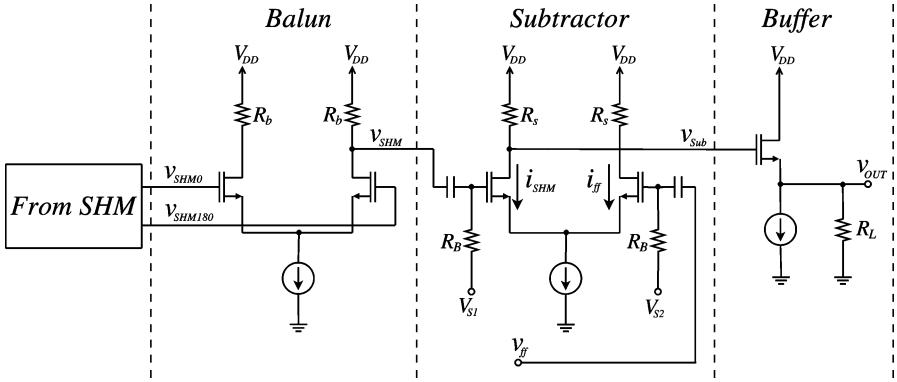

Fig. 7. Simplified schematic of the active balun, subtractor, and output buffer circuits.

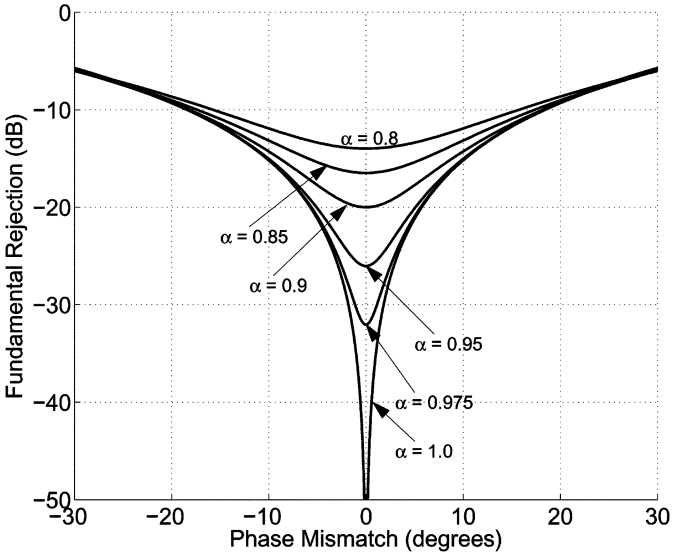

Fig. 8. Fundamental suppression at various subtractor phase and amplitude matches.

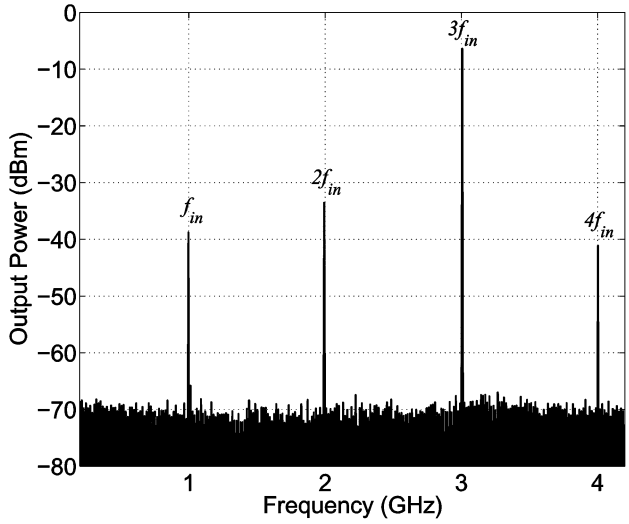

Fig. 9. Typical output spectrum with −10-dBm input power at 1 GHz.

in this figure. In order to obtain a fundamental suppression of 30 dB or more, $0.97 \leq \alpha \leq 1.03$ and $|\Delta\phi| < 2^\circ$.

The output of the subtractor circuit, $V_{\rm Sub}$, is connected to a source follower buffer to drive the external 50-Ω load. The output voltage $v_{\rm OUT}$ of the tripler at $3\omega_{\rm in}$ is given by

$$v_{\rm OUT} = A_{\rm Buf} A_{\rm Sub}(v_{\rm SHM} - v_{\rm ff}) \tag{11}$$

where $A_{\rm Sub}$ is the gain of the subtractor and $A_{\rm Buf}$ is the gain of the buffer. The overall gain of the cascaded balun, subtractor, and buffer circuits was designed to be approximately one, and therefore, the gain of the SHM determines the conversion gain of the frequency tripler. In other words, the third harmonic signal amplitude at the SHM output $v_{\rm SHM0} - v_{\rm SHM180}$ is equal to the third harmonic voltage amplitude at the output $v_{\rm OUT}$.

III. Experimental Results

To demonstrate the validity of this tripler concept, a 1.0–3.0-GHz multiplier was designed and fabricated. The input signal was differential and the output spectrum was measured using a spectrum analyzer. A typical plot of the output power spectrum is shown in Fig. 9 for an input power of −10 dBm. From this figure, the output power of the third harmonic is approximately −7 dBm, which is a 3-dB gain, and the fundamental is suppressed by more than 30 dB. The second harmonic in Fig. 9 is approximately 26 dB below the third harmonic, and the fourth (and all higher order harmonics) are more than 30 dB below the desired tripled frequency output. Note that these high levels of suppression are achieved without any filtering (on or off chip), and without the use of any inductors.

Fig. 10 shows the output powers of the fundamental, second harmonic, and third harmonic at various input power levels. At low input power levels, the LO signals are not large enough for the switching pairs in the SHM to generate a strong double-frequency signal, and therefore there is a low third-order output power. However, at about −16 dBm input power, the SHM is in full operational mode. From −16- to −10-dBm input power the tripler is in its linear range. The slope of this line is slightly greater than one since the LO power is increasing simultaneously with the RF signal. A peak conversion gain of approximately 3 dB is obtained at an input power level of −10 dBm. The power of the fundamental at the output is below the third harmonic at input powers above −17 dBm with significant rejection (greater than 10 dB) between −15- and −8-dBm input

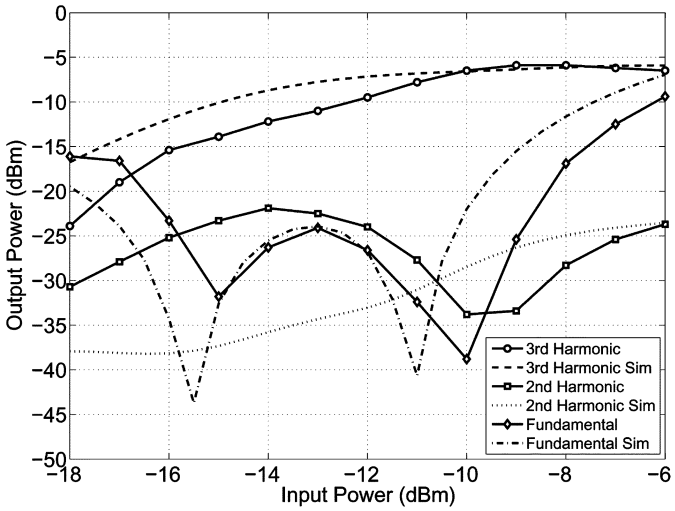

Fig. 10. Measured and simulated output power at various input power levels.

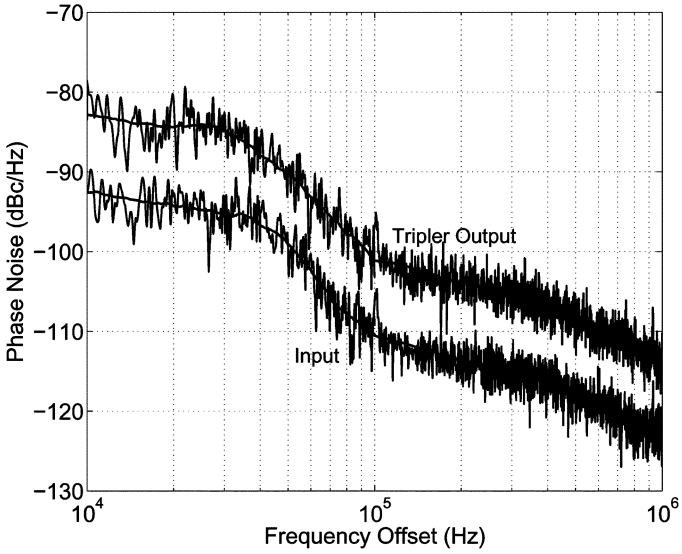

Fig. 12. Measured input and output phase noise.

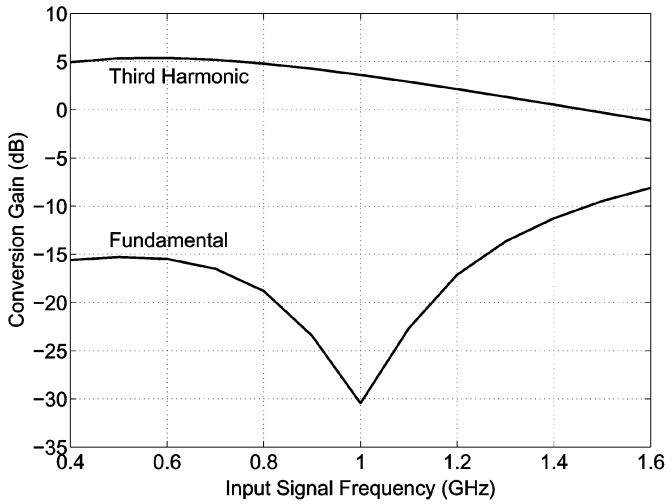

Fig. 11. Simulated broadband performance of the tripler using an ideal quadrature input signal with a power of −11 dBm.

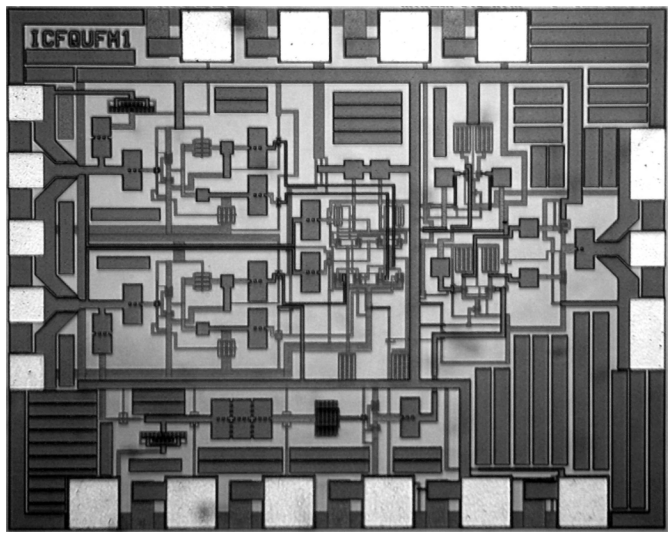

Fig. 13. Microphotograph of the proposed frequency tripler chip.

power. At an input power of −10 dBm, there is a very large fundamental suppression of 30 dB. At this point, the input signals to the summer circuit are very closely matched (see Fig. 8). The reason for the optimal match at certain input power level is due to the various leakage fundamental signals that degrade the amplitude and phase match at other power levels. The second harmonic in Fig. 10 is below the third-order signal by −10 dB or more for input powers above −16 dBm. The second harmonic signal at the output is due predominately to the nonlinear distortion in the active balun at the output of the SHM since the fundamental signal components at the gates of the differential pair are strong. The simulation results shown in this figure are similar to the experimental for the fundamental and third-order harmonic output power levels, but noticeably differs in the second harmonic response at low power levels. The difference in the measured and simulated results for the second harmonic could be due to leakage of this signal through the substrate to other circuits (e.g., the second-harmonic distortion generated from the strong fundamental signal at the balun could leak to the input of the feedforward amplifier) and/or possibly limitations of the nonlinear FET model that was used for simulations.

Measurements were made at only one input frequency, i.e., 1.0 GHz, due to the quadrature generator RC–CR phase shifter for the SHM that works optimally at only this frequency. However, there is not an inherent narrowband frequency limitation with the proposed frequency multiplier topology. In fact, if a quadrature VCO was used for the input signal then the multiplier circuit would work over a wide bandwidth, with the only potential bandwidth restriction being from the tuning range of the feedforward phase shifter. To evaluate the performance of the proposed tripler circuit over a range of input frequencies without the limitation of the RC–CR phase shift network, a simulation was performed using an ideal broadband quadrature input signal with −11-dBm input power. The results, shown in Fig. 11, indicate that without the limitation of the phase shifter, the circuit achieves a conversion gain and a fundamental suppression of

TABLE I
COMPARISON OF SEVERAL RECENT FREQUENCY TRIPLERS WITH THIS STUDY

Reference	Technology	Input Frequency (GHz)	Conversion Gain (dB)	Fundamental Suppression (dB)	DC Power (mW)	Area (mm^2)
[8]	GaAs (Hybrid)	1	−5.7	62.7	–	∼7000
[9]	InGaAs PHEMT	12	−9.4	22.3	18.9	5.0
[11]	CMOS 0.18 μm	8.8	−10.9	22.7	0.45	0.46
[11]	CMOS 0.13 μm	20.0	−11.2	–	1.86	0.39
[12]	CMOS 90 nm	20	–	–	23.8	0.81
[13]	CMOS 0.18 μm	2	−5.6	13	27	0.18
This Work	CMOS 0.18 μm	1	3	30	68	0.8

over 10 dB for input signals from 400 MHz to 1.4 GHz without tuning the feedforward circuit. The phase noise degradation of the tripler was measured and the results are shown in Fig. 12 for offset frequencies from 10 kHz to 1 MHz. From theory, the minimum phase noise degradation in a frequency multiplier is given by $20\log(n)$, where n is the order of multiplication. For the case of a frequency tripler, the minimum phase noise degradation is 9.54 dB relative to the input signal phase noise. For this circuit, the average measured phase noise degradation from 10 kHz to 1 MHz is 9.69 dB, which is quite close to the theoretical minimum.

The supply voltage of the circuit was set to 2.0 V and the dc current consumed was 34 mA, resulting in a power consumption of 68 mW. A microphotograph of the chip is shown in Fig. 13. The dimensions of the chip including bonding pads was 1.0 mm × 0.8 mm (0.8 mm^2). A performance comparison of several recent monolithic microwave integrated circuit (MMIC) frequency triplers with this work is presented in Table I, which shows that the proposed tripler method has advantages in terms of conversion gain and fundamental suppression.

IV. CONCLUSION

A new topology for a frequency tripler circuit has been demonstrated in this study. This technique uses a 2× SHM along with a feedforward circuit and a subtraction circuit to realize fundamental cancellation. An input signal with frequency $f_{\rm in}$ is converted to $f_{\rm in}$ and $3f_{\rm in}$ at the output of the SHM $(2f_{\rm in} \pm f_{\rm in})$. A feedforward circuit is used for the input signal at $f_{\rm in}$ and is connected to a summing junction along with the output of the SHM. In the summing junction, the fundamental frequency signals $f_{\rm in}$ in both the SHM output and the feedforward circuit output are cancelled, ideally leaving only the third harmonic $3f_{\rm in}$. Advantages of this technique include the ability to realize very high levels of fundamental suppression without the use of a filter (up to 30 dB was obtained in this study), as well the ability to obtain conversion gain (up to 3 dB was shown in this study). Since no filters or inductors are required, this circuit can be implemented entirely on chip in a relatively small area. While the demonstration circuit was at S-band, this technique could be used at much higher frequencies (e.g., millimeter wave) where the use of frequency multiplication circuits may be required. If the proposed frequency tripler topology is implemented at a higher frequency, it may be possible to use a passive feedforward phase shifter and/or a passive subtractor circuit on-chip, which would reduce the power consumption of the circuit.

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