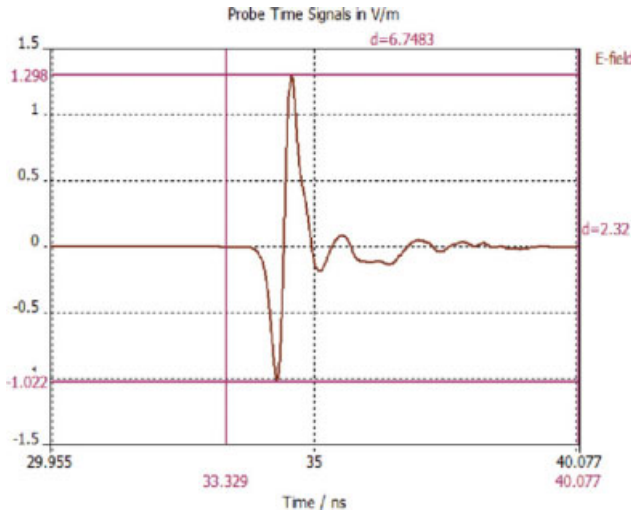

Figure 6 The waveform is tested in the far field of CST. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

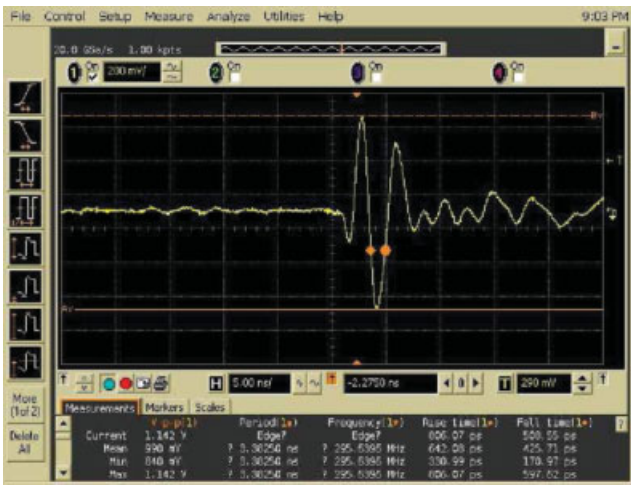

Figure 7 The waveform is tested in the far field of experiment. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

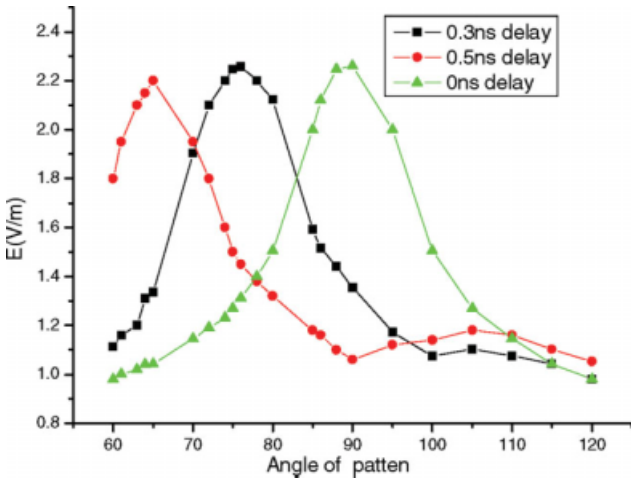

Figure 8 The directivity pattern that delay time of 2-unit antennas is set as 0, 0.3, and 0.5 ns. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

actual orientation angle after delay is 90°, 75.5°, and 65°, which agrees well with theoretical calculation results. This shows that UWB time-domain antenna array scanning can achieve by precise delay of fiber delay line.

5. CONCLUSIONS

The transmission system of UWB impulse radar comprises delay controller, pulse source, and transmitting antenna array. UWB time-domain antenna array scanning is realized by UWB time-domain antenna array and delay controller, which is most promising, such as in the applications of detecting moving-target and tracking UWB impulse radar.

ACKNOWLEDGMENT

This work was supported in part by the state key laboratory funds of China and defense innovation and technology fund of China.

REFERENCES

1. C.L. Ruan, Ultra-wideband antenna theory and technology, Haerbin, China, 2006, pp. 52–55.
2. A.B. Suksmono and A. Hirose, Ultra-wideband beamforming by using a complex-valued spatio-temporal neural network, ICONIP 2004, LNCS 3316 (2004), 104–109.
3. M.G.M. Hussain, Cylindrical array beamforming based on ultra-wideband signals, IEEE International Radar Conference, 2005, pp. 618–622.
4. G.S. Smith, A note on the criteria for the far zone in the time-domain analysis of antennas, IEEE Trans Antenna Propag 54 (2006), 292–297.
5. C.L. Ruan, The conspectus of electromagnetic missile, Publishing company of demos-postoffice in Beijing, China, 1994, pp. 3–6.
6. T. Sakamoto and T. Sato, A fast algorithm of 3-dimensional imaging for pulse radar systems, IEEE AP-S Int Symp USNC/URSI National Radio Sci Meeting 3 (2004), 2099–2102.
7. W. Sirgel, C. Waldschmidt, and W. Wiesheck, Transient responses of a vivaldi antenna and a logarithmic periodic dipole array for ultra wideband communication, IEEE Antennas Propag Soc Int Symp 3 (2003), 592–595.
8. X.H. Wu, A.A. Kishk, and Z.N. Chen, A linear antenna array for UWB applications, IEEE Antennas Propag Soc Int Symp 1A (2005), 594–597.

A VARIABLE GAIN AMPLIFIER USING A VERY-HIGH SPEED OTA

You Zheng and Carlos E. Saavedra
Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada K7L 3N6; Corresponding author: carlos.saavedra@queensu.ca

Received 14 July 2009

ABSTRACT: *A variable gain amplifier is demonstrated using only one fully-differential operational transconductance amplifier (OTA) as the core circuit element. Gain control is achieved by varying the transconductance of the OTA and by using an output buffer circuit to sum the output signals of the OTA in the correct phase relationship. The circuit was designed and fabricated using 0.18 μm CMOS technology. Measured results show a gain control range of 15 dB between 1 GHz*

and 3 GHz and the input and output reflection coefficients are below −10 dB and −20 dB, respectively. The output power of the amplifier is +2.3 dBm at its 1-dB compression point. The chip has a maximum DC power consumption 12.6 mW and it measures 0.25 mm² including bonding pads. © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52: 1112–1116, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25114

Key words: *variable gain amplifier; automatic gain control; OTA; feedback amplifier*

1. INTRODUCTION

An abundant number of variable gain amplifier (VGA) circuit designs exist and more continue to be developed on a regular basis. The majority of these circuits typically rely on four broad design methods. One method is to use a fixed-gain amplifier in conjunction with a variable attenuator circuit. This approach is often used at very high frequencies due to its simplicity [1]. A second method is to also use a fixed-gain stage but with a variable output load, often called a degeneration resistance [2–4]. The third method involves using a feedback amplifier with an adaptive feedback network (e.g., a variable resistor) to control the VGA gain [5]. Either a voltage amplifier or an operational transconductance amplifier (OTA) can be used in this approach. The fourth common method is to vary the gain of the VGA by changing the transconductance, G_m, of an OTA through its DC bias current [6–8].

In this article, we demonstrate a VGA that relies on a combination of the latter two approaches: it consists of an OTA with a static feedback network and gain control is achieved by varying the G_m of the OTA. An input active balun feeds the OTA with differential signals and an output buffer circuit serves to combine the output waveforms of the OTA into a single-ended signal in the correct phase relationship. These two interface circuits have the added benefit of providing a nearly constant input and output impedance at the VGA ports, leading to a very good impedance match over a broadband. While many VGA's that rely on OTA's rarely reach 1 GHz in operating frequency [4], the VGA in this work can function up to 3 GHz by using a very high-speed feedforward-regulated cascode OTA. The circuit uses only one OTA, leading to a very compact chip measuring only 0.25 mm^2 including pads.

2. VARIABLE GAIN AMPLIFIER CIRCUIT

A schematic of the proposed VGA is shown in Figure 1. It consists of three stages: an active balun, an OTA with feedback, and a final output stage. The active balun converts the single-ended input signal, v_{in}, into a pair of differential signals, v_{i+} and v_{i-}, which are fed to the differential OTA through two bypass capacitors (C_3 and C_4). The OTA stage is configured as a negative feedback amplifier using two identical feedback impedances, $Z_f = R_6 + 1/j\omega C_5$. The overall gain of the VGA is varied by changing the gain of the feedback amplifier through the OTA transconductance. Since the OTA amplifier produces differential output signals (v_{o+} and v_{o-}) these waveforms are converted into a single-ended signal by using an output stage. The resistors R_8–R_{10} in this stage are very large, and they are used for DC biasing purposes. The output stage has a common-drain transistor T_3 which yields an output signal at its source terminal that is in-phase with v_{o+}. Transistor T_4 is a common-source device which adds a 180° phase shift to its input signal, v_{o-}. Since v_{o-} is originally out-of-phase with respect to v_{o+}, the additional 180° phase shift puts these two signals in-phase and they are thus power-combined at the output.

The active balun has a common-gate/common-source (CG-CS) topology, and it was chosen for its compact size and wideband performance. Its design is well understood and further details can be found in various references such as [9].

The OTA cell used in this work employs a feedforward-regulated cascode topology, and the schematic is shown in Figure 2. The DC bias voltages to all the transistor gates in the OTA are applied through a set of very large resistors, R_{11}–R_{14}, and capacitors C_{10} and C_{11} are used for DC isolation between the cascode transistors. The OTA uses a PMOS current mirror arrangement consisting of transistors T_9–T_{11} as its DC current source.

The feedforward regulation is implemented by using a set of cross-connections between the cascode pairs (T_5–T_7 and T_6–T_8). With this procedure the gate-source voltages of the cascoding transistors, T_7 and T_8, will either increase or decrease to counteract changes in the drain voltages of T_5 and T_6 when there are large differential input signals. The result is a stabilization of the drain voltages of transistors T_5 and T_6 by creating an interlocking regulation mechanism between these two drain voltages. This OTA cell is a variant of our previous works on feedforward-regulated OTA's, which are described in detail in Refs. 10 and 11.

The gain of the feedback amplifier stage in Figure 1 can be derived by making a few simplifying assumptions: (a) that the input impedance into the OTA cell is very large and (b) that the parasitic reactances are negligible. In this manner, the gain is

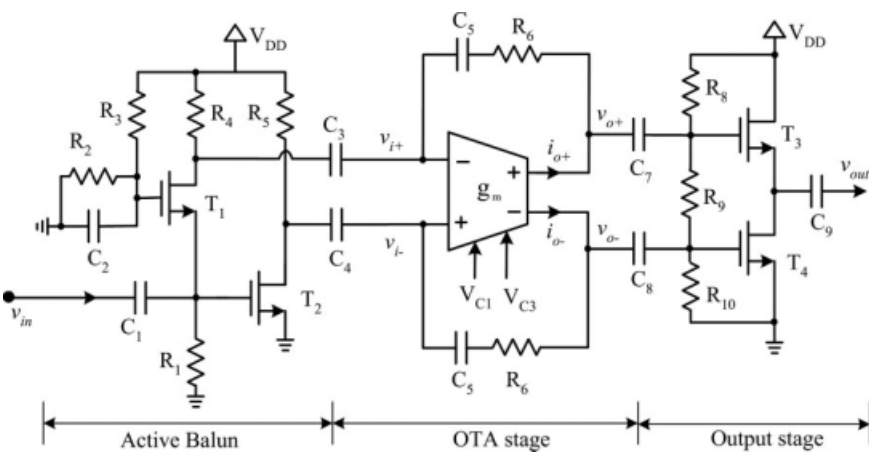

Figure 1 Variable gain amplifier schematic

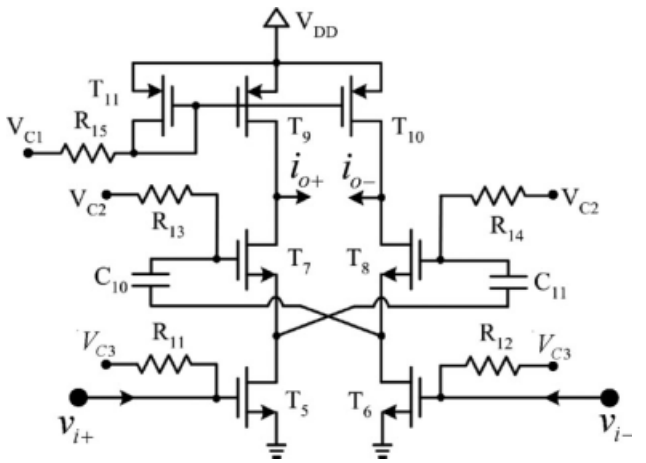

Figure 2 Feedforward-regulated cascode OTA

given by,

$$A_f(j\omega) = \frac{v_{o+} - v_{o-}}{v_{i+} - v_{i-}} = \frac{(1 - 2G_m Z_f)(R_o||Z_{L,amp})}{2Z_f + (R_o||Z_{L,amp})} \quad (1)$$

where G_m and R_o are, respectively, the transconductance and the output resistance of the OTA cell, and $Z_{L,amp}$ represents the load impedance seen at the output of the feedback amplifier. This load impedance is very large since it consists of the bias resistors R_8–R_{10} and the small gate capacitances of T_3 and T_4.

By making use of the symmetry in the feedforward OTA cell in Figure 2, the transconductance and the output resistance of the OTA can be derived to be,

$$G_m = \frac{i_{o+} - i_{o-}}{v_{i+} - v_{i-}} = g_{m5}\left[\frac{\frac{1}{r_{o7}} + 2g_{m7}}{\frac{1}{r_{o5}} + \frac{1}{r_{o7}} + 2g_{m7}}\right] \quad (2)$$

and,

$$R_o = 2r_{o5} + 2r_{o7} + 4g_{m7}r_{o5}r_{o7} \quad (3)$$

where r_{o5} and r_{o7} are the small-signal output resistances of transistors T_5 and T_7, respectively, and g_{m5} and g_{m7} are the transconductances of those same transistors. Since r_{o5} and r_{o7} are each several kΩ in size and because the NMOS transconductance, g_{m7}, in this work is larger than a few mS then $2g_{m7} \gg \frac{1}{r_{o5}} + \frac{1}{r_{o7}}$, and we can conclude from Eq. (2) that,

$$G_m \approx g_{m5} \quad (4)$$

which is in agreement with the well-known expression for the transconductance of a cascode amplifier [12].

From the previous discussion and from Eq. (3) it is clear that R_o has a very large value and since $Z_{L,amp}$ is also very large compared to $2Z_f$, then the equation for the gain of the feedback amplifier described by Eq. (1) can be approximated as,

$$A_f(j\omega) \approx 1 - 2G_m Z_f \approx 1 - 2g_{m5}Z_f \quad (5)$$

Given that the input balun and the output stage in Figure 1 each have about unity gain, then Eq. (5) is also the first-order expression for the overall gain of the VGA circuit. As a result, the gain of the VGA can be varied just by changing the value of g_{m5} through the gate control voltage, V_{C3}, and that is the approach taken here.

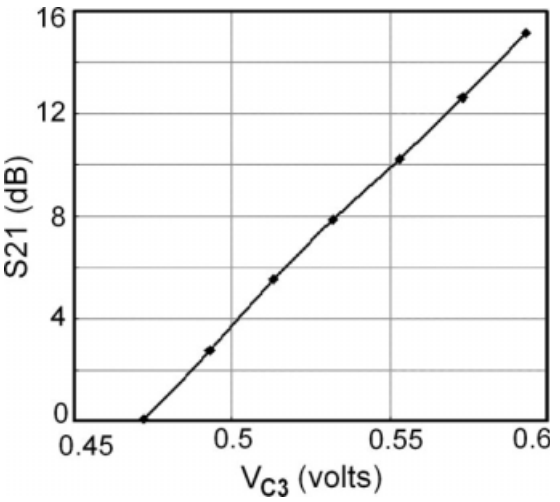

Figure 4 Gain versus control voltage at 2 GHz

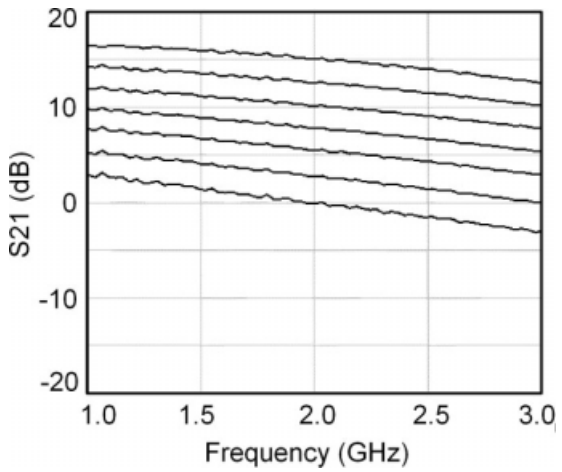

Figure 3 Measured forward gain of the VGA at different control voltages

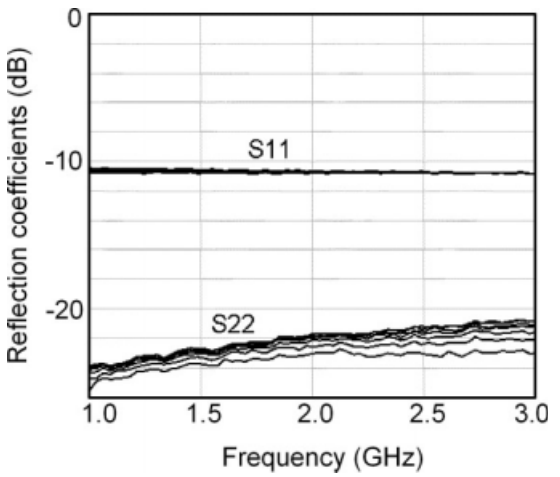

Figure 5 Measured input and output reflection coefficients

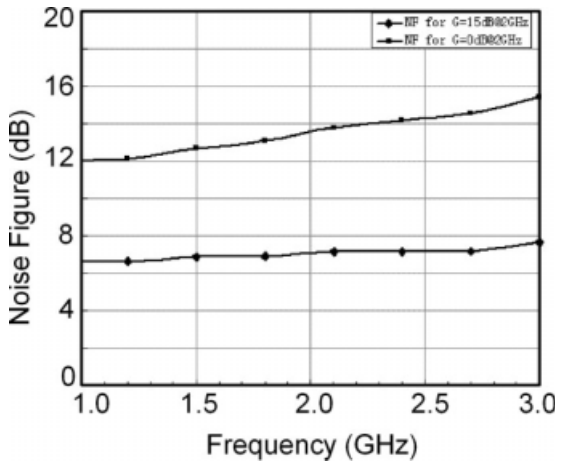

Figure 6 Measured NF at the maximum and minimum VGA gain states

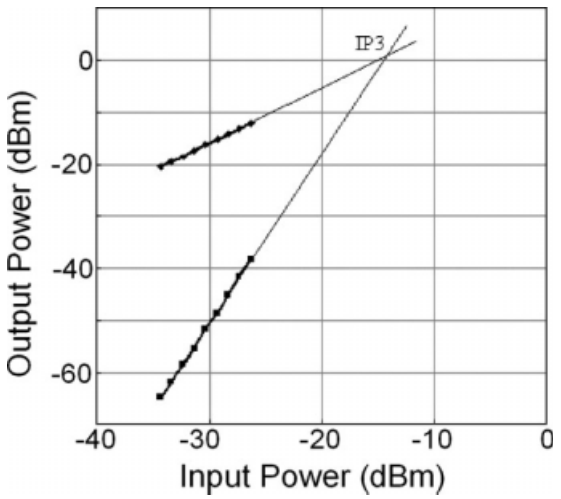

Figure 8 Third-order intermodulation distortion performance

3. EXPERIMENTAL DEMONSTRATION

The variable gain amplifier described in the previous section was fabricated using a standard 0.18 μm CMOS process. On-wafer measurements were carried out on the chip using GSG coplanar-waveguide (CPW) probes.

The s-parameters of the amplifier were measured using an Agilent 8510C vector network analyzer for different values of the gain control voltage, V_{C3}. In Figure 3, the forward gain of the VGA, S_{21}, is plotted versus frequency from 1 GHz to 3 GHz at various control voltages. The observed frequency roll-off is mainly due to the frequency response of the active balun circuit. While the active balun has a good amplitude balance between the signals at its two output ports, these output signals do exhibit a uniform roll-off nonetheless.

Figure 4 is a plot of the VGA gain versus control voltage at the center frequency of 2 GHz. The gain can be varied from 0 dB to 15 dB using a control voltage of 0.59 V for the highest gain state and a voltage of 0.475 V for the lowest gain state. The gain curve exhibits an essentially linear-in-dB versus voltage dependence and this is without the use of any special control voltage bias circuitry.

In Figure 5 the input and output reflection coefficients, S_{11} and S_{22}, are plotted from 1 GHz to 3 GHz. The S_{11} parameters are below -10 dB and the S_{22} parameters are below -20 dB for all values of the gain control voltage, V_{C3}. Both sets of reflection coefficients show only a small variation with frequency and V_{C3}. In many VGA's the reflection coefficients show a much stronger variation with frequency and specially control voltage because as the gain of the amplifier changes, its input and output impedances also change, thus leading to mismatches. In this VGA, the relative flatness of S_{11} and S_{22} is the result of using an input balun and an output stage which serve to isolate the variable-gain section from the output ports.

The noise figure (NF) of the VGA was measured versus frequency at the lowest and highest gain states, and the results are plotted in Figure 6. Normally in a VGA, the lowest noise figure is achieved at the highest gain state and conversely the worst-case noise figure occurs at the lowest gain state. For this VGA, the NF is between 6.6 dB and 7.8 dB for the high-gain state and it is between 12 dB and 15.5 dB for the low-gain state.

The output power versus input power of the VGA was measured at its highest gain state of 15 dB at the center frequency of 2 GHz. The results are shown in Figure 7. From this graph the

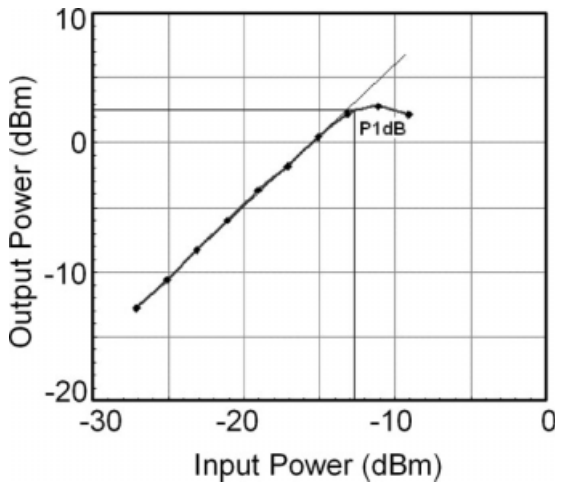

Figure 7 Measured power performance of the VGA at 2 GHz

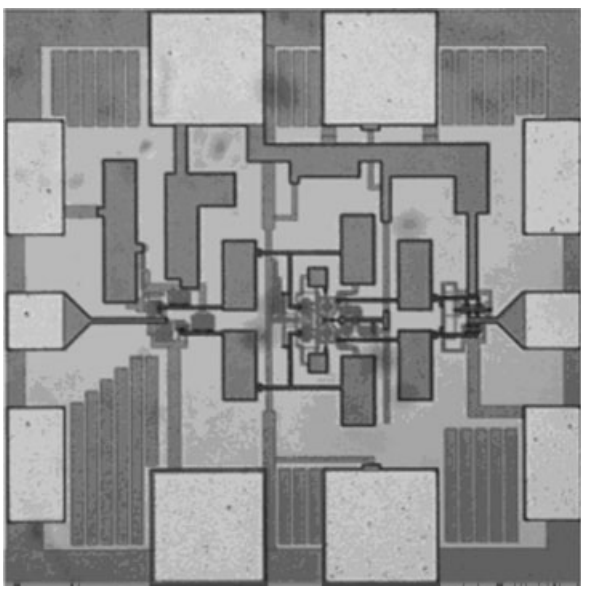

Figure 9 Microphotograph of the VGA

TABLE 1 Performance Summary Table

Min. gain at 2 GHz	0 dB
Max. gain at 2 GHz	15 dB
Frequency span	1–3 GHz
Min. NF	6.6 dB
Max. NF	15.5 dB
$P_{1dB,in}$ at 2 GHz	−12.7 dBm
DC power	8.4 mW (min)
	12.6 mW (max)
Chip area	0.25 mm^2
Technology	0.18 μm CMOS

output 1-dB compression point, P_{1dBout}, of the amplifier is determined to be +2.3 dBm at an input power of −12.7 dBm. Further measurements reveal that, as expected, the P_{1dBout} of the amplifier remains constant as the gain of the system is decreased and that the input power necessary to achieve that P_{1dBout} increases. The third-order intermodulation distortion performance of the VGA was also measured and, the results are plotted in Figure 8. The IIP3 is at about −14 dBm, which is lower than expected since the $P_{1dB,in}$ is at −12.7 dBm. One straightforward explanation for this occurrence is that the IP3 measurements were made at a different amplifier gain setting than the P_{1dB} measurements.

Figure 9 shows a microphotograph of the fabricated integrated circuit, which occupies a total area of only 0.25 mm^2 including bonding pads. With the chip supply voltage set to 2.1 V the DC power consumption of the VGA ranged from 8.4 mW in the low-gain state to 12.6 mW in the high-gain state, with the average power draw being 10.5 mW.

Table 1 shows the performance summary for this VGA.

4. CONCLUSION

In this article we have demonstrated a novel concept for a VGA that uses a single, very high-speed, fully-differential CMOS OTA as the core circuit element. Only a small amount input and output circuitry is used to interface with the OTA, and the result is a super-compact VGA measuring only 0.25 mm^2. The circuit exhibits a wide gain range with a very moderate power consumption, and it has a 100% fractional bandwdith relative to its center frequency.

REFERENCES

1. B. Lefebvre, A. Bessemoulin, H. Amara, R. Sevin, and P. Quentin, High dynamic range, triple gate-based compact DC-40 GHz variable attenuator MMIC for Ka-band variable gain amplifier ICs, In: IEEE Gallium Arsenide Integrated Circuit Symposium, San Diego, CA, 2003, pp. 135–138.
2. J.J.F. Rijns, CMOS low-distortion high-frequency variable-gain amplifier, IEEE J Solid-State Circuits 31 (1996), 1029–1034.
3. J. Xiao, I. Mehr, and J. Silva-Martinez, A high dynamic range CMOS variable gain amplifier for mobile DTV tuner, IEEE J Solid-State Circuits 42 (2007), 292–301.
4. H.D. Lee, K.A. Lee, and S. Hong, A wideband CMOS variable gain amplifier with an exponential gain control, IEEE Trans Microwave Theory Tech 55 (2007), 1363–1373.
5. K. Nishikawa and T. Tokumitsu, An MMIC low-distortion variable-gain amplifier using active feedback, IEEE Trans Microwave Theory Tech 43 (1995), 2812–2816.
6. R. Harjani, A low-power CMOS VGA for 50 MB/s disk-drive read channels, IEEE Trans Circuits Syst II Analog Digit Signal Process 42 (1995), 370–376.
7. Q. Duong, Q. Le, C. Kim, and S. Lee, A 95-dB linear low-power variable gain amplifier, IEEE Trans Circuits Syst I Regul Pap 53 (2006), 1648–1657.
8. N. Stanic, A. Balankutty, P. Kinget, and Y. Tsividis, A 0.5 V receiver in 90 nm CMOS for 2.4 GHz applications, IEEE Trans Microwave Theory Tech 43 (1995), 2812–2816.
9. C.E. Saavedra and B.R. Jackson, Voltage-variable attenuator MMIC using phase cancellation, IEE Proc Circuits Devices Syst 153 (2006), 442–446.
10. Y. Zheng and C.E. Saavedra, Feedforward-regulated cascode OTA for gigahertz applications, IEEE Trans Circuits Syst I Regul Pap 55 (2008).
11. A microwave OTA using a feedforward-regulated cascode topology, In: IEEE International Symposium on Circuits and Systems, New Orleans, 2007, pp. 1887–1890.
12. A.S. Sedra and K.C. Smith, Microelectronic circuits, 5th ed., Oxford University Press, New York, 2004.

UHF RFID NEAR FIELD READER ANTENNA FOR ITEM LEVEL APPLICATIONS

Jeong-Seok Kim, Won-Kyu Choi, and Gil-Young Choi
RFID/USN Research Group, Electronics and Telecommunications Research Institute (ETRI), 161 Gajeong-dong, Yuseong-gu, Daejon 305-700, Korea; Corresponding author: jskim0113@etri.re.kr

Received 15 July 2009

ABSTRACT: *A UHF band near-field antenna using microstrip lines and stubs for tagging stacked tags in a smart table is presented. It is shown that a suitable near-field reader antenna can be designed from signal lines, ground lines, and several stubs to generate coupled electric and magnetic fields. The proposed near-field reader antenna satisfactorily operates in a UHF radio frequency identification (RFID) smart table, and the measurements show that the antenna is capable of detecting 200 stacked tags in a reading area of 200 mm × 190 mm and achieves a detection rate of 97% when the tags are stacked in a smart table. The proposed UHF RFID smart table is successfully implemented for casino chip management.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52: 1116–1119, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25115

Key words: *RFID; reader antenna; near field*

1. INTRODUCTION

Radio frequency identification (RFID) is a rapidly developing technology for the automatic identification of objects. In contrast to RFID applications for pallet and case tracking, RFID applications at an item-level is driven by the tagging of fairly small items – retail apparel, jewelry, rented apparel/laundry, drugs, postal authorities, libraries, and so on. RFID systems for near-field communications are increasingly popular for item-level tagging since the tags can be detected more consistently on various target objects such as bottles of water, clothes, and small items [1].

The antenna, including the reading zone of a reader antenna, is one of the key factors for RFID systems. A patch antenna array for an RFID reader was designed to cover the whole belt width for a bottom conveyor reader in the RFID sortation of an item-level tagging application [2]. Besides retail applications, a smart shelf or smart table is expected to be applied in libraries, pharmacies, restaurants, and offices to manage small items. An