Full 360° Vector-Sum Phase-Shifter for Microwave System Applications

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***Abstract*—An innovative vector-sum phase shifter with a full 360° variable phase-shift range is proposed and experimentally demonstrated in this paper. It employs an active balun and a very high-speed CMOS operational transconductance amplifier (OTA) integrator to generate the four quadrature basis vector signals. The fabricated chip operates in the 2–3 GHz, it exhibits an average insertion gain of 1.5 dB at midband, and has an RMS phase error below 5° over the measured frequency span. The chip consumes 24 mW of DC power and is highly compact, measuring only 0.38 mm^2 including bonding pads.**

***Index Terms*—Active balun, differential amplifier, integrated circuit, microwave circuits, phase shifter, quadrature generation.**

I. Introduction

THERE are various phase shifting techniques suitable for integrated circuit (IC) implementation including vector-sum networks, LC-based circuits [1]–[5], all-pass networks [6], true-time-delay circuits [7] and others [8], [9]. A key requirement in a vector-sum phase shifter is the generation of the four quadrature basis vector signals, often at 0°, 90°, 180°, and 270° but not always [10]. While generating quadrature signals on-chip using passive couplers/dividers [11] or *LC* networks [12] is often viable at high microwave or millimeter-wave frequencies, these methods are much less attractive in the lower microwave bands such as the important 2.4-GHz ISM band because the long wavelengths lead to prohibitively large passive structures on-chip. A lumped-element *RC* polyphase network is an attractive solution for quadrature-signal generation due to its small size but this must be viewed in the context of tolerating a certain amount of insertion loss.

In this paper, we present a concept for a 360° vector sum phase shifter IC which relies on a novel vector summing circuit. The four quadrature basis vectors are generated using an active balun and an OTA integrator circuit. Using an active balun to generate the 0° and 180° vectors and the integrator for the 90° and 270° vectors has the benefit of requiring a small amount of chip area and both circuits can be designed to have gain. The measured phase shifter covers the full 360° phase-shift range and it operates from 2 to 3 GHz. The IC was fabricated in 0.18-μm CMOS technology and it measures only 0.38 mm^2.

Manuscript received January 21, 2009; revised April 20, 2009. First published June 19, 2009; current version published April 09, 2010. This paper was recommended by Associate Editor S.-I. Liu.

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Digital Object Identifier 10.1109/TCSI.2009.2025851

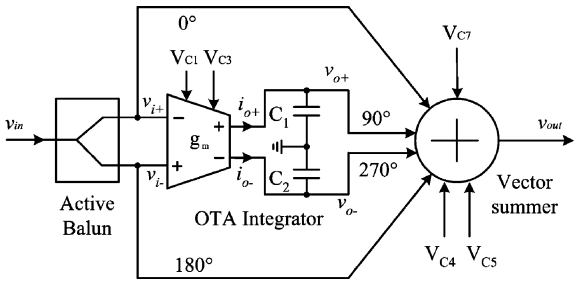

Fig. 1. Proposed 360° vector-sum phase shifter circuit.

II. Vector Phase Shifter Concept

A high-level circuit diagram of the proposed vector-sum phase shifter is illustrated in Fig. 1. A single-ended input signal, $v_{\rm in}$, enters the phase shifter at the left and four basis vectors of equal magnitude but spaced 90° apart in phase are generated using an active balun and a wideband integrator circuit. The basis vectors subsequently enter a specialized summing junction where they are added together with the correct magnitude relationships in order to generate a single output vector with the desired phase angle relative to the input signal. A set of three control voltages, $\rm V_{C4}$, $\rm V_{C5}$, and $\rm V_{C7}$ are fed to the summing junction to vary the magnitudes of the basis vectors and to select the quadrant of the output vector.

The 0° and 180° basis vectors are produced using the active balun, which is designed to have unity voltage gain. These two basis vectors are then fed to the differential OTA integrator to generate the other two basis vectors at 90° and 270°. In Fig. 1 the capacitors $\rm C_1$ and $\rm C_2$ are identical and therefore the transfer function of the integrator is given by

$$T(j\omega) = \frac{v_{o+} - v_{o-}}{v_{i+} - v_{i-}} = \frac{-2G_m R_o}{2 + j\omega R_o C_1} \tag{1}$$

where $\rm G_m$ is the transconductance of the OTA and $\rm R_o$ is its output resistance. Since $\rm R_o$ is very large (see (6), Section III) the above expression can be approximated as

$$T(j\omega) \approx j\frac{2G_m}{\omega C_1} \tag{2}$$

from which $\angle T(j\omega) = 90°$ for all frequencies, as desired. Thus, the phase angle of v_{o+} is 90° relative to the input signal, $v_{\rm in}$, while the phase of v_{o-} is $270° = -90°$ relative to the input signal. Given that all four basis vectors should have equal magnitude, it follows that we must make $|T(j\omega)| = 1$ and

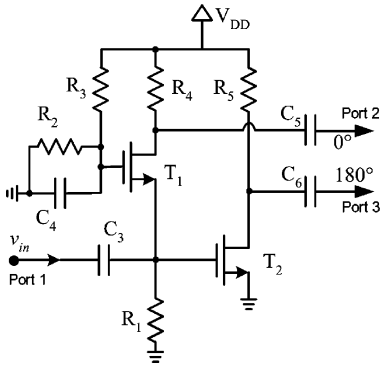

Fig. 2. Active balun circuit.

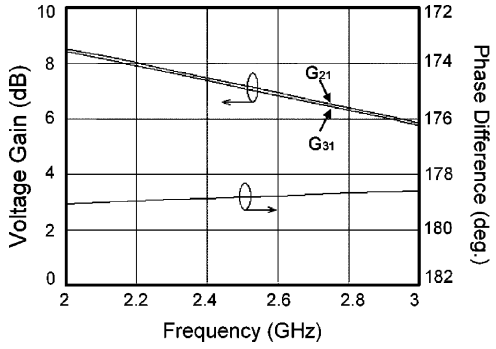

Fig. 3. Balun amplitude and phase response (simulated).

since the only free parameter in (2) is the transconductance, then $G_m = \omega C_1/2$. If the phase shifter operates at a single frequency, then G_m can be precisely set to this value. It is more likely, however, that the phase shifter will operate over a particular frequency band and then it is necessary to consider more carefully how $|T(j\omega)|$ varies with frequency.

While $|T(j\omega)|$ has a very familiar frequency dependence, it is the *rate of change* of the transfer function with frequency that is more relevant here. Taking the partial derivative with respect to frequency gives

$$\frac{\partial |T(j\omega)|}{\partial \omega} = -\frac{2G_m}{\omega^2 C_1} \tag{3}$$

and we see that using this circuit at progressively higher frequencies will significantly reduce the frequency variation of $|T(j\omega)|$, and by extension the magnitude error of the basis vectors at 90° and 270°.

III. Integrated Circuit Design

A. Active Balun

An active balun was chosen in this work to generate the 0° and 180° basis vectors because it is physically compact. Furthermore, this balun was designed to have voltage gain, which compensates for losses in other circuit stages. The active balun has a common-gate common-source (CG-CS) topology, as illustrated in Fig. 2. The input signal, $v_{\rm in}$, enters transistor $\rm T_1$ at the source and emerges at the drain with essentially a 0° phase shift. In practice there will be a very small phase shift as the signal travels through $\rm T_1$ because the transistor channel resistance, r_{ds}, and the device capacitances C_{gs} and C_{gd} constitute a parasitic *RC* phase shift network. The DC bias to the gate of $\rm T_1$ is supplied through the resistors $\rm R_2$ and $\rm R_3$ in a voltage-divider arrangement. At the same time, the gate of $\rm T_1$ is at RF ground through a large capacitor, $\rm C_4$.

When the input signal enters the gate of transistor $\rm T_2$ it emerges at the drain with a 180° phase shift. The gate of $\rm T_2$ is directly connected to the source of $\rm T_1$ and it is AC coupled to the input signal, $v_{\rm in}$. A broadband input match is obtained by using a medium-valued resistor, $\rm R_1 = 700\ \Omega$, at the input port.

In addition to obtaining the correct phase relationships at the outputs of the balun, it is important to have a good amplitude balance, and this is achieved by proper selection of the load resistors $\rm R_4$ and $\rm R_5$. In this work, both of these resistors had a value of about 400 Ω.

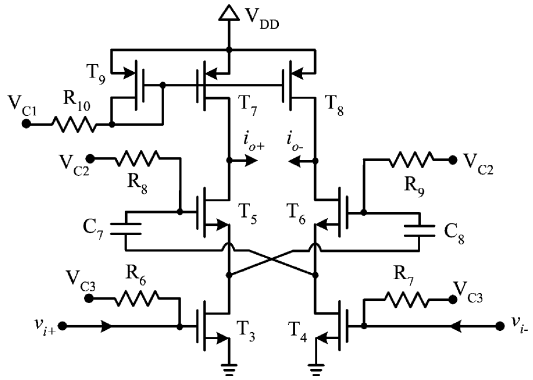

Fig. 4. OTA circuit using a feedforward-regulated topology.

A graph of the simulated balun performance is presented in Fig. 3. The voltage gain response shows a gradual roll-off versus frequency. While this roll-off will have a certain impact on the gain response of the phase-shifter, as discussed in Section IV, it is important to note that the difference between $\rm G_{21}$ and $\rm G_{31}$ (i.e., the gain imbalance) is only 0.05 dB in the 2–3 GHz range. The phase imbalance is $< 1.5°$ over this same span. A Monte Carlo simulation with 1000 trials and a 1% Gaussian-distribution on the transistor sizes was conducted to assess the effects of CMOS fabrication process variations on the balun's performance. The simulations show that for 980 trials the voltage gain imbalance is within a 0.25 dB window. The phase imbalance is within a 0.3° window for 990 trials. The Monte Carlo simulation was also conducted on the resistors of the active balun with the same variations as noted before, and the results showed that 970 trials were within a 0.4-dB range for the gain difference, and 980 trials were within a 1° range for the phase difference. High-precision resistor layouts were used for these resistors, which can mitigate the effect of the reistor variation and mismatch on the active-balun performance.

B. Feedforward-Regulated Cascode OTA

A very high-speed differential feedforward-regulated cascode OTA is used in the integrator, and its schematic is shown in Fig. 4. The feedforward regulation is implemented by using a set of cross-connections between the cascode pairs ($\rm T_3/T_5$ and $\rm T_4/T_6$). With this procedure the gate-source voltages of the cascoding transistors, $\rm T_5$ and $\rm T_6$, will either increase or

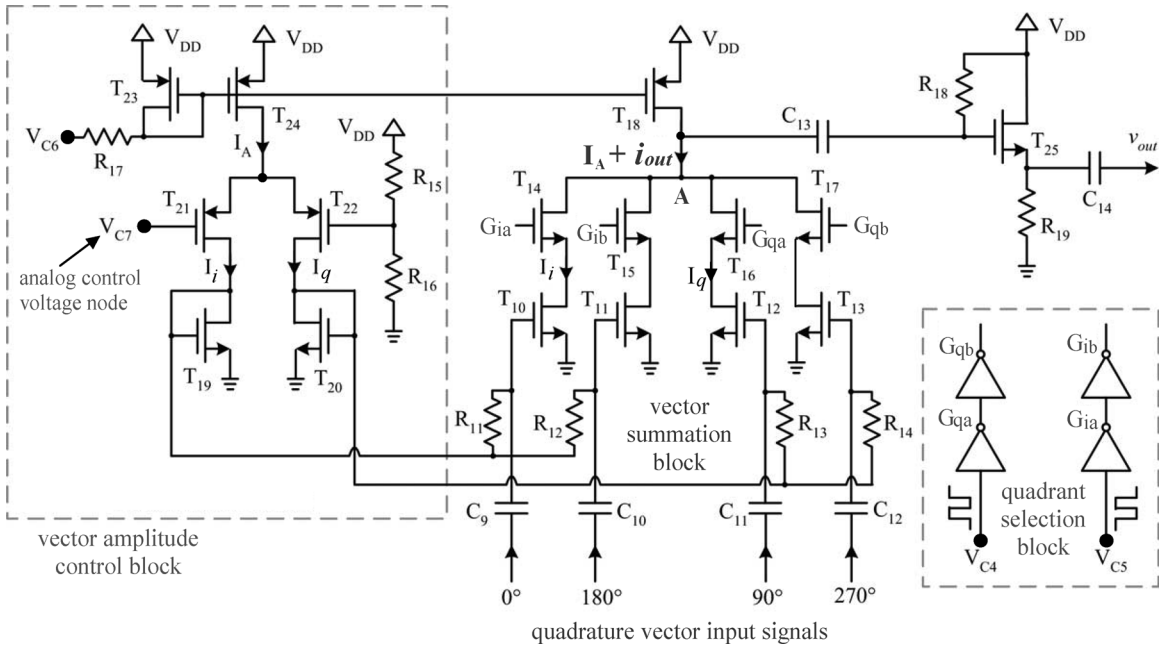

Fig. 5. Vector summing junction network.

decrease to counteract changes in the drain voltages of T_3 and T_4 when there are large differential input signals. The result is a stabilization of the drain voltages of transistors T_3 and T_4 by creating an inter-locking regulation mechanism between these two drain voltages. This OTA cell is a variant of our previous works on feedforward-regulated OTA's, which are described in detail in [13], [14].

The DC bias voltages to all the transistor gates in the OTA are applied through a set of very large resistors, R_6–R_{10}, and capacitors C_7 and C_8 are used for DC isolation between the cascode transistors. The OTA uses a pMOS current mirror arrangement consisting of transistors T_7–T_9 as the DC current source.

The expression for the transconductance of the OTA can be derived by making use of the symmetry in the circuit and the result is

$$G_m = \frac{i_{o+} - i_{o-}}{v_{i+} - v_{i-}} = g_{m3}\left[\frac{\frac{1}{r_{o5}} + 2g_{m5}}{\frac{1}{r_{o3}} + \frac{1}{r_{o5}} + 2g_{m5}}\right] \tag{4}$$

where r_{o3} and r_{o5} are the small-signal output resistances of transistors T_3 and T_5, respectively, and g_{m3} and g_{m5} are the transconductances of T_3 and T_5. Since r_{o3} and r_{o5} are in the $\mathrm{k}\Omega$ range and since g_{m5} is usually a few mS, we conclude that

$$G_m \approx g_{m3}. \tag{5}$$

This equation implies that the G_m of the OTA can be varied through just one control voltage in Fig. 4, namely V_{C3}. This is highly convenient since it allows the designer to easily make $G_m = \omega C_1/2$ as described in Section II.

Making use of the symmetry in the OTA, it is also straightforward to derive the output resistance of the circuit. That resistance is given by

$$R_o = 2r_{o3} + 2r_{o5} + 4g_{m5}r_{o3}r_{o5} \tag{6}$$

which yields values on the order of $10^4\ \Omega$.

C. Quadrature Vector Summing Network

The four quadrature basis vectors generated by the active balun and OTA integrator enter the vector summing network at the bottom of the diagram shown in Fig. 5. The summing network consists of three distinct sub-circuits, or blocks. The core of the network is the "vector summation block" which is where the vector addition occurs and it consists of four cascode circuits: $\mathrm{T}_{10}/\mathrm{T}_{14}$, $\mathrm{T}_{11}/\mathrm{T}_{15}$, $\mathrm{T}_{12}/\mathrm{T}_{16}$, and $\mathrm{T}_{13}/\mathrm{T}_{17}$. The upper transistors in the cascodes, T_{14}–T_{17}, are switched on or off by four control signals, G_{ia}, G_{ib}, G_{qa} and G_{qb}. These control signals select which two quadrature vector currents will be added together at node A, and thus the vector summation is achieved.

The "quadrant selection block", shown on the bottom-right in Fig. 5, consists of four basic digital CMOS inverters with the two digital control signals V_{C4} and V_{C5} acting as their inputs. For instance, when $\mathrm{V}_{C4} = 0$ V and $\mathrm{V}_{C5} = 0$ V, the four switching signals are $\mathrm{G}_{ia} = 0$, $\mathrm{G}_{ib} = \mathrm{V}_{\mathrm{DD}}$, $\mathrm{G}_{qa} = 0$, and $\mathrm{G}_{qb} = \mathrm{V}_{\mathrm{DD}}$. Therefore, in the vector summation section block, the 0° and 90° currents will be added at node A, yielding an output signal in quadrant I. Table I lists the relationship between the digital control voltages, V_{C4} and V_{C5}, and the quadrant of the final output vector.

Once two basis vectors have been selected for summation at node A, their amplitudes are adjusted in order to obtain the desired output phase anywhere within the selected quadrant. The vector amplitudes are changed through the gate voltages of transistors T_{10}–T_{13}. If two vectors are to be added, say the 0° and 90° vectors again, then to ensure that the resulting vector has a constant magnitude then the amplitudes of the basis vectors have to vary relative to each other such that the following constraint is obeyed

$$\sqrt{A_0^2(v) + A_{90}^2(v)} = k \tag{7}$$

TABLE I
QUADRANT SELECTION TABLE

V_{C4}	V_{C5}	Selected Vectors	Output Quadrant
0	0	0° + 90°	I
0	V_{DD}	90° + 180°	II
V_{DD}	0	0° + 270°	IV
V_{DD}	V_{DD}	180° + 270°	III

where k is a constant and $A_0(v)$ and $A_{90}(v)$ are, respectively, the amplitudes of the 0° and 90° vectors as a function of the control voltage, v.

The "amplitude control block" shown on the left-hand side of Fig. 5 is used to change the basis vector amplitudes in accordance with the constraint specified by (7). In this block, a differential pair consisting of pMOS transistors T_{21} and T_{22} is biased with a supply current, I_A. A DC control voltage, $v = V_{C7}$, is applied to the gate of T_{21} in order to fully steer the current I_A from transistor T_{21} to T_{22} and vice-versa.

As I_A is steered between T_{21} and T_{22}, the drain voltages of these two transistors also change in a manner that tracks the current steering process. Since the drains of T_{21} and T_{22} are connected to the gates of transistors T_{10} and T_{12}, this is the manner in which we can precisely control the amplitudes of the basis vectors in accordance with (7). Next, we will show how this amplitude control mechanism works in more detail by deriving the main governing equations.

At the source terminal of the differential pair T_{21}–T_{22}, the currents have to satisfy the node equation

$$I_A = I_i + I_q \tag{8}$$

where I_i is the current flowing in device T_{21} and I_q is the current flowing in T_{22}. Using the short-channel MOS device equations in the saturation region, one can write the current-voltage relationships for transistors T_{21} and T_{22} as

$$I_i = v_{\text{sat}} C_{\text{ox}} W \left(V_{GS_i} - V_{tn} - \frac{V_{D\text{SAT}_i}}{2} \right) \tag{9}$$

$$I_q = v_{\text{sat}} C_{\text{ox}} W \left(V_{GS_q} - V_{tn} - \frac{V_{D\text{SAT}_q}}{2} \right). \tag{10}$$

It is important to note that these two currents are used to control the gate voltages of T_{19} and T_{20} and by extension the gate voltages of T_{10} and T_{12}.

Since the transconductance of a MOS transistor is calculated from $g_m = \partial i_{DS}/\partial V_{GS}$, then for a short-channel device we have that

$$g_m = v_{\text{sat}} C_{\text{ox}} W \approx \mu_n C_{\text{ox}} \left(\frac{W}{L} \right) V_{D\text{SAT}} \tag{11}$$

which results from invoking the constant saturation-velocity approximation [15]

$$v_{\text{sat}} \approx \left(\frac{\mu_n}{L} \right) V_{D\text{SAT}}. \tag{12}$$

The 0° and 90° small-signal currents flowing in transistors T_{10} and T_{12} are given by

$$i_0 = g_m \tilde{v} = \gamma V_{D\text{SAT}_i} \tilde{v} \tag{13}$$

$$i_{90} = j g_m \tilde{v} = j \gamma V_{D\text{SAT}_q} \tilde{v} \tag{14}$$

where $\gamma = \mu_n C_{\text{ox}}(W/L)$ and $\tilde{v}$ is the amplitude of the small-signal basis vector signals that enter the summing junction at the bottom of Fig. 5. This pair of currents are added at node A in the vector summation block of Fig. 5 to yield the output signal current

$$i_{\text{out}} = i_0 + i_{90} = \gamma [V_{D\text{SAT}_i} + j V_{D\text{SAT}_q}] \tilde{v}. \tag{15}$$

The voltages $V_{D\text{SAT}_i}$ and $V_{D\text{SAT}_q}$ are a function of the gate-to-source voltages of the differential pair T_{21}–T_{22}, which are themselves dependent on the phase control voltage, V_{C7}. Therefore, it is of interest to determine the relationship between these sets of voltages. Substituting (12) into (9) and setting the latter equation to zero yields a quadratic equation in terms of $V_{D\text{SAT}_i}$

$$I_i - \gamma (V_{GS_i} - V_{tn}) V_{D\text{SAT}_i} + \frac{\gamma}{2} V_{D\text{SAT}_i}^2 = 0 \tag{16}$$

whose only useful solution is

$$V_{D\text{SAT}_i} = V_{GTi} + \sqrt{V_{GTi}^2 - \frac{2}{\gamma} I_i} \tag{17}$$

and follwing a similar analysis for $V_{D\text{SAT}_q}$ yields

$$V_{D\text{SAT}_q} = V_{GTq} + \sqrt{V_{GTq}^2 - \frac{2}{\gamma} I_q} \tag{18}$$

where $V_{GTi} = V_{GS_i} - V_{tn}$ and $V_{GTq} = V_{GS_q} - V_{tn}$. Inserting (17) and (18) into (15) we can determine the expression for the output phase angle of the phase shifter to be

$$\phi_{\text{out}} = \tan^{-1} \left(\frac{V_{GTi} + \sqrt{V_{GTi}^2 - \frac{2I_i}{\gamma}}}{V_{GTq} + \sqrt{V_{GTq}^2 - \frac{2I_q}{\gamma}}} \right). \tag{19}$$

IV. EXPERIMENTAL RESULTS

The vector-sum phase shifter was fabricated using a standard 0.18-μm CMOS process. The chip core without bonding pads measures just 0.15 mm^2 and 0.38 mm^2 with pads. The IC uses a supply voltage of 2 V and consumes 12 mA of DC current, resulting in a power consumption of 24 mW. A microphotograph of the fabricated chip is shown in Fig. 6.

Using an Agilent 8510C vector network analyzer, the phase shifting performance of the chip was measured. Fig. 7 shows the measured phase shift as a function of the control voltages, V_{C7} (fine tuning) plus V_{C4} and V_{C5} (quadrant selection). The

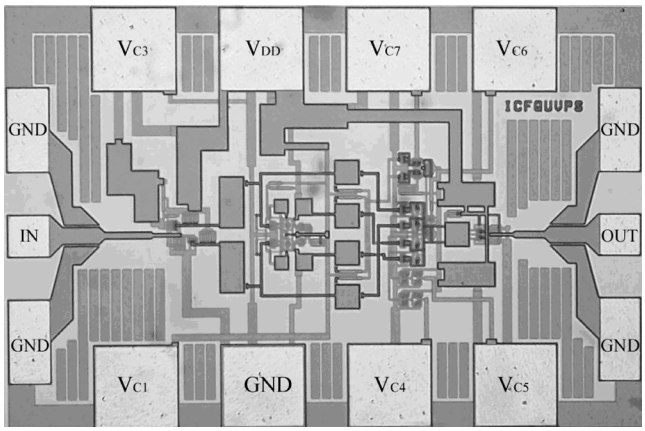

Fig. 6. Microphotograph of the fabricated phase shifter.

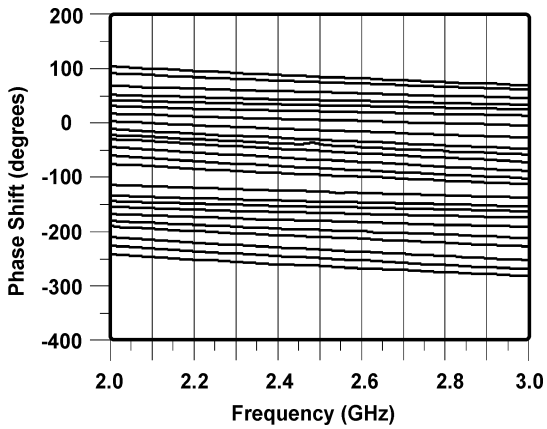

Fig. 7. Measured phase shift versus frequency and control voltage, V_{C7}.

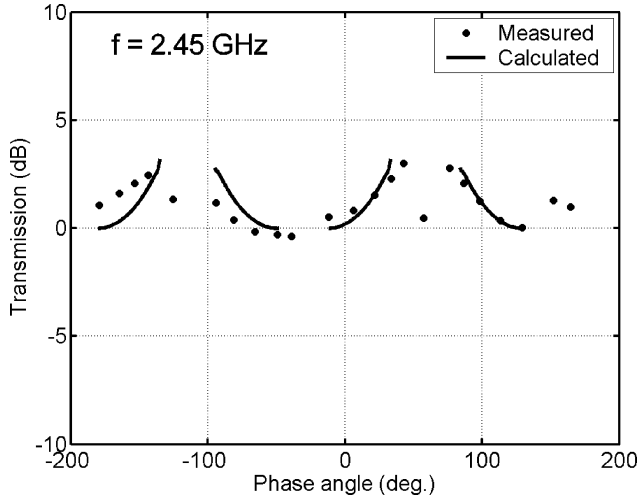

Fig. 8. Transmission coefficient (S_{21}) versus phase angle, ϕ_{out}.

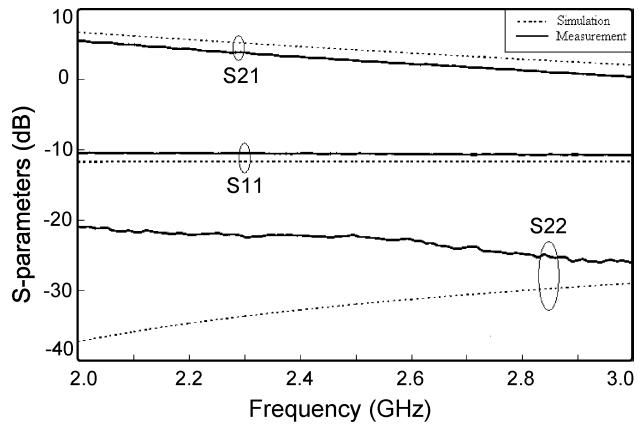

Fig. 9. Measured and simulated s-parameters.

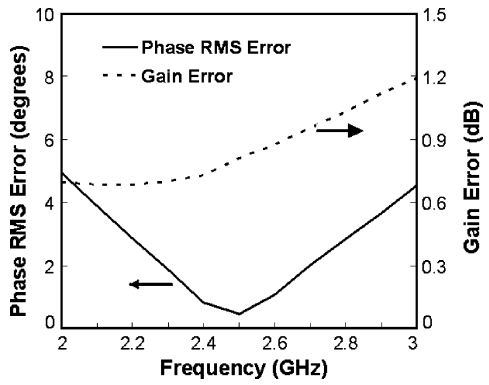

Fig. 10. RMS phase error and gain error versus frequency.

results indicate a full 360° variable phase shift range from 2 to 3 GHz, which includes the 2.4-GHz ISM band, and in addition the curves are quite linear across this frequency range.

In Fig. 8 the measured and calculated signal transmission coefficient, S_{21}, through the phase shifter is plotted as a function of the output phase angle. The theoretical results were obtained using (15) and (19). The measurement was taken at a frequency of 2.45 GHz, the center of the ISM band. We observe that the phase shifter exhibits a gain variation of 1.5 ± 1.5 dB versus phase angle. Note that the gain variation can be eliminated by placing a limiting amplifier after this phase shifter.

The measured and simulated S-parameter magnitudes for this phase shifter are plotted in Fig. 9. For this measurement, the data was taken at a fixed phase-shift control voltage. The observed roll-off in S_{21} is attributed primarily, but not exclusively, to the frequency response of the active balun circuit which was previously shown in Fig. 3.

The results in Fig. 9 show that the input reflection coefficent (S_{11}) is around -10 dB. Further measurements (not shown) reveal that S_{11} changes very little as a function of output phase angle. This is because the first sub-circuit of the IC is an active balun circuit which isolates the input terminal from the rest of the chip where the phase shifting operations are occurring. Since the phase shifting mechanism involves varying the DC current flows in the system, and these have a direct effect on the small-signal circuit parameters of the system, the output reflection coefficient, S_{22}, does experience a more noticeable variation versus phase shift angle.

Using the measurements plotted in Fig. 7, the rms phase error and gain error versus frequency were calculated and the results are shown in Fig. 10. The graph shows that the phase error is below 5° over the 2–3 GHz band.

The measured Noise Figure (NF) of this phase shifter is plotted in Fig. 11. The NF data was taken at equally spaced

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OTHER 360° IC PHASE SHIFTERS

Ref.	Method	Frequencies (GHz)	Phase Range	Die area (mm^2)	$f_{min} \times A$	P_{DC} (mW)	$P_{1dB,in}$ (dBm)	S_{21} (dB)	Technology
This Work	Vector sum	2.00–3.00	360°	0.38	0.76	24	-13.5	1.5±1.5 @ 2.45 GHz	0.18-μm CMOS
[16]	LC structure	3.50–4.50	360°	0.24	0.84	25 (max)	–	-0.3±0.8	0.18-μm CMOS
[6]	All-pass ntwk	5.85–8.20	360°	1.37	8.01	–	–	-5.7±0.8	0.5-μm pHEMT
[2]	Reflection-type	5.15–5.70	360°	0.90	4.6	0	2	-9	GaAs MESFET
[17]	Vector sum	15.0–20.0	360°	0.72	10.8	–	–	-8	0.18-μm CMOS
[12]	Vector sum	15.0–26.0	360°	0.45	6.75	11.7	-0.8±1.1	-3.8±0.8	0.13-μm CMOS

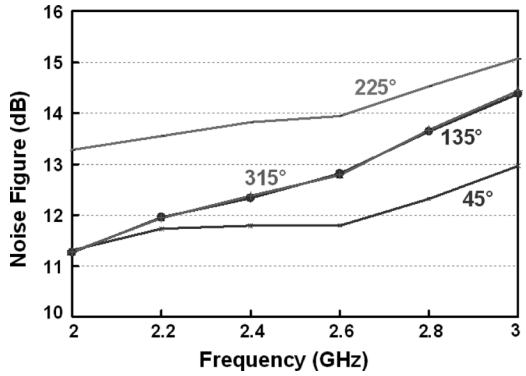

Fig. 11. Measured noise figure (NF) at various phase angles.

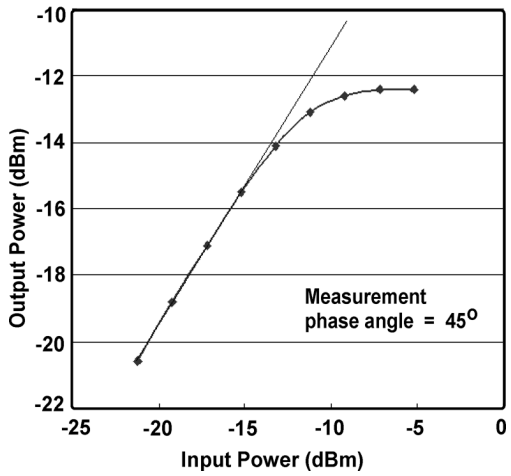

Fig. 12. Measured RF power performance (data taken at 45° phase shift).

phase shift angles covering the four quadrants. The phase noise increases with frequency and it ranges from 11.3 dB at 2 GHz to about 15 dB at 3 GHz. The RF power performance of the phase shifter was measured at a phase shift angle of 45° and the results are plotted in Fig. 12 and we observe that the input-referred 1-dB compression point ($P_{1\ \mathrm{dB},in}$) is about -13.5 dBm.

A performance summary and comparison between this work and other fully monolithic phase shifters exhibiting a 360° variable phase range is shown in Table II. The works are arranged from lowest to highest operating frequency. Since the IC's in Table II cover different frequency bands, a simple one-to-one comparison of the performance metrics is not trivial, specially as it pertains to the die area used in relation to operating frequency (or wavelength). Therefore, we have calculated a very basic metric in Table II which is the product of the minimum operating frequency of the chip (in GHz) and the area of the chip (in mm^2)

$$f_{\min} \times A. \tag{20}$$

Using this simple metric reveals that the technique described in this paper does achieve its goal of producing a highly compact phase-shifter at long wavelengths.

V. CONCLUSION

A highly compact 360° variable phase shifter IC has been proposed and experimentally demonstrated in this paper. The phase shifter uses an active balun circuit and an OTA integrator to generate the quadrature basis vectors. Although this quadrature generation method results in some additional power consumption relative to passive solutions, the benefit of the approach is that there can be signal gain, if needed. The basis vectors are added together using a purpose-built summing junction which varies the amplitudes of the vectors by means of a current-steering mechanism and a current-to-voltage conversion stage. Measured results show that this chip competes quite well with previous works, specially at long wavelengths.

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