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Very low frequency tunable signal generator for neural and cardiac cell stimulation

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An integrated circuit capable of generating very low-frequency signals for biomedical applications is presented in this article. By employing microwave circuit design concepts and techniques, the chip can produce very low frequency signals starting from a pair of 4 GHz signal generators. Measurements reveal that a continuous set of frequencies between 0.03 Hz and 185 Hz are generated, which represents a tuning range of 6167:1. The chip was fabricated using a standard 0.13- μm CMOS process and the circuit core measures 0.49 mm².

Keywords: neural cell stimulation; cardiac cell stimulation; RFICs; oscillators; mixers; frequency dividers

1. Introduction

Deep-brain electrical stimulation of neurons in the subthalamic nucleus is a therapy that can provide patients relief from the symptoms of Parkinson's disease (Limousin et al. 1998; Krack et al. 2003; Karimi et al. 2008). The frequency of the pulses needed to alleviate the tremors caused by Parkinson's varies from person to person, but it is typically in the range of 130 Hz to 185 Hz (Limousin 1998).

The stimulation of cardiac cells is also of major interest and has already been investigated for several decades. The signal frequencies used to stimulate cardiac tissue ranges from about 0.1 Hz to 10 Hz or more. *In vitro* cardiac tissue cultures are sometimes electrically stimulated during and after growth to better mimic their natural environment (Whittington, Giovannardi, and Kovacs 2005; Pollard, Ellis, and Smith 2008). Regarding the stimulation of *in vivo* cardiac tissue through the use of pacemakers, this is a very well established technology.

Generating very low frequency (VLF) signals often requires large-value capacitors, inductors or resistors which are not easily incorporated on-chip. By using impedance converters (Silva-Martinez and Vazquez-Gonzalez 1998) the value of a capacitor or a resistor can be artificially increased and this can help to alleviate the problem of using impractically large components in VLF signal generators (Elwakil 1998). In other designs (Veeravalli, Sanchez-Sinencio, and Silva-Martinez 2002), a capacitance converter circuit is used in conjunction with an active transconductance element, $g_m = 1/R$, to create a VLF oscillator. Such an approach needs small values of g_m which can be produced using low-power operational transconductance amplifiers (OTAs). The output frequencies for

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the circuit in (Veeravalli et al. 2002) range from 0.2 Hz to 5 Hz, representing a tuning range of 25:1.

In this article, we describe an integrated circuit (IC) in 0.13- μm CMOS technology that can generate periodic signals from 0.03 Hz to 185 Hz. We employ microwave circuit design techniques to design a pair of LC-oscillators at 4 GHz which are followed by frequency division and mixing circuits to produce the VLF signals. This approach avoids the need for impedance scaling circuits, thereby allowing the use of normal-valued inductors and capacitors in the nH and pF range, respectively. Furthermore, the use of frequency division in conjunction with a frequency mixing operation leads to an exceptionally large frequency tuning range of more than three orders of magnitude.

2. Physical considerations

The principal challenge in designing a stand-alone integrated circuit to generate VLF signals is related to the physical size of the components that are needed to generate those signals. In a general sense, the output frequency of a relaxation oscillator, f_{osc} , is proportional to the inverse product of the energy storage element and the energy loss element. A capacitor and a resistor are often used in relaxation oscillators, leading to $f_{\text{osc}} \propto 1/RC$. It is straightforward to derive a basic expression for the oscillation frequency as a function of the physical dimensions of R and C . That equation is

$$f_{\text{osc}} \propto \left(\frac{W}{R_{sq}L} \right) \left(\frac{d}{\epsilon A} \right) \quad (1)$$

Typically, a parallel plate capacitor (C) is used and thus the variable d in Equation 1 is the separation between the plates of the capacitor, A is the area of the plates and ϵ is the permittivity of the dielectric medium. IC layout design rules set an upper limit on the parallel-plate area, and typically on-chip capacitor values do not exceed 10^{-11} F. In CMOS, polysilicon is often used to make on-chip resistors and a normal value for that material's sheet resistance, R_{sq} , is in the range of $10^3 \Omega$. There is a minimum value for the width, W , of the resistor that is established by the resolution of the photolithography process, which in this article is 0.13 μm . The overall length of a resistor can be fairly long if a serpentine structure is employed. Thus, letting $L = 1$ mm in Equation 1 and substituting the other values just given into that equation, the lowest possible oscillation frequency (f_{min}) of a generic relaxation oscillator using this particular IC technology can be estimated. In our case, $f_{\text{min}} \approx 13$ kHz and for other IC technologies the lowest frequency will not be substantially different since the main distinguishing feature between technologies is the resolution of the photolithographic process. Bringing the minimum feature size to 32 nm, for instance, would result in $f_{\text{min}} \approx 3.2$ kHz which is still not low enough for most cardiac and deep-brain stimulators.

Using LC-tank oscillators for VLF applications present very similar challenges as relaxation oscillators in terms of the physical size of the components required. However, as we will explain in the remainder of this article, it is possible to generate VLF signals by using normal-sized on-chip components and at the same time achieve a very wide tuning range.

3. VLF signal generator concept

A block diagram of the VLF signal generator proposed in this article is shown in Figure 1. It consists of two microwave voltage-controlled oscillators (VCOs) whose output

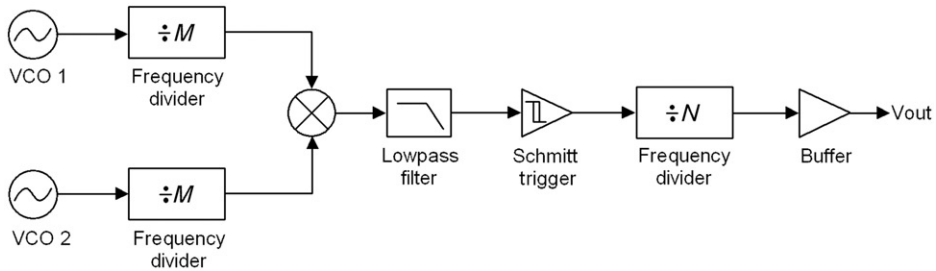


Figure 1. System architecture of the very low-frequency signal generator.

frequencies f_1 and f_2 can be tuned about their centre frequency of 4.0 GHz. This high frequency was chosen because the required values of the inductors and capacitors in the LC tank are sufficiently low (1 nH and 1.58 pF, respectively) to require a very small amount of chip area. The output of each oscillator subsequently enters a frequency divider whose function is to reduce the frequency of each signal by $1/M$. After frequency division, the two signals are fed to a mixer circuit which yields the sum and difference frequencies of the input signals. Since we are only interested in the difference frequency, also called the downconverted frequency, we use a lowpass filter after the mixer to remove the high frequency signal. The frequency of the downconverted signal is

$$f_3 = \frac{f_2}{M} - \frac{f_1}{M} = \frac{f_2 - f_1}{M} \quad (2)$$

The signal that emerges from the lowpass filter has a small amount of ripple superimposed on the desired signal. A Schmitt trigger is used as a hard limiter to remove the ripple. A second frequency division stage which reduces the frequency f_3 by a factor of $1/N$ is used in this design in order bring the frequency of the VLF signal generator into the desired range. The final output frequency is therefore,

$$f_{\text{out}} = \frac{f_3}{N} = \frac{f_2 - f_1}{MN} \quad (3)$$

To produce very low frequency signals it is necessary to use a large division ratio. In this work, a division ratio of $M \times N \approx 10^6$ was chosen by setting $M = N = 2^{10} = 1024$. Making $M = N$ allows the chip designer to re-use the same frequency division block in three distinct places, which is convenient during simulation and layout. However, since it takes ten $\div 2$ stages to reach $\div 1024$ and there are three $\div 1024$ blocks in Figure 1, a total of 30 $\div 2$ stages were needed. This large number of $\div 2$ stages ultimately increases the area and power consumption of the overall circuit. This situation can be mitigated somewhat by making $M < N$ while keeping intact the constraint that $M \times N \approx 10^6$. For example, if $M = 2^5 = 32$ and $N = 2^{15} = 32,768$, then a total of twenty five $\div 2$ units would be needed in Figure 1 instead of thirty, yielding a savings of five $\div 2$ units.

4. Integrated circuit design

4.1. Voltage-controlled oscillators

The two oscillators used in this work were identical negative-resistance LC-tank circuits and their schematic diagram is shown in Figure 2. The two cross-coupled NMOS and PMOS transistors synthesise a negative resistance which precisely cancels the losses in the

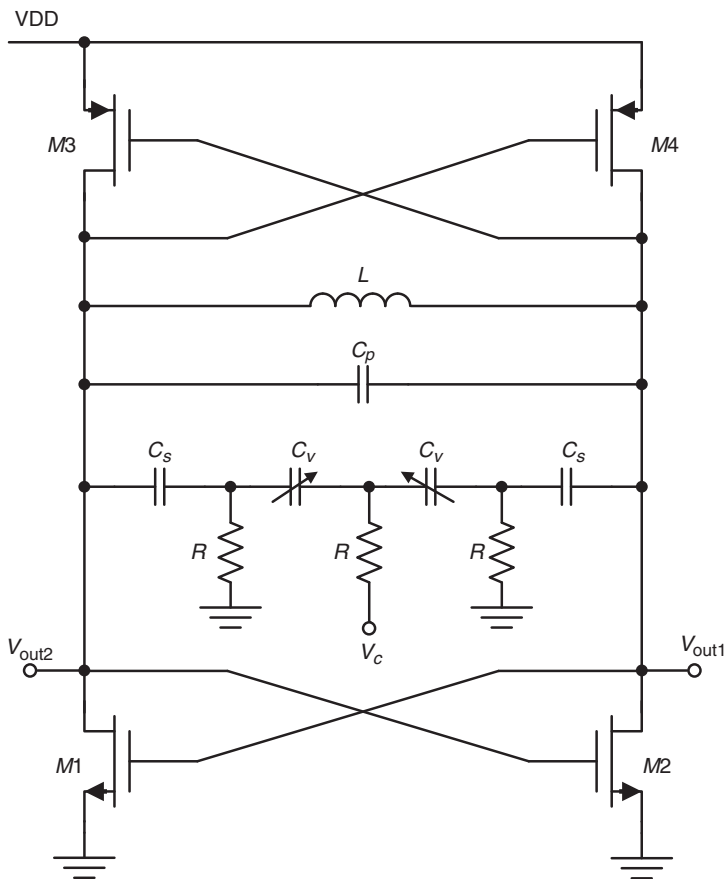


Figure 2. Voltage-controlled oscillator.

LC-tank, thereby sustaining the oscillations in the steady state. If the resonator has a shunt parasitic resistance R_p and the transconductance of the PMOS and NMOS transistors are given by g_{mp} and g_{mn} , respectively, then in order to sustain the oscillation the negative resistance of the differential pairs needs to be

$$R_{\text{neg}} = -R_p = \left(\frac{-2}{g_{mp}}\right) + \left(\frac{-2}{g_{mn}}\right) \quad (4)$$

The above topology also produces oscillators with lower phase-noise compared to oscillators that rely on only one NMOS cross-coupled pair (Hajimiri and Lee 1999).

The on-chip inductor used in the LC-tank had an octagonal spiral geometry and the capacitive element consisted of a varactor network to allow for frequency tuning of the oscillators through the voltage V_c . Two capacitors are connected in series with the varactors in order to form a symmetric network to allow for precisely controlled capacitance variations. The output frequency of the oscillator can be written as,

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (5)$$

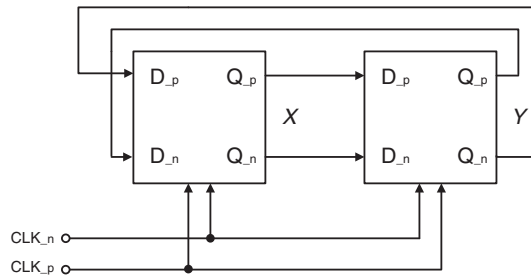


Figure 3. Block diagram of the $\div 2$ circuit.

where L is the tank inductance the capacitance is given by,

$$C = C_p + \frac{C_s C_v}{2(C_s + C_v)} \quad (6)$$

The oscillators were designed to have a free-running output frequency of 4 GHz. Their tuning range was 100 MHz as the control voltage varied from -0.5 V to 1 V. Each oscillator consumed 6.1 mA of DC current from a 1.2 V supply.

4.2. Frequency division circuits

To realise the $\div 1024$ operation, $10 \div 2$ circuits were cascaded since $2^{10} = 1024$. Each $\div 2$ circuit comprised a pair of D flip-flop latches in a negative feedback loop arrangement as shown in Figure 3. The D-latches, in turn, consist of a differential pair plus a regenerative circuit to enable very high-frequency operation (Razavi 1998). The transistor-level schematic of the D-latches used in this work is depicted in Figure 4.

It is well-known that frequency dividers can consume significant amounts of dc power relative to other RF components such as mixers and oscillators. Therefore, in order to reduce power consumption, the load resistors in the D-latches were designed to be relatively large (around 800Ω) and at the same time the transistors had a fairly small gate width of $7.5 \mu\text{m}$. As a result, each $\div 2$ circuit consumed only 2.1 mA of current from a 1.2 V supply.

4.3. Mixer and low-pass-filter

The mixer circuit used in the IC was based on the Gilbert-cell double-balanced mixer (Gilbert 1968) and its schematic is shown in Figure 5. While simpler mixing circuits could have been used, the advantage of using a Gilbert-cell is the well-known fact that it has conversion gain and therefore no amplifiers were needed after the mixer to boost the output signal.

The output resistance of this type of mixer is approximately $R_L // r_o$, where R_L is the resistance of the load and r_o is the differential output resistance of the NMOS devices. It is important to make the load resistance of the mixer larger than its own output resistance so that most of the output voltage drop occurs across the load. In our case, the mixer was followed by a filter and a high-input impedance Schmitt trigger.

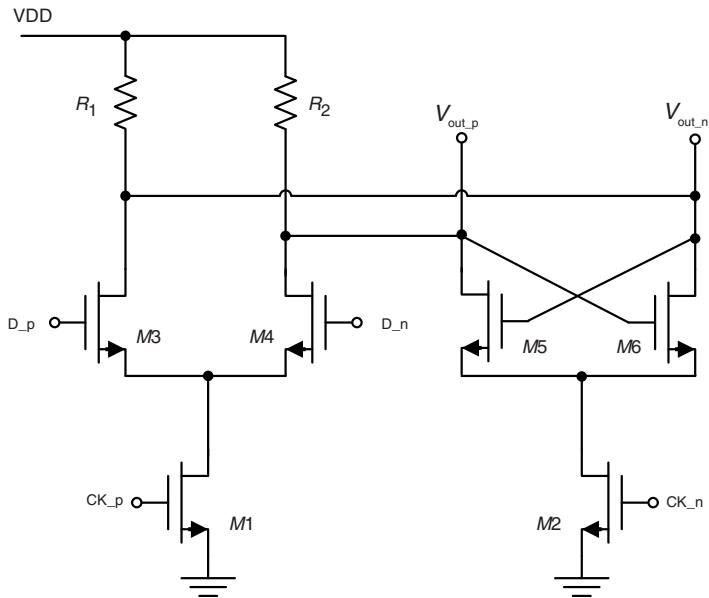


Figure 4. Implementation of the D-latch used in the $\div 2$ circuits.

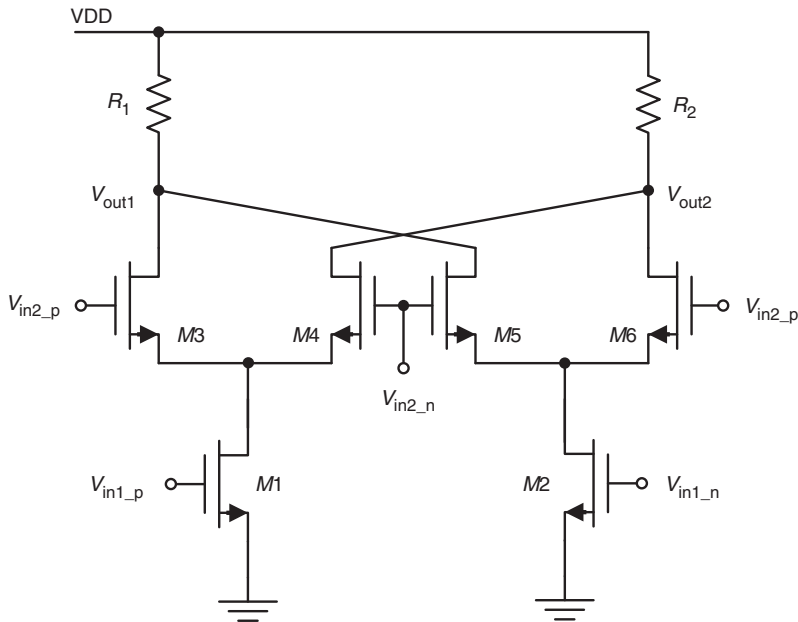


Figure 5. Mixer circuit.

Since we were only interested in the low-frequency signal generated by the mixer, a lowpass filter was used to suppress the unwanted high-frequency waveforms. The upconverted signal was at 8 GHz and the desired low frequency signals were in the 4 MHz range. Therefore, a simple one-pole RC network was sufficient for our purposes.

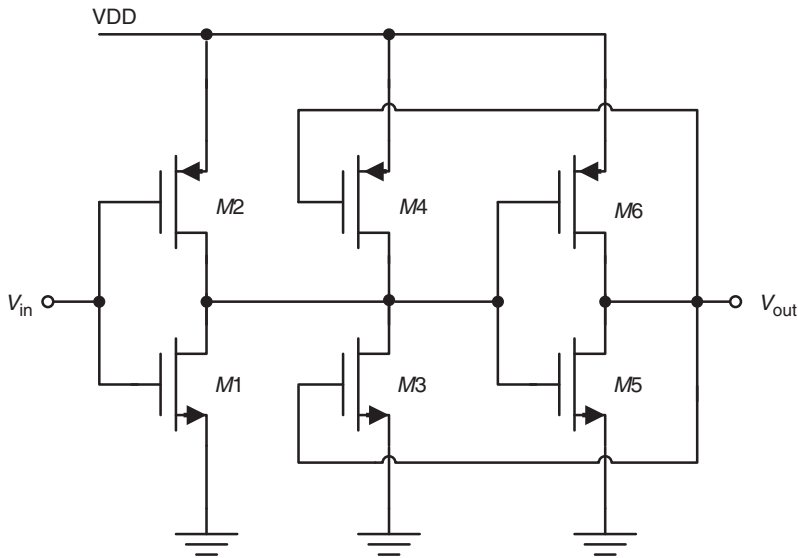


Figure 6. Schmitt Trigger.

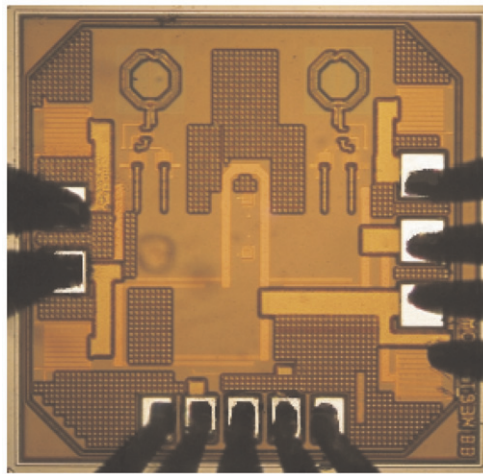


Figure 7. Fabricated die photograph.

4.4. Schmitt Trigger

While the lowpass filter significantly attenuates the unwanted high-frequency signal generated by the mixer, there is still a residual amount of energy from that frequency component which manifests itself as a ripple superimposed on the desired low-frequency signal. Furthermore, since the downconverted signal needs to be frequency divided again using D-latches, which are digital circuits, then it is critical to transform the sinusoid into a digital signal. Therefore, we used a Schmitt Trigger to eliminate the ripple simultaneously and to convert the signal into a square-wave.

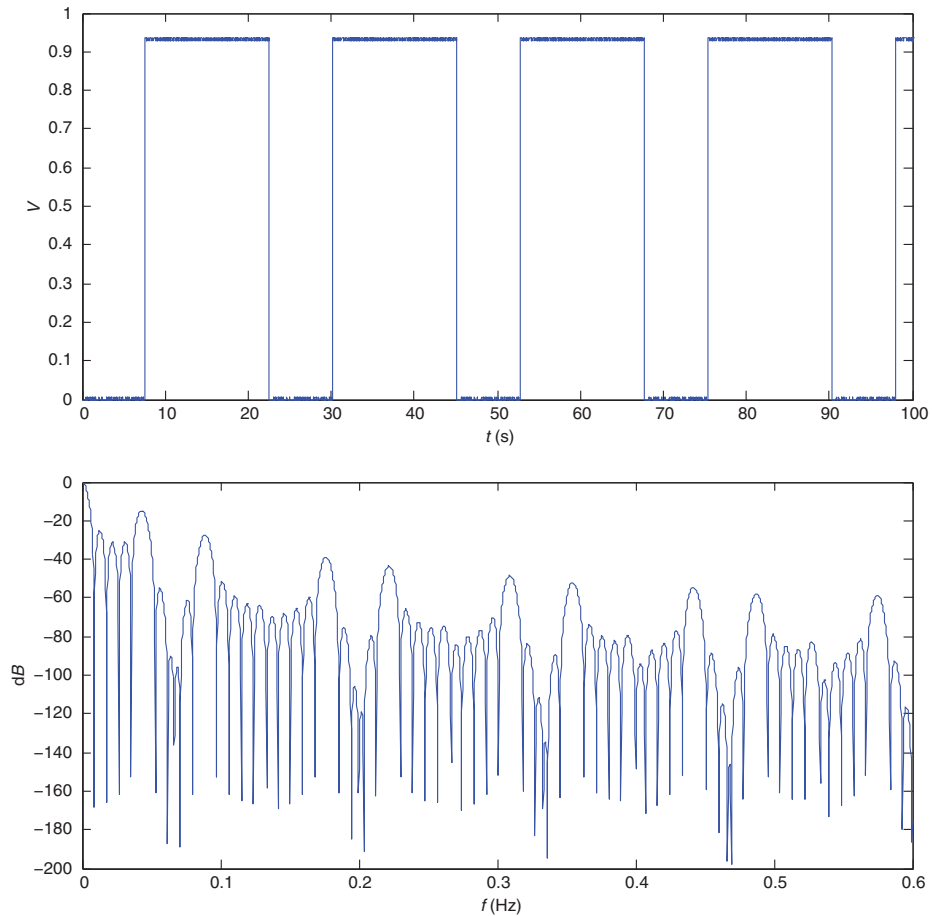


Figure 8. Measured waveform at 0.03 Hz: (a) time-domain and (b) spectral response.

A schematic of the Schmitt Trigger is shown in Figure 6. The trigger has a high threshold voltage, V_{hi} , and a low one, V_{lo} . When the input signal is above V_{hi} the output voltage will be at logic 1 and when the input is below the V_{lo} , the output voltage will be at logic 0. If the input signal falls between the two threshold voltages, the output signal will retain its last value. In this work, V_{hi} was designed to be 0.8 V, while V_{lo} was set to 0.5 V.

5. Measured results

The circuit was fabricated in 0.13- μm CMOS technology and a photograph of the die is shown in Figure 7. The chip core measures 0.45 mm² without test pads and 1 mm² with pads. The circuit was biased from a single 1.2 V supply.

Since the circuit generates a differential output signal, on-wafer testing was carried out using GSGSG differential coplanar waveguide (CPW) probes. A Tektronix TDS 210 oscilloscope was used to measure the output waveforms in the time-domain. One of the

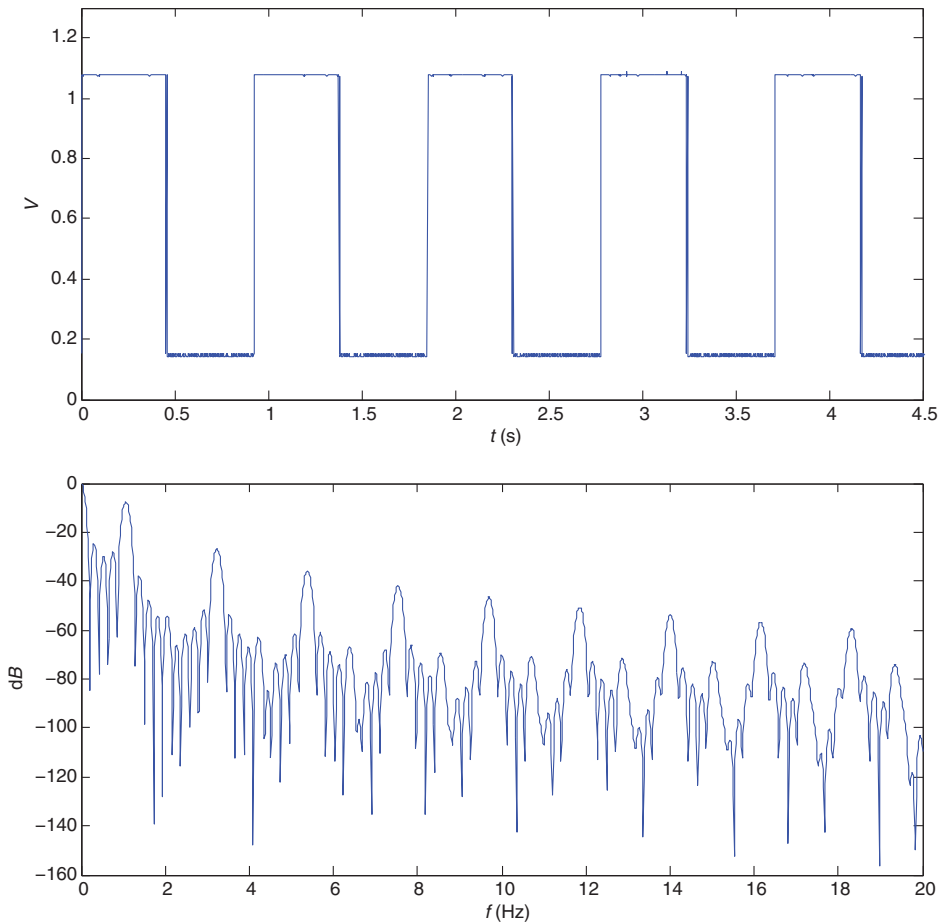


Figure 9. Measured waveform at 1 Hz: (a) time-domain and (b) spectral response.

differential outputs was fed to the display input port of the oscilloscope, while the other output signal was used to trigger the instrument.

In the experiments, VCO_1 was kept at a fixed frequency while VCO_2 was tuned in order to produce different output frequencies. As a result, the control voltage of VCO_1 was kept constant at 0.9 V.

Figure 8 shows the measured time-domain waveform of the lowest frequency signal generated by the chip, which was at 0.03 Hz. The control voltage of VCO_2 was $V_{c2} = 0.8$ V. The spectral plot was generated by taking the Fourier transform of the measured time-domain data using Matlab.

Figure 9 shows the measurements of a 1 Hz waveform and its associated spectra. To produce the 1 Hz signal, the control voltage V_{c2} was set to 0.788 V. When $V_{c2} = 0.589$ V a 10 Hz wave is obtained as shown in Figure 10. The highest frequency that was generated was 185 Hz when $V_{c2} = -0.5$ V and its graph is shown in Figure 11.

We observe that the amplitudes of all the measured signals was nearly constant at 0.93 V for all cases. This is expected since the final stages of the signal generator chip

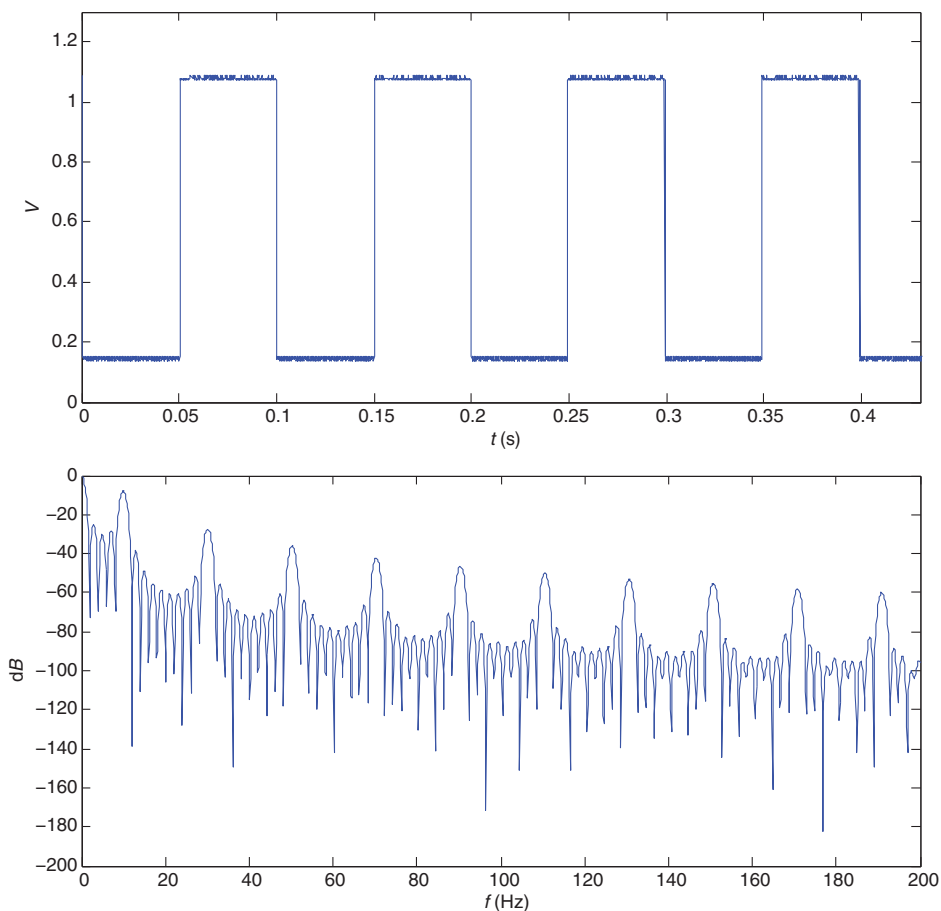


Figure 10. Measured waveform at 10 Hz: (a) time-domain and (b) spectral response.

consist of a frequency divider followed by a buffer circuit. The divider has a chain of 10 flip-flops, which are digital circuits that produce a binary pair of output voltages.

The duty cycle of the measured waveforms was 50%. However, at 0.03 Hz the duty cycle looks somewhat smaller. All electronic systems experience a transient period before reaching steady state and since the period associated with a 0.03 Hz signal is 33 s, the transient period can last for many minutes. Therefore, with a sufficiently long measurement period it is expected that the duty cycle of the waveform in Figure 8 will eventually settle down to 50% since the graph on Figure 8 only captures 5 wave cycles.

The plot in Figure 12 shows the output frequencies produced by the chip versus the control voltage, V_{c2} . The frequency spans from 0.03 Hz to 185 Hz as V_{c2} varies from 0.8 V down to -0.5 V. This represents a tuning range of over 6100:1.

A summary of the measured results is given in Table 1 together with a comparison to related works. The circuit described in this article can produce the lowest frequency and it has the largest tuning ratio. At the same time, however, the power consumption of the chip is higher than the other works. The high power consumption stems from the large number of frequency division stages. Furthermore, low-power design techniques such as sub-threshold operation were not employed because the goal of this chip was to verify the

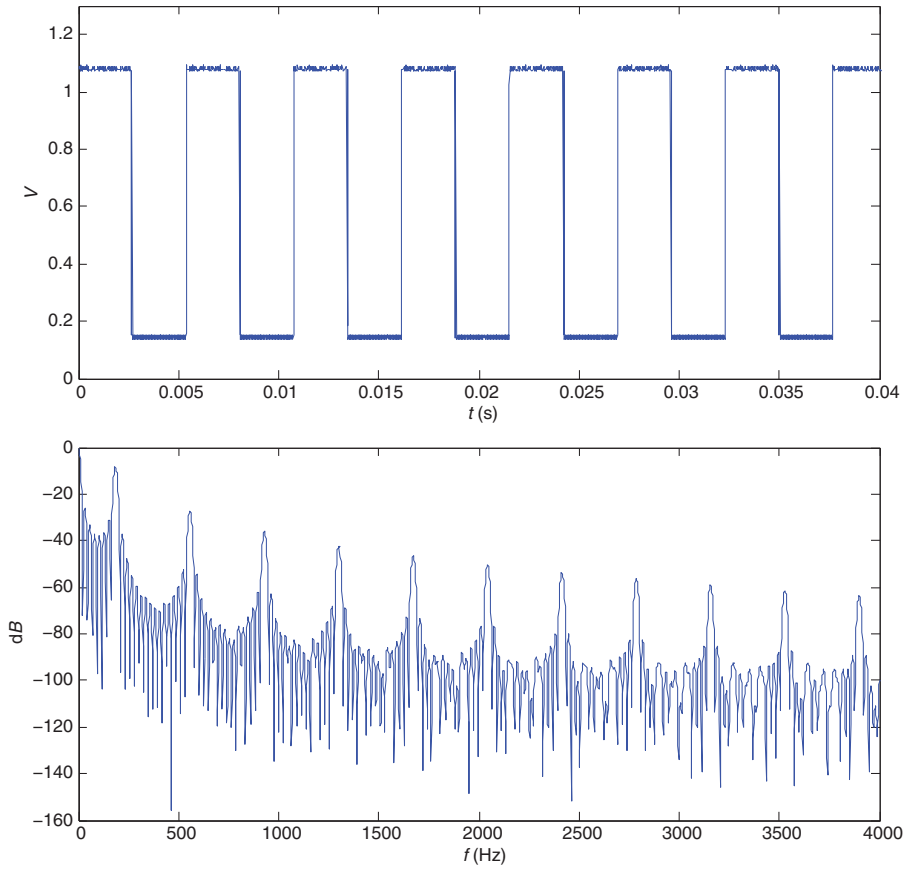


Figure 11. Measured waveform at 185 Hz: (a) time-domain and (b) spectral response.

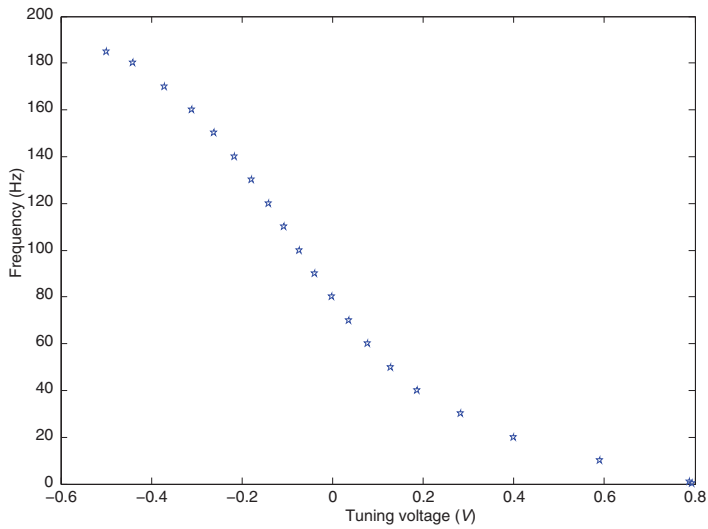


Figure 12. Measured output frequency versus control tuning voltage.

Table 1. Summary of measured results and comparison table.

	This work	Veeravalli et al. (2002)	Hwang et al. (1995)
Minimum frequency (Hz)	0.03	0.2	0.3
Maximum frequency (Hz)	185	5.0	100
Tuning ratio	6167:1	25:1	333:1
Chip core area (mm ²)	0.45	2.16	0.281
DC supply voltage (V)	1.2	±1.5	3.0
DC power dissipation	97.2 mW	5.57 μW	0.3 μW
CMOS technology	0.13-μm	1.2-μm	2-μm

functionality of the idea depicted in Figure 1. Future iterations of this chip in which devices are operated in the sub-threshold region should significantly lower the power consumption.

6. Conclusion

A new method to generate very low-frequency signals has been presented which relies on microwave circuit design techniques and makes use of both frequency division and frequency mixing. The chip can produce signals in the range of 0.03–185 Hz and therefore it can be used for either deep brain or cardiac tissue stimulation. The chip has the widest tuning range reported to date for a VLF oscillator, yet the power consumption is high due to the multiplicity of $\div 2$ sub-circuits needed to obtain a 10^6 division ratio. The power consumption can be lowered by using low-power design techniques such as sub-threshold device operation.

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