A 5.4 GHz Fully-Integrated Low-Noise Mixer

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ABSTRACT

A fully integrated CMOS low-noise mixing circuit operating at an RF frequency of 5.4 GHz is presented in this paper. The mixer is a Gilbert cell with a low-noise transconductor stage and a current-bleeding circuit. The transconductor, designed using the power constrained simultaneous noise and input match technique, together with the bleeding circuit enables the mixer to have a measured single-sideband noise figure of 7.8 dB and a power conversion gain of 13.1 dB. The output-referred 1-dB compression point, OP_{1dB}, is -5 dBm and the output-referred IP3 is $+6.9$ dBm. All of the inductors are on-chip and the size of the mixer core is only 380 μm x 350 μm (0.133 mm^2).

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: General

General Terms

Design, experimentation, measurement, performance, reliability, verification

Keywords

Analog circuits, RFIC, mixer, CMOS, broadband, MMIC, low-noise circuits, microwaves

1. INTRODUCTION

Mixers and low-noise amplifiers (LNA's) are important components at the receiver front-end. A proper design of these components is essential in order to meet the requirements of a particular standard. These components are normally designed separately and compromises in terms of the performance of the individual blocks need to be made during system integration.

Active mixers generally produce more noise than passive mixers, yet they can have certain advantages over passive mixers such as conversion gain instead of loss. Often, one or more LNA's with sufficiently low noise figure and high amounts of gain are needed to minimize the impact of an active mixer stage on the overall system noise and to meet receiver sensitivity requirements.

The noise figure of the active Gilbert cell mixer can be significantly reduced by combining the LNA and the mixer into a single component. This type of current-reuse structure is favourable in low-cost and low-power applications and can be easily achieved by replacing the transconductor by an LNA [10]. The challenge is that as the gate-length scales down, the biasing current required increases, which in turn reduces the conversion gain. To alleviate this problem, the current-bleeding technique [4] can be applied to reduce the noise figure and supply the current required by the transconductors [8, 2, 9, 11, 3]. As the transistor gate-length is reduced, a larger bleeding circuit is required. The large tail capacitor associated with the bleeding circuit will require a shunt inductor to be placed between the drains of the transconductors to keep the gain high even when flicker noise is not a concern. This paper shows that by properly designing the transconductor, the shunt inductor can be removed while all inductors can be realized on-chip without compromising its performance.

2. INTEGRATED CIRCUIT DESIGN

In this design, the goal is to improve the performance of the low-noise mixer in Fig. 1 in several ways. While prior designs required large inductors, which often had to be placed off-chip, in this paper all of the components including the inductors have been carfully optimized to create a compact RFIC without off-chip components. Furthermore, the conversion gain of the mixer must be kept at a reasonable level such that there is no compromise in gain in using this mixer topology compared with other mixer topologies.

The low-noise transconductors shown in Fig. 1 can be designed with the simultaneous noise and impedance match (SNIM) technique to achieve the lowest possible noise figure and input match at the same time [7]. The draw back of this technique is that the large gate-source capacitance (C_{gs}) required in the transistor results in a large current consumption. Since the required C_{gs} at a particular frequency is roughly independent of technology node, the drain current increases substantially when shorter gate-length transistors are used. Furthermore, as the length of the transistor goes down, so does the operating voltage. With a small voltage headroom, the large biasing current suggests the values of the load resistors (R_{load}) must be small in order to keep all of the transistors in saturation. The low resistance value trans-

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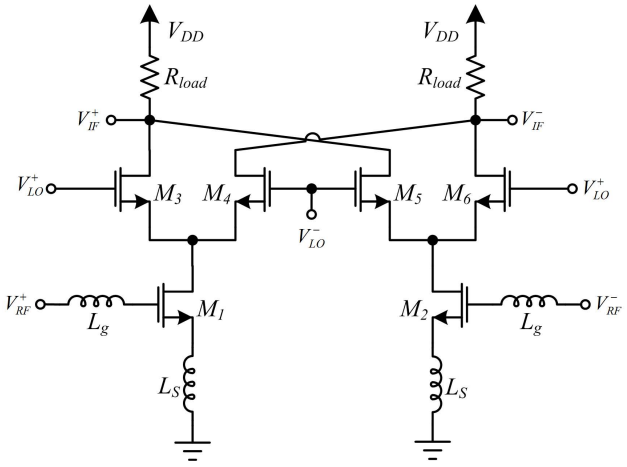

Figure 1: Conventional low-noise mixer circuit.

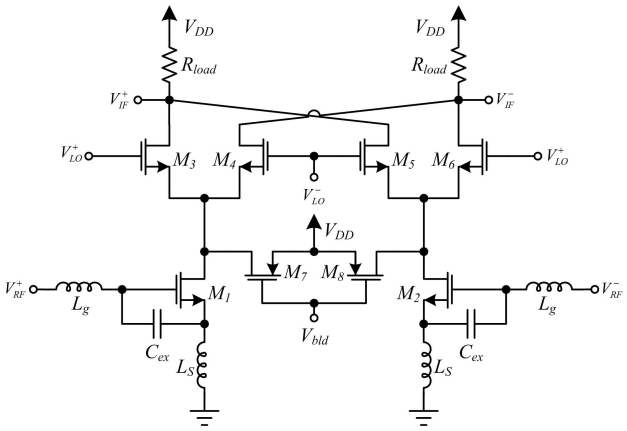

Figure 2: Improved low-noise mixer circuit.

lates into a low conversion gain for the Gilbert cell mixer, since its gain is approximately given by [5, 6]

$$A_V = \frac{2}{\pi} g_m R_{load} \tag{1}$$

where perfect switching is assumed for transistors M_3-M_6. To keep the gain high by using larger value resistors, the current flow needs to be reduced. Thus, the power constrained SNIM (PCSNIM) [7] technique is used in this paper and the resulting circuit is shown in Fig. 2. Transistors M_1 and M_2 are the low-noise transconductors and $C_{\rm ex}$ is an external capacitor placed between the gate and the source of the transistor so that the device size can be reduced. With this technique, the biasing current is reduced and the load resistors can be large. However, this approach increases the inductances needed at the source and the gate of the transistors. It is well-known that the inductor quality factor, Q, in CMOS is usually not very high, and the gate and source inductance must be kept as small as possible to maximize their Q. This in turn sets the lower bound for the transconductor size.

In order to incorporate all components on-chip, a current bleeding circuit [6] is used to break the relationship between the inductor sizes and the gain. The current-bleeding circuit is comprised of two PMOS transistors M_7 and M_8 in Fig. 2. PMOS transistors are preferable because the common-source configuration provides a high output impedance at the drain of the transistors. This large output impedance of the PMOS forces the weak RF signal to go into the switching pairs. The loading effect is, thus, much smaller compared to an NMOS bleeding circuit, where the input impedance at the source is $\frac{1}{g_m}$, which is comparable to the input impedance of the switching pair.

The switching pairs also contribute noise. In [1], the output noise density due to one switch is given by

$$\overline{|i_{o,n}|^2} = 4kT\gamma\frac{I}{\pi A} \tag{2}$$

where γ is the channel noise factor, I is the bias current, and A is the LO amplitude. From (2), it is clear that the output noise density of the switches is proportional to the bias current and inversely proportional to the LO amplitude. The current-bleeding circuit can therefore reduce the thermal noise from the switches since it has become the dominant source of current for the transconductors. With the current through the switches reduced, the size of the switches can either be reduced, which reduces the tail capacitance, or kept the same such that a smaller overdrive voltage is needed. With a smaller overdrive voltage, a more ideal switching can be obtained such that it is more like a square wave. Since the conversion gain for non-perfect switching can be approximated by

$$A_V = g_m R_{load}\frac{2}{\pi}\frac{sin(t_r/T)}{t_r/T} \tag{3}$$

where t_r is the rise time of the non-perfect square wave, the conversion gain can be improved by having a reduced overdrive voltage.

In this design, the PCSNIM technique is used in conjunction with the current-bleeding circuit. As mentioned before, this LNA design technique can reduce the current by having larger inductors. The LNA transistor is reduced to a point where high Q inductors can no longer be realized on chip at the frequency of interest. The current-bleeding circuit is then used to provide the extra current needed. The switching pairs are sized to reduce the switching rise time while keeping the tail capacitance low enough. For testing purposes, an on-chip buffer is integrated with the mixer to convert the differential output into a single-ended signal that drives a 50 Ω instrument. The buffer is designed to have a 0 dB voltage gain so that the true conversion gain of the mixer can be measured. It also acts as a broadband output matching network. Fig. 3 shows the complete circuit of the low-noise mixer.

3. EXPERIMENTAL RESULTS

The chip was fabricated using a standard 180 nm CMOS process. All of the inductors are on-chip and they were designed using ASITIC and verified with the full-wave field solver Momentum from Agilent Technologies. Furthermore, the RF input and output transmission lines were also simulated in Momentum in order to model the self inductance of the lines and other parasitics. The area for the low-noise mixer core is about 380 μm x 350 μm (0.133 mm^2) and the total chip size including pads is 700 μm x 670 μm (0.469 mm^2).

The low-noise mixer was designed at 5.4 GHz with a 300 MHz IF and a 5.1 GHz LO. All measurements were done

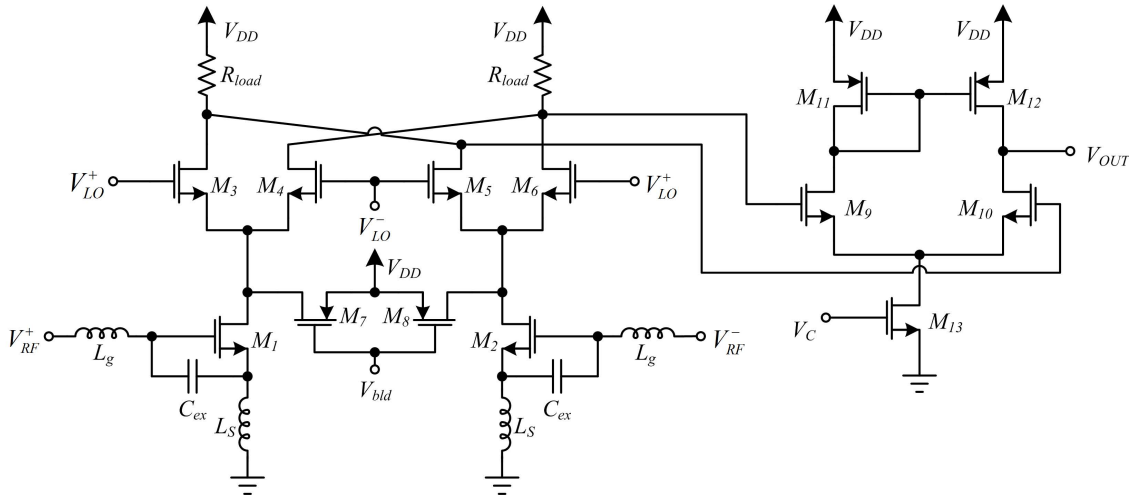

Figure 3: Complete low-noise mixer including output buffer.

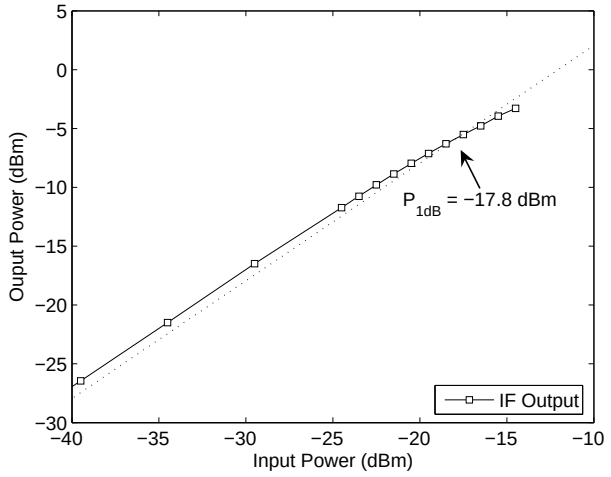

Figure 4: Measured IF output power versus RF input power.

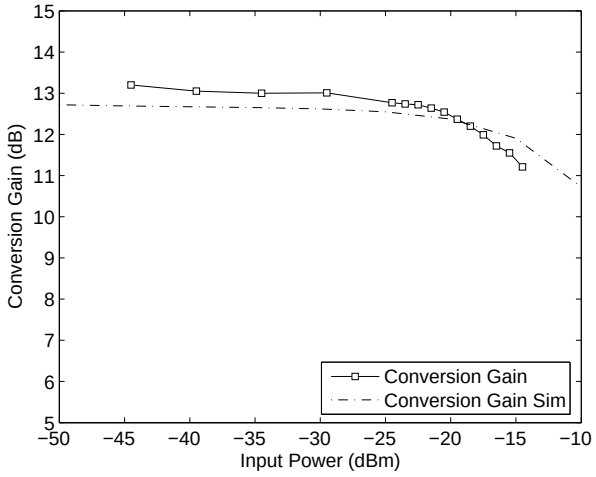

Figure 5: Measured and simulated conversion gain.

on wafer with the use of two differential CPW probes and one GSG CPW probe for the single-ended IF output. The LO input power was set to 0 dBm. The RF power was swept and the output power of the mixer was measured using a spectrum analyzer. Fig. 4 shows the measured output power versus input power and the measured input-referred 1-dB compression point (IP_{1dB}) is −17.8 dBm, while the output-referred 1-dB compression point (OP_{1dB}) is −5 dBm. Fig. 5 shows the measured conversion gain of the mixer to be 13.1 dB, which is very close to the simulated gain of 12.76 dB. The single-sideband (SSB) noise figure was measured and after de-embedding the loss and noise from the input balun, the SSB noise figure is found to be 7.8 dB. It should be noted that the noise from the buffer was included in the measurement. The SSB noise figure of the mixer block alone should thus be smaller than 7.8 dB.

Shown in Fig. 6 is the measured input reflection coefficient. Due to unwanted coupling between the gate inductors, the frequency for best match drifted upwards. Nevertheless, at 5.4 GHz, the measured S11 is −11.1 dB. Good port-to-port isolation was achieved by making the layout as symmetric as possible. The LO-to-RF feedthrough was measured, and it is −61.8 dB. To measure the third-order intercept point (IP3), a two-tone test was conducted with the signals separated by 1 MHz. Fig. 7 includes both the measured IF and intermodulation output powers. The input-referred IP3 is −6.2 dBm and the output-referred IP3 is +6.9 dBm.

The entire chip was biased from a single DC voltage power supply, V_{DD}, of 2 V. No current mirrors were used on-chip. The complete mixer including the output buffer consumes 31 mA, while the mixer core only consumes 18 mA of current. Fig. 8 shows a microphotograph of the complete chip.

4. CONCLUSIONS

In this paper, a design guideline was proposed and a fully integrated low-noise mixer in 180 nm CMOS technology was presented. Both PCSNIM and current-bleeding techniques were used in the design to reduce the noise figure while hav-

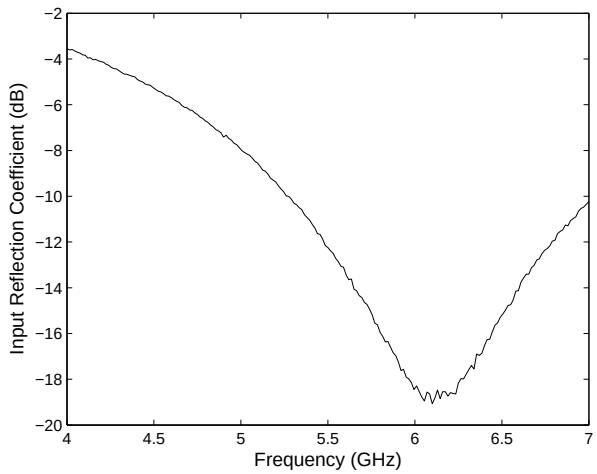

Figure 6: Measured reflection coefficient at the RF input port.

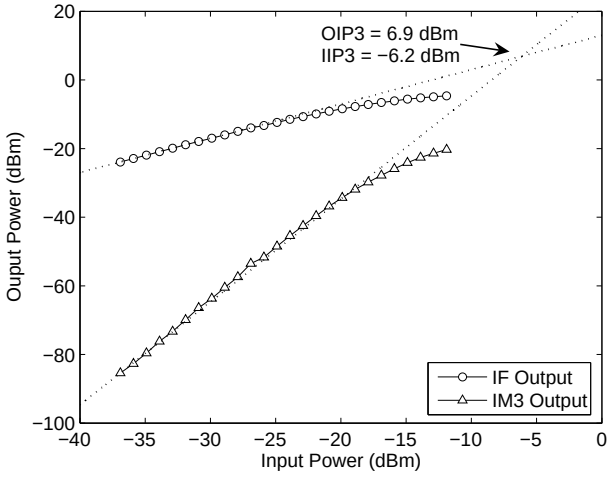

Figure 7: Measured IF and third order intermodulation product outputs.

ing a reasonable gain. The mixer works at 5.4 GHz with a 300 MHz IF and has a power conversion gain of 13.1 dB, a low 7.8 dB SSB noise figure, and an IIP3 of −6.2 dBm. The mixer core itself only consumes 18 mA from a 2.0 V supply and the complete test circuit consumes 31 mA.

5. ACKNOWLEDGMENTS

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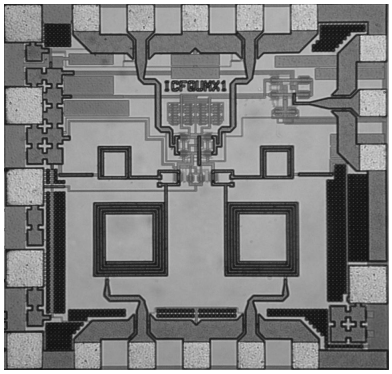

Figure 8: Microphotograph of the complete low-noise mixer chip.

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