A CMOS wideband front-end chip using direct RF sampling mixer with embedded discrete-time filtering

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Abstract: A CMOS wideband front-end IC is demonstrated in this paper. It consists of a low noise transconductance amplifier (LNTA) and a direct RF sampling mixer (DSM) with embedded programmable discrete-time filtering. The LNTA has the features of 0.5–6 GHz wideband, wideband input matching and low noise. The embedded filter following the DSM operates in discrete-time charge domain, filtering the aliasing signals and interferences while controlling the IF bandwidth according to the clock frequency. The measured NF of the front-end was below 7 dB throughout the whole band from 0.5 to 6 GHz. It shows a conversion gain of 12.6 dB and IP_{1dB} of −7.5 dBm at 2.4 GHz. It occupies a chip area of 0.23 mm^2 and consumes 14 mA DC current.

Key words: wideband front-end; LNTA; DSM; discrete time; FIR filtering; IIR; windowed integration
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1. Introduction

The trend of future radio receivers is to have the flexibility and programmability to accommodate various wireless standards. So the receiver has to fulfill the different requirements of bandwidth and dynamic range in each standard while still maintaining a high degree of integration[1−4].

Commercial CMOS technology has been proven to be most suitable for integrating both the RF/analog front-end and the digital baseband functions on the same chip. However, the recent low-cost digital sub-micron CMOS processes are not especially optimized for RF/analog circuits. At the same time, due to the increasingly enhanced performance of digital signal processing, it is beneficial to transform the RF and analog circuit design complexity to the digital domain. Direct RF sampling techniques allow great flexibility in reconfigurable radio design. They can also relieve the requirement for the ADC, and reduce cost and power consumption.

As the CMOS process advances, the dropping in supply voltage limits the headroom in analog circuits, which gives rise to poor linearity or bad conversion gain at a reasonable power consumption. The direct RF sampling and build-in filtering process signal in discrete time and charge domain, which requires low headroom for operation. This is one of the solutions to relax the tradeoff between low voltage design and high linearity requirement[5]. A sub-sampling technique is used to sample the IF or directly RF signal prior to the A/D conversion, which relieves the bandwidth constraints and decreases the power consumption in the subsequent circuits by lowering their sampling frequency. In addition to the wanted signal, subsampling will also lead to unwanted aliasing of out-of-band signals and wideband noise present at the front-end of the sampler, if the input bandwidth of the sampler is not strictly limited by a bandpass anti-aliasing filter. Due to their modest dynamic range, especially bad noise performance, the use of conventional simple sub-sampling circuits has usually been avoided in demanding wireless applications. Furthermore, charge sampling has some advantages over conventional voltage sampling. In voltage sampling, the bandwidth of the sample and hold system may be limited by the value of the on-resistance and capacitance. However, charge sampling doesn't track the signal voltage but integrates the current into the sampling capacitor. The transconductor can provide an almost constant output current up to GHz to charge the sampling capacitor. And the value of the capacitance could be so large that both noise and clock/charge feedthrough would be reduced[6].

In RF-CMOS technology, attention is currently focused on digital RF processors (DRP), which integrate RF circuits and digital baseband circuits on a single chip, transfer some RF/analog functions to the discrete-time domain, and provide comprehensive user programmability. In DRP technology, the direct sampling mixer (DSM) in the discrete time performs the functions of down-conversion, decimation and filtering. Down-conversion is performed by charge sampling. Decimation and filtering are performed by the embedded switched capacitor filter (SCF). Operation of the ADC is eased by decimation[7]. In this paper, as shown in Fig. 1, a front-end prototype integrating the LNTA, DSM, discrete-time filtering and multiphase clock generator is demonstrated. The technique of direct RF sampling mixer with embedded discrete-time filtering is explored for wideband application.

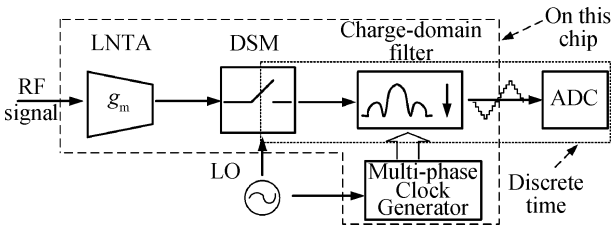

Fig. 1. The system diagram of the front-end.

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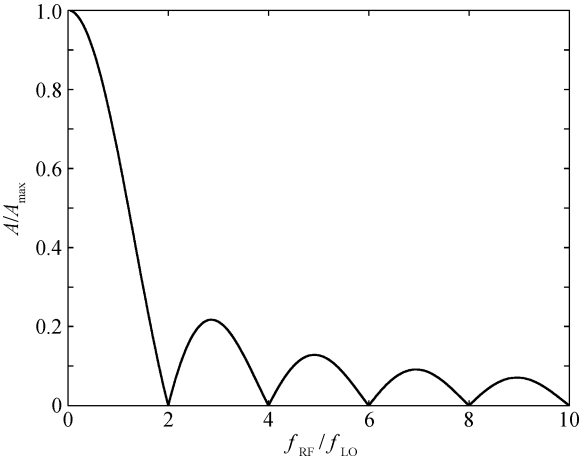

Fig. 2. Transfer function of the charge sampling mixer.

2. Charge sampling with embedded filtering function

A signal can be sampled by integrating its current in a given time window[6]. When a sinusoidal current signal $I_i \sin(\omega_i t + \phi_i)$ is gated by a switch and integrated into a sampling capacitor C_s during the time period from t_1 to t_2, the total integrated charge from t_1 to t_2 is

$$Q_i = (I_i/\omega_i)[\cos(\omega_i t_1 + \phi_i) - \cos(\omega_i t_2 + \phi_i)], \quad (1)$$

if t_s is the center time of the sampling window, and $2\Delta t = t_2 - t_1$ is the width of the sampling window, then

$$Q_i = 2\Delta t[\sin(\omega_i \Delta t)/(\omega_i \Delta t)] I_i \sin(\omega_i t_s + \phi_i), \quad (2)$$

where $I_i \sin(\omega_i t_s + \phi_i)$ is the instant value of the input signal at t_s and $2\Delta t[\sin(\omega_i \Delta t)/(\omega_i \Delta t)]$ is a frequency dependent coefficient. When the RF current is the output of a transconductor with the transconductance of g_m and the switch is controlled by the LO ($2f_{LO} = \frac{1}{2\Delta t}$), the integrated charge of a single LO half-cycle becomes

$$Q_i = \frac{1}{2f_{LO}} \frac{\sin\left(\frac{\pi}{2} f_{RF}/f_{LO}\right)}{\frac{\pi}{2} f_{RF}/f_{LO}} g_m V_{in}, \quad (3)$$

and the voltage gain is

$$G_{v,RF} = \frac{Q_i \frac{1}{C_s}}{V_{in}} = \frac{\sin\left(\frac{\pi}{2} \frac{f_{RF}}{f_{LO}}\right)}{\pi f_{RF}} \frac{g_m}{C_s}. \quad (4)$$

Figure 2 plots the normalized transfer function of Eq. (4). It is found that most power of the signal can pass through around the LO frequency and the power will be totally null around even multiples of LO frequency.

Continuously integrating N half-rectified RF samples results in a finite-impulse response (FIR) operation with N all-one coefficients, also known as moving-average (MA)[1]. Its time-domain expression and frequency response are listed below,

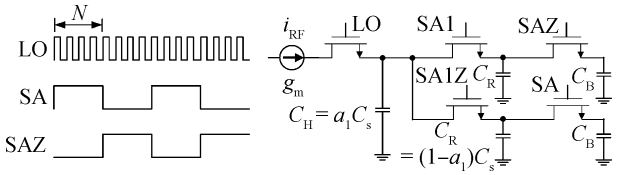

Fig. 3. Discrete-time filtering operation.

$$Q_{MA,i} = \sum_{l=0}^{N-1} Q_{i-l},$$

$$|H_{MA}(f)| = \left| \frac{\sin(\pi f N/f_{LO})}{\sin(\pi f/f_{LO})} \exp\left(-j \frac{N-1}{2} \frac{2\pi f}{f_{LO}}\right) \right|, \quad (5)$$

where Q_i is the ith RF sample and $Q_{MA,i}$ is the accumulated charge. The sinc transfer function shows notches at frequencies of $m\frac{f_{LO}}{N}$, where $m = 1, 2, s$. The sampling rate is decimated by N and the voltage gain equals N.

The charge $Q_{MA,i}$ is distributed between the history capacitor C_H and the rotation capacitor C_R, which together comprise the sampling capacitor, as shown in Fig. 3. In the next period, the charge stored in C_H will be preserved while the charge in C_R will be ready to read out. During the $(j-1)$th integrating period including N RF samples, the total charge stored in the system is $Q_{MA,j-1}$. Therein, $a\,Q_{MA,j-1}$ is preserved in C_H and $(1-a_1)Q_{MA,j-1}$ is stored in C_R, where $a_1 = \frac{C_H}{C_H+C_R}$. In the next j-th integrating period, additional variation charge $Q_{IIR1,j}$ is further stored in the system according to the input RF current, so the total charge in the j-th integrating period can be written as

$$Q_{MA,j} = a_1 Q_{MA,j-1} + Q_{IIR1,j}. \quad (6)$$

The charge recursive operation results in the capacity of infinite-impulse response (IIR) filtering[8], and the transfer function is found to be

$$G_{v,IIR1} = \frac{v_{out}}{v_{in}} = \frac{(1-a_1)Q_{MA,j}}{C_R} \times \left(\frac{Q_{IIR1,j}}{C_H + C_R}\right)^{-1},$$

$$|H_{IIR1}(f)| = \left| \frac{1}{1 - a_1 \exp\left(-j \frac{2\pi N f}{f_{LO}}\right)} \right|. \quad (7)$$

This discrete-time IIR filter operates at a f_{LO}/N sampling rate and introduces a single pole with attenuation of 20 dB/dec. IIR has better filtering than FIR, but the decimation normally leads to an aliasing problem, which can be minimized by the preceding MA filter. The equivalent pole in the continuous-time domain is located at $f_{c1} = \frac{1}{2\pi} \frac{f_{LO}}{N} \frac{C_R}{C_H+C_R}$ for $f_{c1} \ll f_{LO}/N$.

If the sampling rate remains too high and further decimation is needed, redundant C_R capacitors should be added and paralleled with the original ones. Input charge cyclically integrating in the parallel bank of C_R's by the non-overlapping multi-phase clocks creates additional spatial MA filter[9].

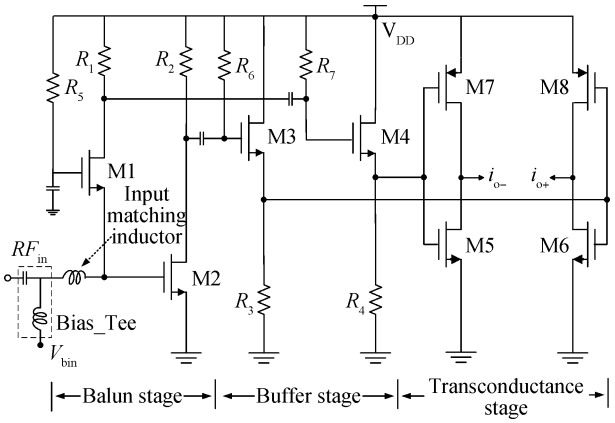

Fig. 4. Schematic of LNTA.

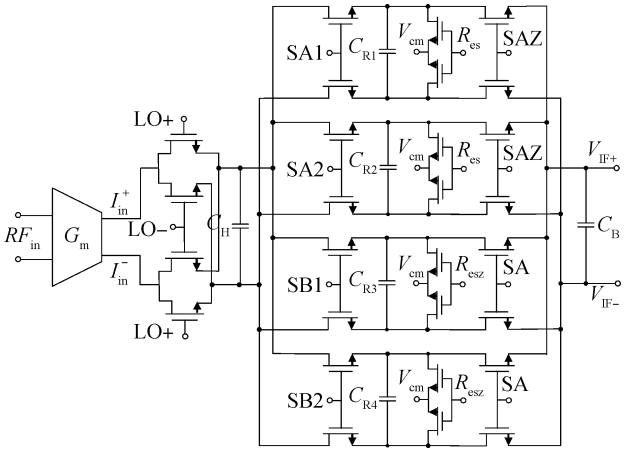

Fig. 5. Schematic of the sampling mixer with discrete-time filtering.

3. Circuit design

The discrete-time charge-domain sampling filter has been separately designed for IF receivers[5, 7] and used in an RF wideband SDR receiver following the passive mixer stage[3]. However, in direct RF sampling mixer architecture, discrete-time analog signal processing techniques are used to sample the RF input signal directly, which is down-converted, down-sampled and filtered by the DSM with an embedded filter. This method achieves a great selectivity right at the mixer level. The selectivity is digitally controlled by the frequency ratio of the LO and clock ($\frac{f_{\rm CLK}}{f_{\rm LO}}$) and by the capacitance ratio of the sampling capacitors ($\frac{C_{\rm R}}{C_{\rm H}}$). Both of the ratios are extremely precise, even in deep-submicron CMOS processes. This technique has been employed in single-band or dual-band RF receivers[1, 8]. In this paper, we will explore its application in the proposed wideband front-end. As shown in Fig. 1, the received RF signal is converted from voltage domain to RF current by the wideband LNTA. The RF current is then switched by the LO and window-integrated into the sampling capacitors. Through the subsequent moving average and charge rotation, the FIR and IIR filtering are achieved while anti-aliasing and out-of-band filtering are performed. Except for the LNTA stage, the following circuits are all passive. The switches and capacitors can handle large signals, especially in the charge domain. So the linearity will be improved and mainly depends on the LNTA stage.

3.1. LNTA

A schematic of the LNTA is shown in Fig. 4. To accommodate an RF signal from 500 MHz to 6 GHz, a wideband LNTA stage is necessary, given that the following direct sampling mixer is usually not band-limited. Due to the single-ended characteristic of the antenna or first stage of the receiver, an active balun is preferred and integrated here. Common-gate common-source topology is employed due to its virtues of wideband input matching and canceling of both noise and nonlinearity. To achieve low noise performance, R_1 is chosen to be 3 times R_2 while $g_{\rm m,M2}$ is 3 times $g_{\rm m,M1}$[10]. The third stage is a complementary transconductor. To obtain a sufficient transconductance from the stage, the sizes of the NMOS (M5/M6) and PMOS (M7/M8) transistors are large. If the transconductor follows after the balun directly, the big difference in the time constant ($R_1C_{\rm in} \neq R_2C_{\rm in}$) at the interface will make the phase and magnitude imbalances degrade severely toward the high frequency of the band. To alleviate this problem, a source follower buffer is inserted between the balun stage and the transconductance stage. The 1 nH input matching inductor indicated in Fig. 4 is to simulate the inductive effect of the bonding wire, which also improves the input matching at high frequencies.

3.2. DSM

A schematic of the sampling mixer is shown in Fig. 5. The waveforms of the clocks used in this section are shown in Fig. 7. The RF current is switched by the LO signal and integrated into the sampling capacitors $C_{\rm H}$ and $C_{\rm R}$, which forms the charge sampling. To reduce and stabilize the on-resistance of the LO switches even under large input signal conditions, the complementary CMOS switches are used here. Furthermore, the larger the sampling capacitor used in the circuit, the lower the sampling noise and clock feedthrough[11].

Clocks $\rm SA_{1,2}$, $\rm SB_{1,2}$ have non-overlapping time windows that let successive N samples be integrated into the sampling capacitors, which performs moving average and results in FIR filter mainly for anti-aliasing filtering. Distributing the integrated charge between $C_{\rm H}$ and $C_{\rm R}$ at a rate of $f_{\rm LO}/N$ gives rise to a IIR1 filter. To prevent the IIR filter from limiting the IF bandwidth, the ratio between the sampling capacitor and the rotating capacitor $C_{\rm H}/C_{\rm R} = 6$ pF/10 pF is not chosen to be too large in order to have the potential to tune the bandwidth from hundreds of kHz to tens of MHz. Non-overlapping clocks $\rm SA_{1,2}$ successively transfer the charge into the parallel $C_{\rm R1}$ and $C_{\rm R2}$, which realizes additional decimation by 2 , i.e. the 2nd order spacial moving average. Of course, more branches can be parallelized to get better FIR filtering. Here is just a demonstration of the techniques.

The combination charge stored in $C_{\rm R1}$ and $C_{\rm R2}$ is read out into the output buffer capacitor $C_{\rm B}$ at an even lower rate $f_{\rm LO}/2N$ switched by a clock SA/SAZ. Assuming the total charge stored in $C_{\rm R1,2}$ and $C_{\rm B}$ at read-out moment is $Q_{{\rm FIR2},j}$, then the output charge is $\frac{C_{\rm B}}{2C_{\rm R}+C_{\rm B}}Q_{{\rm FIR2},j}$. If every time the new input charge obtained by $C_{\rm R1,2}$ is $Q_{{\rm IIR2},j}$, then the difference

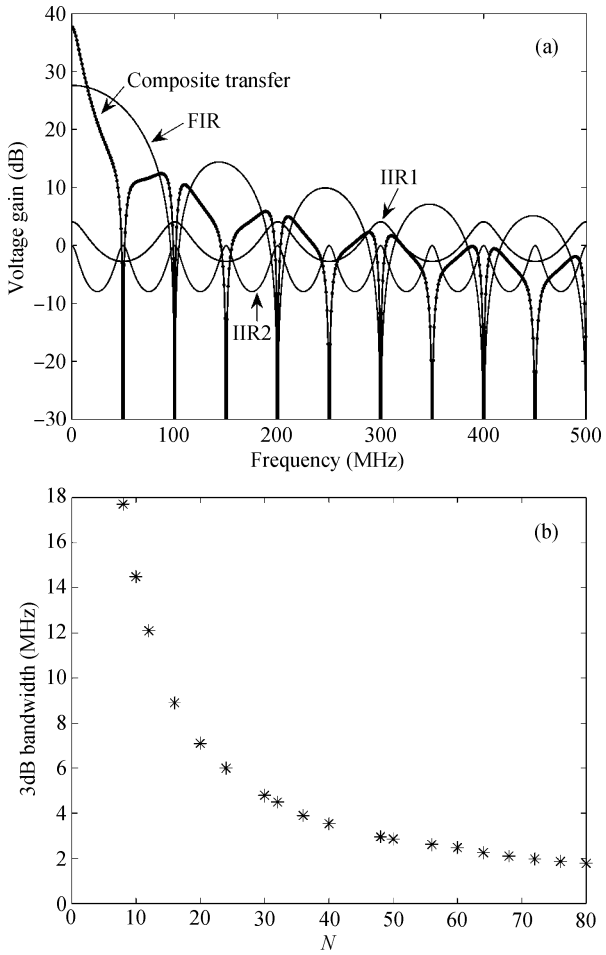

Fig. 6. The amplitude-frequency response of the composite transfer function of the discrete-time filters, including (a) FIR and IIR filters, and (b) the relation between 3 dB bandwidth and N.

equation and transfer function can be expressed as

$$Q_{\mathrm{FIR2},j} = Q_{\mathrm{IIR2},j} + \frac{C_{\mathrm{B}}}{2C_{\mathrm{R}} + C_{\mathrm{B}}} Q_{\mathrm{FIR2},j-1}, \tag{8}$$

$$G_{\mathrm{v,IIR2}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{\dfrac{C_{\mathrm{B}}}{2C_{\mathrm{R}} + C_{\mathrm{B}}} Q_{\mathrm{FIR2},j} \dfrac{1}{C_{\boldsymbol{B}}}}{\left(Q_{\mathrm{FIR2},j} - \dfrac{C_{\boldsymbol{B}}}{2C_{\boldsymbol{R}} + C_{\boldsymbol{B}}} Q_{\mathrm{FIR2},j-1}\right) \dfrac{1}{2C_{\boldsymbol{R}}}}, \tag{9}$$

$$|H_{\mathrm{IIR2}}(f)| = \left| \frac{1 - a_2}{1 - a_2 \mathrm{e}^{-j\frac{2N2\pi f}{f_{\mathrm{LO}}}}} \right|_{a_2 = \frac{C_{\mathrm{B}}}{2C_{\mathrm{R}} + C_{\mathrm{B}}}}. \tag{10}$$

The amplitude-frequency response of the composite transfer function of the discrete-time filters including FIR and IIR filters in this design are shown in Fig. 6(a) when LO = 2.4 GHz and $N = 24$. The theoretical relation between its 3 dB bandwidth and the $f_{\mathrm{LO}}/f_{\mathrm{CLK}}$ ratio N is derived from the composite transfer function and shown in Fig. 6(b). This will help us to set the bandwidth according to different protocols.

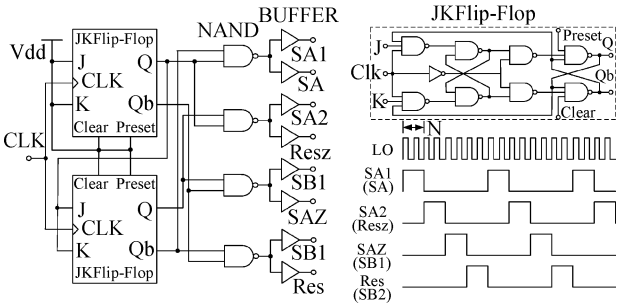

Fig. 7. Circuit block of the clock generator and clock diagram.

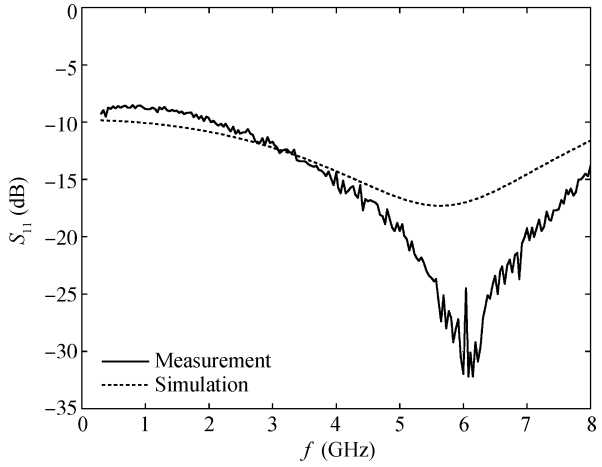

Fig. 8. Input matching of LNTA.

Afterwards, C_{R1} and C_{R2} are discharged by reset clock R_{es}. They are reset to a common voltage of V_{cm}, which is at the same level as the DC common output voltage of the transconductor stage to prevent DC current from flowing through the sampling mixer and the discrete-time filter in order to eliminate the flicker noise. Meanwhile, V_{cm} also provides a DC common input voltage to the following stage so that the large AC couple capacitors and related biasing circuitry are spared. Additionally, C_{H}, C_{R} and C_{B} are connected between the two differential paths instead of connecting one of their terminals to ground to reduce the number of capacitors needed and save capacitance area by a factor of 4. At the same time, they are composed of a pair of inversed capacitors to remove the non-symmetrical effect with respect to the top and bottom plates of the capacitor.

3.3. Multi-phase clock generator

A schematic of the multi-phase clock generator is shown in Fig. 7. The divide-by-4 function is performed by two J–K flip flops. The master-slave architecture for the J–K flip flop is chosen due to its stability. The output combination logic consisting of the nands and buffers processes the divide-by-2 and divide-by-4 outputs from the two J–K flip flops and generates four non-overlapping multi-phase clocks. To simplify the circuitry and design complexity, the clocks are elaborately designed to be multiplexed.

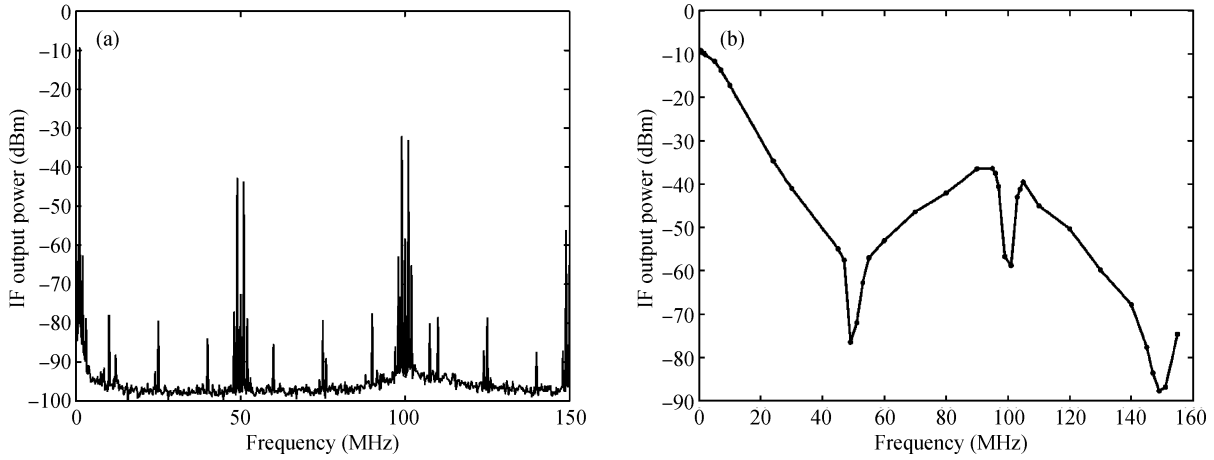

Fig. 9. (a) IF output spectrum @ LO = 2.4 GHz, IF = 1 MHz, Pin = −21.6 dBm and CLK = 100 MHz. (b) Filtering characteristic when sweeping the IF from 500 kHz to 150 MHz.

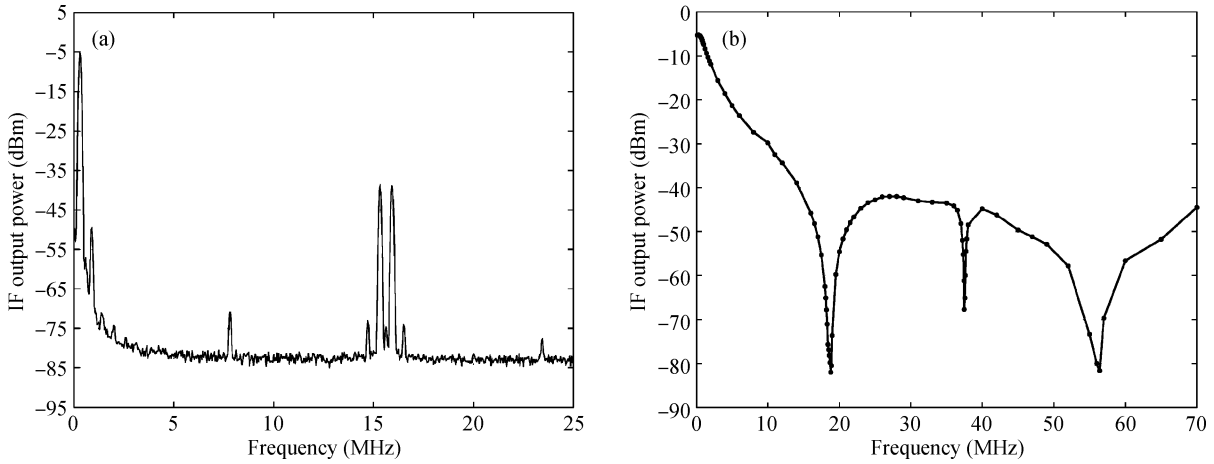

Fig. 10. (a) IF output spectrum @ LO = 2.4 GHz, IF = 0.3 MHz, Pin = −21.6 dBm and CLK = 37.5 MHz. (b) Filtering characteristic when sweeping the IF from 100 kHz to 70 MHz.

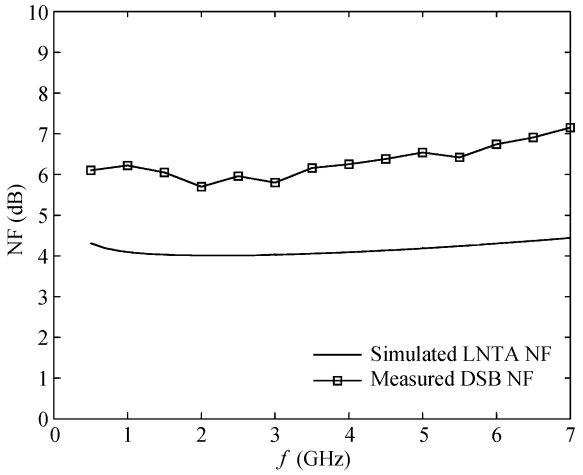

Fig. 11. Measured NF @ IF = 500 kHz, clk = 100 MHz.

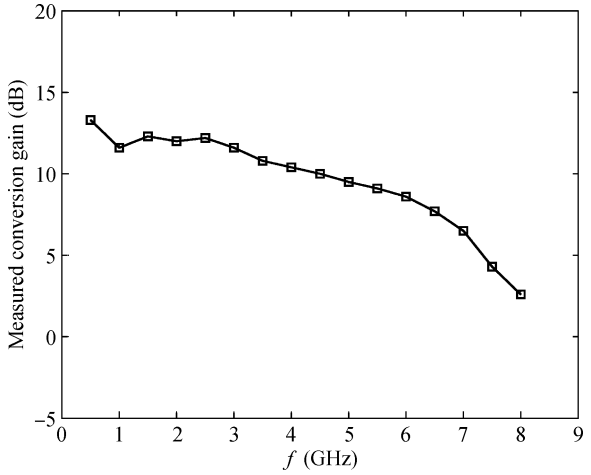

Fig. 12. The wideband performance of the front-end.

4. Measurement results

This front-end prototype has been fabricated in a 0.13 μm CMOS process and tested on wafer. The input matching of LNTA is shown in Fig. 8. The worst measured S_{11} is −8.5 at low frequency end.

The IF output spectrum is measured by Agilent E4446A Spectrum Analyzer and shown in Fig. 9(a). It was measured

Table 1. Performance summary and comparison table

Reference	Technology	Freq. band (GHz)	NF (dB)	Linearity (dBm)	Power (mW)
This work	0.13 μm CMOS charge sampling	0.5−6	6 (DSB)	IIP_3: + 3.2 [a] IP_{1dB}: − 7.5	16.8
Ref. [3]	90 nm CMOS charge sampling	0.8−6	5	IIP_3: − 3.5 [b] —	36.5 [d]
Ref. [12]	0.18 μm CMOS voltage subsampling	DC−3.5	15 (Min)	— IP_{1dB}: − 11 [c]	21.6

Frequency & gain settings: [a] 2.4 GHz 12.5 dB, [b] GSM 900 MHz mid-gain, [c] 500 MHz 12 dB, [d] GSM low gain setting.

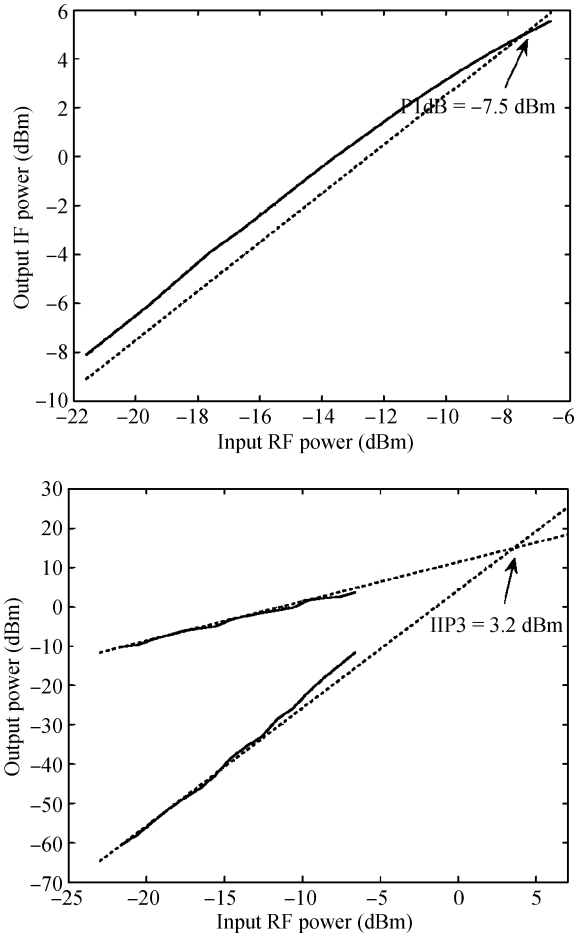

Fig. 13. Measured (a) IP_{1dB} and (b) IIP_3 at LO = 2.4 GHz, $N = 24$.

under the condition of LO = 2.4 GHz, IF = 1 MHz, Pin = −21.6 dBm and CLK = 100 MHz ($N = 24$). According to the theory analysis above, the theoretical conversion gain at DC IF should be

$$G_{v,IF,DC} = \frac{1}{\pi}\frac{1}{f_{LO}}\frac{g_m}{C_s} \times N \times \frac{1}{1-a_1} \times 1 = \frac{1}{\pi}\frac{1}{2.4\ \text{GHz}}\frac{30\ \text{mS}}{16\ \text{pF}} \times 24 \times \frac{1}{1-6/16} \times 1 = 19.6\ \text{dB}. \quad (11)$$

The measured gain at 1 MHz IF is 12.5 dB with 7.1 dB degradation due to all the nonideal factors, such as transconductance degradation, parasitic effects and charge leakage. The large clock signal also converses the IF signal to around 100 MHz, which is 22.5 dB lower than the IF signal of interest at 1 MHz. Because the 2nd order parallel moving average was employed, the aliasing IF signal will also appear at around 50 MHz.

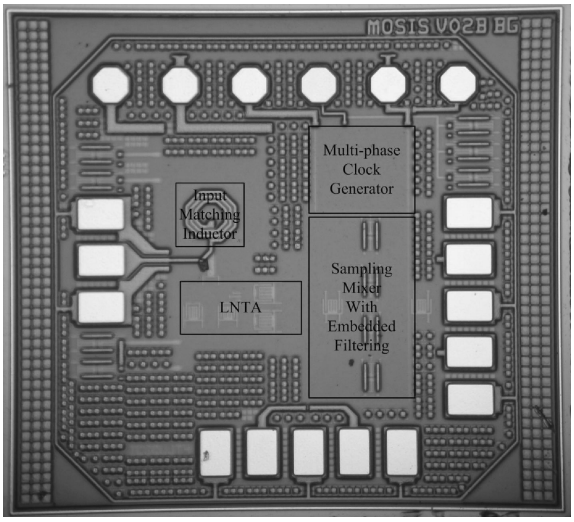

Fig. 14. Chip photograph indicating each building block.

If we sweep the RF input frequency from 2.4005 GHz to 2.55 GHz, which results in a IF frequency from 500 kHz to 150 MHz, then the filtering characteristic of the whole sampling mixer is obtained. Figure 9(b) shows the measurement result of filtering. The 3 dB IF bandwidth is at about 5.4 MHz. The characteristic of the filtering is consistent with the theoretical analysis in Fig. 6(a). The IF output spectrum when changing the clock frequency to 37.5 MHz ($N = 64$) is shown in Fig. 10(a). The measured IF filtering response is shown in Fig. 10(b). The gain and 3 dB bandwidth were tested at 16.4 and 1.2 MHz, respectively.

The noise figure (NF) measured at IF = 1 MHz is shown in Fig. 11, compared with the simulated NF of LNTA. Because the noise parameter γ of the technology employed is as high as 2.5, the NF of the LNTA stage is above 4 dB. The overall NF is below 7 dB up to 6 GHz, as shown in Fig. 11. The wideband performance of the sampling mixer is obtained and shown in Fig. 12, when the RF frequency is swept from 500 MHz to 8 GHz at IF = 1 MHz, $N = 24$. The 3 dB bandwidth is measured at 5 GHz.

The IP_{1dB} is −7.5 dBm measured at LO = 2.4 GHz and CLK = 100 MHz, while the IIP_3 is + 3.2 dBm, as shown in Fig. 13(a) and Fig. 13(b). The chip photograph is shown in Fig. 14 with indicated building blocks. The core chip occupies

an area of 0.23 mm^2. The chip consumes 14 mA DC current from a 1.2 V supply. Table I compares the key performances between the proposed and other wideband front-ends employing similar and different techniques.

5. Conclusion

A CMOS front-end prototype comprising an LNTA and a direct RF sampling mixer with embedded programmable switched capacitor filtering is demonstrated in this paper. The measured 3 dB bandwidth is up to 5 GHz. The NF of the front-end was measured below 7 dB throughout the whole band from 0.5 to 6 GHz. It shows a conversion gain of 12.6 dB and IP_{1dB} of -7.5 dBm at 2.4 GHz. It occupies a chip area of 0.23 mm^2 and consumes 14 mA DC current from a 1.2 V supply.

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