Broadband Low-Noise Amplifier With Fast Power Switching for 3.1–10.6-GHz Ultra-Wideband Applications

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***Abstract*—A novel fast switching noise-cancelling low-noise amplifier (LNA) is presented in this paper using 0.13-μm CMOS for 3.1–10.6-GHz ultra-wideband applications. A new noise-cancelling topology is employed to simultaneously achieve a sub-4-dB flat noise figure and a high gain of 16.6 dB for frequencies up to 10 GHz. Fast on and off power switching is achieved by bypassing the large dc-bias resistors that lead to long charging time constants, allowing the output voltage to settle within only 1.3 ns for switching frequencies as high as 200 MHz. The phase noise and jitter added by the switched LNA was characterized, and the measured output integrated rms jitter is about 750 fs from 10 Hz to 1 MHz, while the input integrated rms jitter is 420 fs. The circuit consumes 18 mW of dc power in the on state. When the circuit is switched on and off with a 50% duty cycle, the power consumption is less than 10 mW. It occupies an active chip area of less than 0.5 mm^2.**

***Index Terms*—CMOS integrated circuits, low-noise amplifiers (LNAs), microwave integrated circuits, switched circuits, ultra-wideband (UWB) technology.**

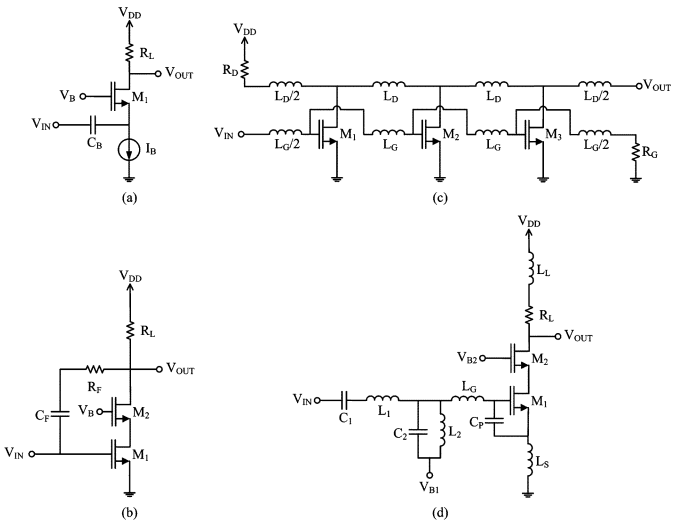

Fig. 1. Common wideband LNA topologies. (a) Common gate. (b) Shunt resistive feedback. (c) Distributed. (d) Passive input matching.

I. Introduction

IMPULSE ultra-wideband (UWB) technology employing short time duration impulses has drawn much attention from researchers and industry as it potentially offers several advantages, including high data rates, low power and complexity, reduced multipath fading, high time and range resolution, and low probability of undesired detection and interception. Energy-efficient and low-cost impulse UWB transceivers [1] are attractive for wireless communication and biomedical applications, such as wireless personal area networks (WPANs) [2]–[8], interchip communications [9]–[12], and UWB biotelemetry [13]–[15]. The low-noise amplifier (LNA) is an important component in UWB receiver front-ends, posing some serious challenges in circuit design. A low noise figure (NF) and a high gain are simultaneously required over a wide bandwidth, which causes the LNA to be the most power-hungry component in UWB receiver front-ends. Yet low circuit complexity is often necessary to reduce cost.

There are many different topologies commonly used for wideband LNAs, as shown in Fig. 1 [16]–[20]. Conventional wideband amplifiers, such as the common-gate amplifier or the common-source resistive shunt-feedback amplifier, often have difficulties in achieving a low NF while maintaining a good impedance match over a wide range of frequencies, or suffer from limited gain and stability. Distributed and traveling-wave amplifiers can provide a low NF, good impedance match, and flat gain over a very wide frequency bandwidth, but they can suffer from limited gain, consume a significant amount of power, or occupy a particularly large chip area. More recently, inductive degeneration and multisection inductor–capacitor (*LC*) networks have been reported for wideband noise and impedance matching. However, the insertion loss of the matching network in the input path degrades the NF rapidly as the frequency increases. Noise cancelling has been shown to be an effective approach for achieving a low NF and an impedance match simultaneously without the need for feedback. Nevertheless, the input voltage sensing and auxiliary amplifier stages used for noise canceling can contribute significant input-referred noise at high frequencies, thus degrading the NF.

The LNA is not required to operate continuously in pulsed UWB systems, but only when a pulse is being received. Thus, applying on and off switching can lead to significant power savings that might not be possible otherwise. However, the LNA must respond fast enough to the switching in order to be power efficient. In this paper, a novel fast switching noise-cancelling LNA is presented in 0.13-μm CMOS for 3.1–10.6-GHz UWB

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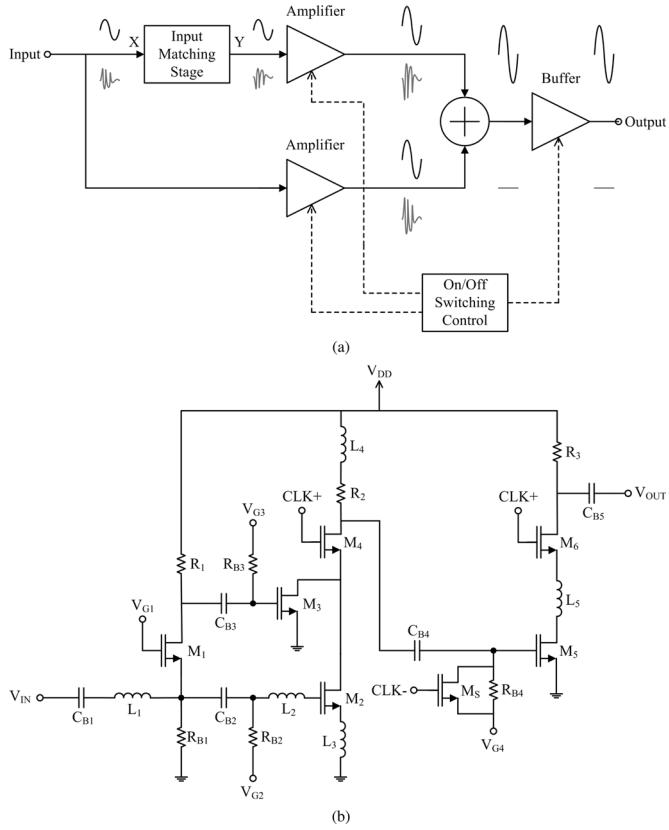

Fig. 2. Block diagram and circuit schematic of the proposed LNA.

applications. A new noise-cancelling topology is employed to simultaneously achieve a sub-4-dB flat NF and a high gain of 16.6 dB for frequencies up to 10 GHz. Fast switching is achieved by bypassing the large dc-bias resistors that lead to long charging time constants, allowing the output voltage to settle within only 1.3 ns for a switching frequency as high as 200 MHz. The jitter added by the switched LNA was characterized from the pulsed output phase noise, and the measured integrated rms jitter is about 750 fs from 10 Hz to 1 MHz. The circuit consumes less than 18 mW of dc power, and it consumes less than 10 mW of average power with a 50% duty-cycle clock. It occupies an active chip area of less than 0.5 mm^2.

II. Circuit Architecture and Design

In this study, a common-gate amplifier is used to provide a wideband input impedance match. Since a single-stage amplifier cannot provide sufficient gain, additional stages (i.e., common-source amplifiers) are added. These amplifiers contribute noise that will affect the NF. However, if they are used to cancel the output noise of the input matching device, as illustrated in Fig. 2(a), a lower NF can be achieved [21]–[23]. In addition, the amplifiers and the output buffer can be quickly switched on and off to save a significant amount of power.

A circuit schematic of the proposed LNA is shown in Fig. 2(b). Transistor M_1 and resistor R_1 form the common-gate amplifier that provides a wideband input impedance match. An inductor L_1 is connected in series with the source of M_1 to absorb the total parasitic capacitance appearing at this node and improve the input match at high frequencies. The output noise of the matching device (M_1) is cancelled using two other common-source amplifiers M_2 and M_3, as shown in Fig. 2(b). The noise current of M_1 $(i_{\rm ND1})$ flows out of the drain, but into the source creating two correlated noise voltages with opposite polarities, $V_D \approx -R_1 i_{\rm ND1}/(1+g_{M1}R_S)$ and $V_S \approx R_S i_{\rm ND1}/(1+g_{M1}R_S)$, respectively, where R_S is the signal source impedance (50 Ω) and g_{M1} is the transconductance of M_1. However, the signal voltages at these nodes are in phase. Thus, by amplifying the source and drain voltages using M_2 and M_3, respectively, and adding them together, the noise contribution of M_1 can be cancelled while the signal is added. It can be seen that the noise current $\overline{i_{o23}^2}$ at the combined output of M_2 and M_3 is given by

$$\overline{i_{o23}^2} = \overline{|g_{M2}V_S + g_{M3}V_D|^2} = \left(\frac{g_{M2}R_S - g_{M3}R_1}{1+g_{M1}R_S}\right)^2 \overline{i_{\rm ND1}^2} \tag{1}$$

where g_{M2} and g_{M3} is the transconductance of M_2 and M_3, respectively. Cancellation can thus be achieved if, to the first order, $g_{M2}R_S \approx g_{M3}R_1$. When this condition is met, the noise from the noisiest component of the LNA can be eliminated. Note that the noise generated by R_1 cannot be cancelled because it appears in phase at the drain and source nodes of transistor M_1. However, this noise contribution can be made small by using a sufficiently large resistance value for R_1.

After cancelling the output noise of matching device M_1, the noise generated by the common-source device M_2 dominates the NF of the LNA. The relatively large resistance value of R_1 and the gain provided by the common-gate amplifier M_1 reduce the noise contribution of the common-source amplifier M_3 [22]. The width, transconductance, and gain of M_2 can be made relatively large to reduce its noise contribution. However, this increases the gate–source $C_{\rm GS2}$ and gate–drain $C_{\rm GD2}$ parasitic capacitances diminishing the increase in gain and deteriorating the NF at high frequencies. To mitigate this effect, an inductor (L_2) is connected in series with the gate of M_2 to absorb its parasitic capacitance and increase the bandwidth. In addition, inductive degeneration is used at the source of M_2 (L_3). An equivalent small-signal model of M_2, L_2, and L_3 is illustrated in Fig. 3. It can be shown that the input impedance (Z_{i2}), effective transconductance (G_{M2}), input-referred noise current $(\overline{i_{\rm NI}^2})$, and input-referred noise voltage $(\overline{v_{\rm NI}^2})$ of the common-source amplifier M_2 are given by

$$Z_{i2} = \frac{g_{M2}L_3}{C_{\rm GS2}} + j\omega(L_2+L_3) - \frac{j}{\omega C_{\rm GS2}} \tag{2a}$$

$$G_{M2} = \frac{g_{M2}}{1-\omega^2 C_{\rm GS2}(L_2+L_3) + j\omega g_{M2}L_3} \tag{2b}$$

$$\overline{i_{\rm NI}^2} = \frac{\omega^2 C_{\rm GS2}^2}{g_{M2}^2}\overline{i_{\rm ND2}^2} \tag{2c}$$

$$\overline{v_{\rm NI}^2} = \frac{\left(1-\omega^2 C_{\rm GS2}(L_2+L_3)\right)^2}{g_{M2}^2}\overline{i_{\rm ND2}^2}. \tag{2d}$$

where $\overline{i_{\rm ND2}^2}$ is the drain–source noise current of M_2. Equation (2) indicates that L_2 and L_3 can increase G_{M2} and reduce $\overline{v_{\rm NI}^2}$ at high frequencies. This occurs while $\overline{i_{\rm NI}^2}$ remains unaffected. Therefore, the gain of the common-source amplifier M_2 can

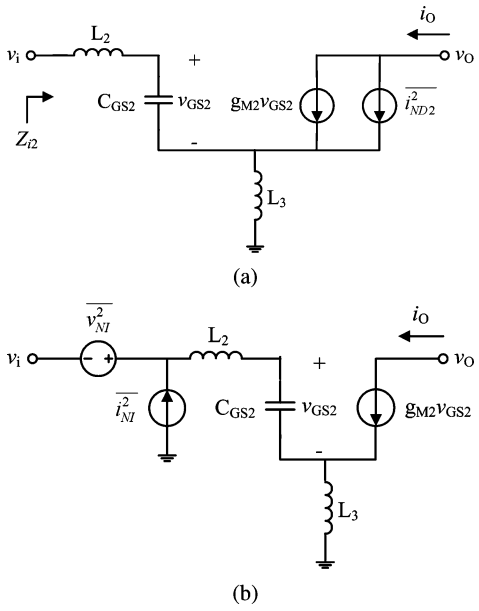

Fig. 3. Small-signal model of M_2 with L_2 and L_3. (a) Output drain–source noise current $\overline{i^2_{\rm ND2}}$ and (b) input-referred noise voltage $\overline{v^2_{\rm NI}}$ and current $\overline{i^2_{\rm NI}}$.

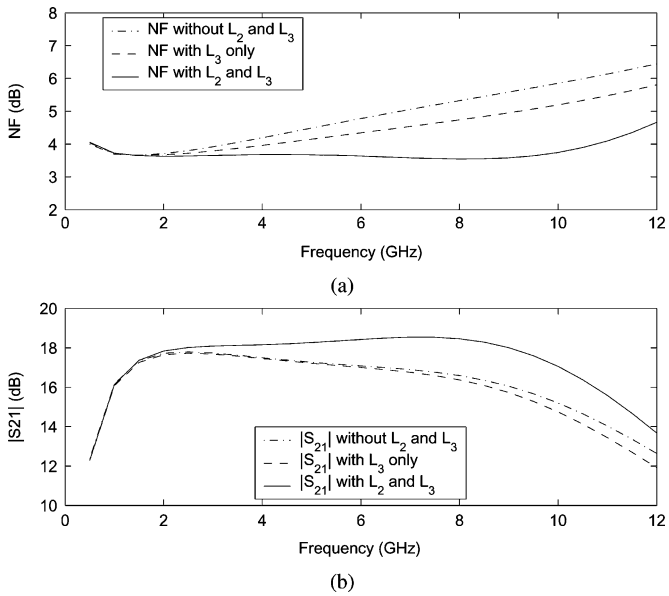

Fig. 4. Simulated LNA NF and gain $|S_{21}|$ with and without inductors L_2 and L_3.

be increased, while its total input-referred noise and NF contribution can be suppressed at high frequencies by using L_2 and L_3. Fig. 4 shows the schematic simulation results for the NF and gain $|S_{21}|$ of the LNA with and without the inductors L_2 and L_3. RF models provided by the foundry are used in this simulation for all devices shown in Fig. 2(b), including the transistors, on-chip spiral and line inductors, and metal–insulator–metal (MIM) capacitors, as they can predict their measured performance more closely. It is clear that the NF can be reduced by about 2 dB at high frequencies around 10 GHz using inductors L_2 and L_3. This is accompanied with an increase in gain of approximately 2 dB at 10 GHz.

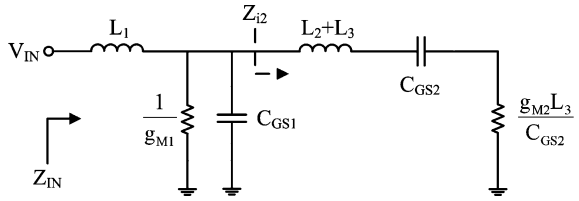

Fig. 5. Small-signal model of the input matching network.

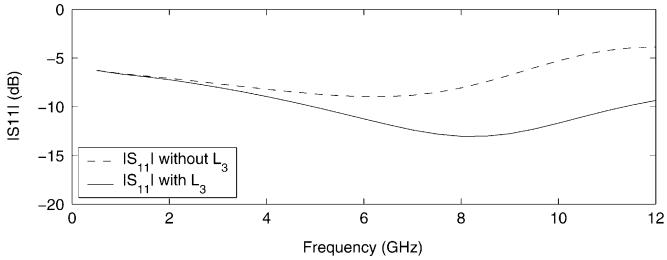

Fig. 6. Simulated LNA input reflection coefficient $|S_{11}|$ with and without inductor L_3.

The inductor L_3 is also used to provide a wideband input impedance match. Fig. 5 shows an equivalent small-signal model of the input network consisting of M_1, M_2, L_2, and L_3 from which the input impedance $Z_{\rm IN}$ can be written as

$$Z_{\rm IN} = j\omega L_1 + \frac{X - jY}{X^2 + Y^2} \tag{3}$$

where

$$X = g_{M1} + \frac{\omega^2 g_{M2} L_3 C_{\rm GS2}}{\omega^2 g_{M2}^2 L_3^2 + \left(1 - \omega^2 C_{\rm GS2}(L_2 + L_3)\right)^2} \tag{4a}$$

$$Y = \omega C_{\rm GS1} + \frac{\omega C_{\rm GS2}\left(1 - \omega^2 C_{\rm GS2}(L_2 + L_3)\right)}{\omega^2 g_{M2}^2 L_3^2 + \left(1 - \omega^2 C_{\rm GS2}(L_2 + L_3)\right)^2} \tag{4b}$$

and $C_{\rm GS1}$ is the gate–source parasitic capacitance of M_1. The inductance L_3 increases the real part of the input impedance $\mathrm{Re}\{Z_{\rm IN}\} = X/(X^2 + Y^2)$ and improves the input match at high frequencies. This also reduces the quality factor Q of the input network for a wideband input impedance match. The input impedance $Z_{\rm IN}$ is designed to be closest to the source impedance toward the higher end of the UWB band from 6 to 10 GHz, i.e., $\mathrm{Re}\{Z_{\rm IN}\} \approx R_S$ and $\mathrm{Im}\{Z_{\rm IN}\} \approx 0$. A good impedance match is also achieved in the lower end of the UWB band from 3 to 5 GHz due to the low quality factor and broadband frequency response of the input network. Fig. 6 shows the schematic simulation result for the input reflection coefficient $|S_{11}|$ of the LNA with and without the inductor L_3. It is clear that the input matching can be improved by about 6 dB at 10 GHz.

The quality factor (Q) of inductors L_1, L_2, and L_3 is important for a low parasitic resistance and a low NF, especially since they appear in the input matching network of the LNA. From the RF models provided by the foundry, the Q of these inductors is more than 10 and 16 at 3 and 10 GHz, respectively. The increasing Q from 3 to 10 GHz is useful to compensate for the lower gain and higher input-referred noise of devices M_1, M_2,

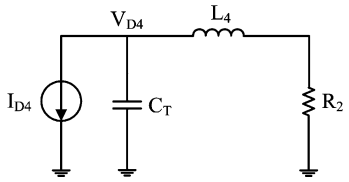

Fig. 7. Two-pole shunt inductive peaking network.

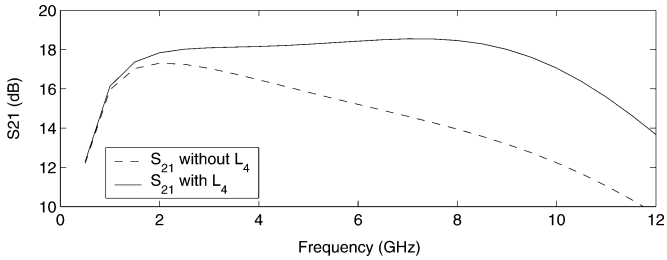

Fig. 8. Simulated LNA gain $|S_{21}|$ with and without inductor L_4.

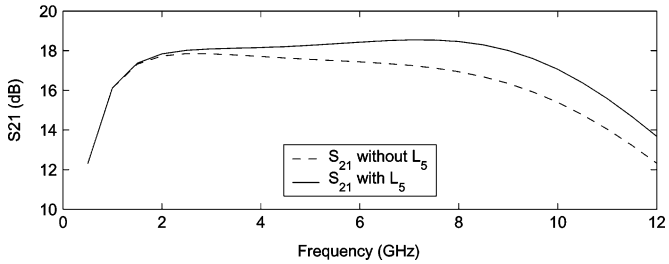

Fig. 9. Simulated LNA gain $|S_{21}|$ with and without inductor L_5.

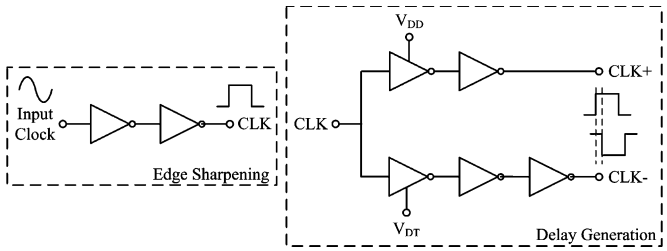

Fig. 10. Clock edge sharpening and delay generation circuits.

and M_3 at higher frequencies and to obtain a flat low NF over the UWB band.

The biasing current of the common-source amplifiers M_2 and M_3 is switched on and off by cascoding a second common-gate device M_4 at their outputs, which are connected together for signal combination. This cascode device also acts as a current buffer to reduce the Miller effect, improve the high-frequency response, and increase the reverse isolation. Shunt inductive peaking (L_4) is employed at the drain of M_4 to increase the bandwidth. Inductive peaking can be intuitively explained from the time-domain step response of the circuit shown in Fig. 7. Without the inductor L_4, the charging time constant for the voltage at the drain of M_4 (v_{D4}) would be $\tau \approx R_2 C_T$, and the voltage rise time from 10% to 90% would be $t_r \approx 2.2\tau$, where R_2 is the load resistance and C_T is the total parasitic capacitance seen at the drain of M_4. By adding the inductance L_4, as shown in Fig. 7, the load resistance R_2 can be decoupled from the output loading capacitance C_T, to force all of the available charging current from M_4 to flow into the capacitance C_T. This reduces the charging rise time t_r of the drain voltage v_{D4}, which implies an increase in the frequency bandwidth. Fig. 8 shows schematic simulation results for the gain $|S_{21}|$ of the LNA with and without the inductor L_4. It is clear that the gain can be increased by about 5 dB at high frequencies around 10 GHz using inductor L_4.

A second amplification stage M_5 is added (ac coupled) to increase the gain to more than 16 dB and provide an output impedance match from 3 to 10 GHz. The biasing current of the common-source amplifier M_5 is switched on and off using the cascode common-gate device M_6, which also reduces the Miller effect for a wider bandwidth. An inductor (L_5) is connected between the drain of M_5 and source of M_6 to absorb the parasitic capacitances at these nodes and further extend the bandwidth. Finally, the load resistance value of $R_{D3} = 67\ \Omega$ is chosen to provide a good broadband output impedance match when driving the 50-Ω load impedance of the measurement equipment. Fig. 9 shows schematic simulation results for the gain $|S_{21}|$ of the LNA with and without the inductor L_5. It is clear that the gain can be increased by about 1.7 dB at high frequencies around 10 GHz using inductor L_5. Inductors L_4 and L_5 have a high self-resonant frequency of more than 30 GHz for a constant inductance value from 3 to 10 GHz, which is important for obtaining a flat gain over the UWB band.

Fast switching can only be achieved by bypassing the large dc-bias resistor R_{B4} that leads to a long charging time constant of $\tau \approx R_{B4}C_{B4}$. An nMOS switch M_S is thus added in parallel to the dc-bias resistor R_{B4}, which is activated only for a short time period (0.8 ns) after startup. The nMOS device M_S is made sufficiently wide for a relatively small on-resistance R_{MS} to reduce the equivalent bias resistance $R_{MS}||R_{B4}$ during this short period of time. The output voltage amplitude can thus settle within 1.3 ns. A square-wave clock signal and its delayed inverse are created from the input sinusoidal clock, namely, CLK+ and CLK−, as shown in Fig. 10. The clock signal CLK+ is used to trigger the cascode transistors M_4 and M_6, while the delayed and inverted clock signal CLK− is used to activate the switch M_S. There is a short time period (0.8 ns) where CLK− is still held at logic high after the rising edge of CLK+, during which the switch M_S remains on to minimize the equivalent bias resistance and reduce the settling time after startup. CMOS inverters are used to sharpen the edges of the input clock, while current-starved CMOS inverters are used to generate the small delay of 0.8 ns between the clock signals CLK+ and CLK−.

Table I summarizes the transistor gate dimensions, inductor values, and resistor values used in the design of the proposed LNA.

III. Simulation and Measurement Results

The LNA was fabricated in a standard 0.13-μm CMOS process and a photograph of the integrated circuit (IC) is shown in Fig. 11. It occupies a die area of 1 mm^2 including bonding pads, decoupling capacitors, and the chip guard ring (plus

TABLE I
SUMMARY OF COMPONENT VALUES FOR THE LNA

Transistor	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_5$	$(W/L)_S$
Size	32/0.12	100/0.12	22/0.12	70/0.12	8/0.12
Inductor	L_1	L_2	L_3	L_4	L_5
Value	0.26 nH	1.4 nH	0.16 nH	1.2 nH	0.54 nH
Resistor	R_1	R_2	R_3	R_{B1}	R_{B2-4}
Value	680 Ω	100 Ω	67 Ω	1.3 kΩ	20 kΩ

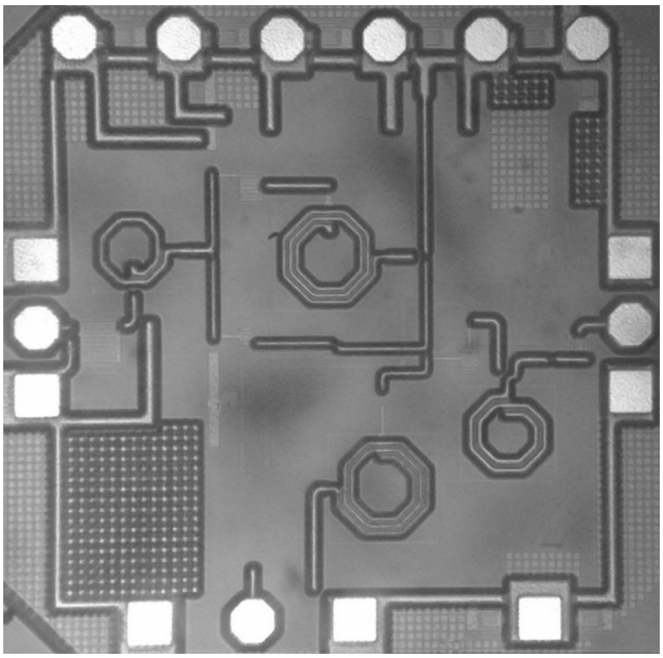

Fig. 11. Photograph of UWB LNA IC.

chamfer regions), while the core circuit area is $660 \times 760\ \mu\text{m}^2$. The circuit consumes less than 18 mW of dc or peak power, while it consumes less than 10 mW of average power (P_{AVG}) at a clock frequency of 100 MHz. The LNA's power when switched off is also about 0.7 mW, which is significantly lower than the peak power consumption.

The UWB LNA IC was measured directly on-wafer using 40-GHz coplanar waveguide (CPW) probes and dc probes. A 50-GHz Agilent vector network analyzer (8510C VNA) was used for the S-parameter measurements, while a 50-GHz Agilent spectrum analyzer (E4448A) was used for NF, power spectrum, and phase-noise measurements. A 60-GHz Tektronix Digital Serial Analyzer (DSA8200) was also used to observe the output in the time domain.

Fig. 12 shows the measured two-port S-parameters and NF of the LNA in comparison with the post-layout simulation results. Both measurements and simulation have the same bias conditions, and there is good agreement between the measured and simulated results. Pre-drawn device layouts characterized and modeled by the foundry were used as is in this design to achieve the best model-to-hardware correlation. A full-chip extraction was also carried out using Assura RCX to predict the parasitics of the interconnects. It is clear that the transmission coefficient S_{21} and NF are quite flat from 3 m to 10 GHz at about

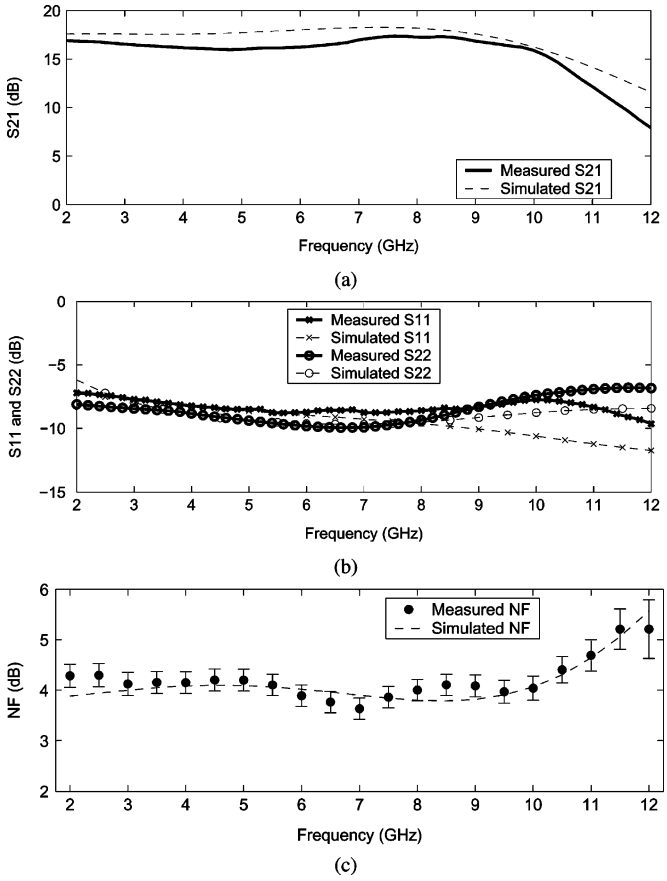

Fig. 12. (a) and (b) Measured LNA two-port S-parameters and (c) NF.

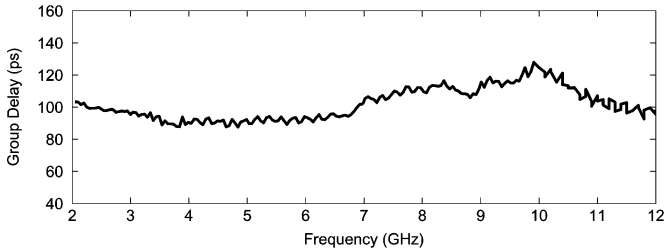

Fig. 13. Measured LNA group delay from 2 to 12 GHz.

16.6 ± 0.75 dB and 3.9 ± 0.28 dB, respectively. The NF measurement uncertainty in the 3–10-GHz frequency range is less than ± 0.24 dB and is depicted in Fig. 12(c) using error bars. The input and output reflection coefficients, S_{11} and S_{22}, are also below -8 and -7 dB, respectively, from 3 to 10 GHz. The input reflection coefficient can be enhanced by increasing the width, bias current, and transconductance of transistor M_1. A more effective approach is to add a common-source amplifier between the gate and source of M_1 to boost its effective transconductance G_{M1} [23], [24]. Alternatively, transistor M_2 can be reused for boosting the transconductance of M_1 instead of using an additional common-source amplifier, by ac coupling the drain of M_2 to the gate of M_1. The measured group delay is shown in Fig. 13, which depicts an average value of 105 ps with a small variation of ± 18 ps in the 3–10-GHz bandwidth. The linearity of the LNA was tested and the (input) output third-order intercept point ranges from (-8.6 dBm) 7.8 to (-9.2 dBm) 6.4 dBm

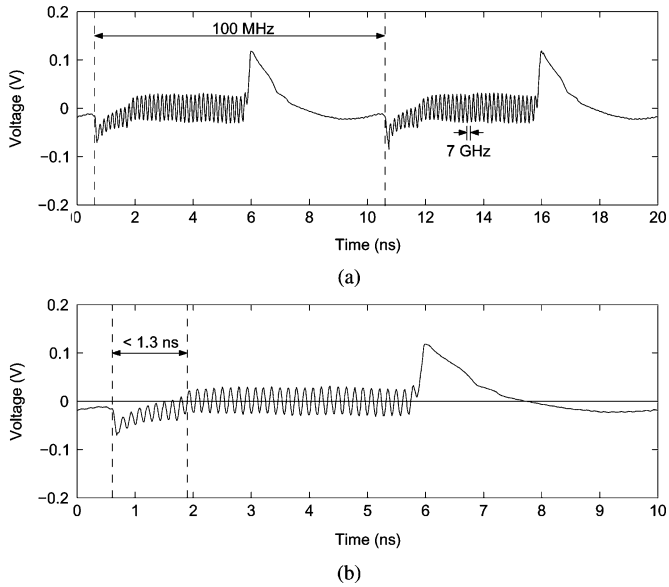

Fig. 14. Measured time-domain output at 100 MHz. (a) Two clock periods. (b) One clock period.

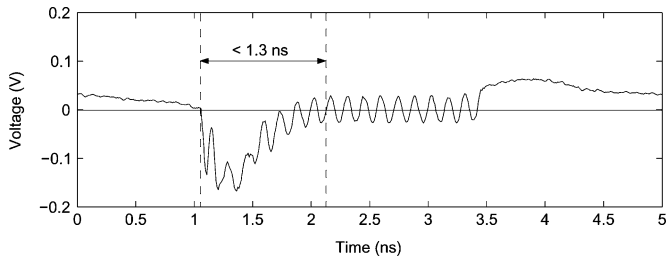

Fig. 15. Measured time-domain output at 200 MHz (one clock period).

over the 3–10-GHz frequency range. The output 1-dB compression point were also measured to be −2.2 dBm, −4.0 dBm, and −4.6 dBm at 3, 7, and 10 GHz, respectively.

The performance of the LNA while being switched on and off was also tested using 100- and 200-MHz clock signals. The input clock is a periodic sinusoidal signal that is converted on-chip into a digital square wave using the edge sharpening inverters. The output was first measured in the time domain at 100- and 200-MHz clock frequencies, and Figs. 14 and 15 show the digital serial analyzer (DSA)'s measurement results. A 7-GHz sinusoidal signal was used for the RF input of the LNA for the time-domain measurements. It is clear that the output is periodic and coherent, and that the LNA gain can settle within 1.3 ns from the turn-on instant.

The output power spectrum was also measured using the spectrum analyzer and is plotted in Fig. 16(a) over a span of 1 GHz around the center (input) frequency of 7 GHz. It is clear that the harmonic components generated at multiples of the clock frequency (100 MHz) are coherent and well defined. Fig. 16(b) shows the measured phase noise of the 7-GHz component in the output spectrum. The phase noise of the input 7-GHz reference is also included for comparison. As depicted in Fig. 16(b), the output phase noise matches that of the input signal, but is approximately 6–10 dB higher. This amounts to

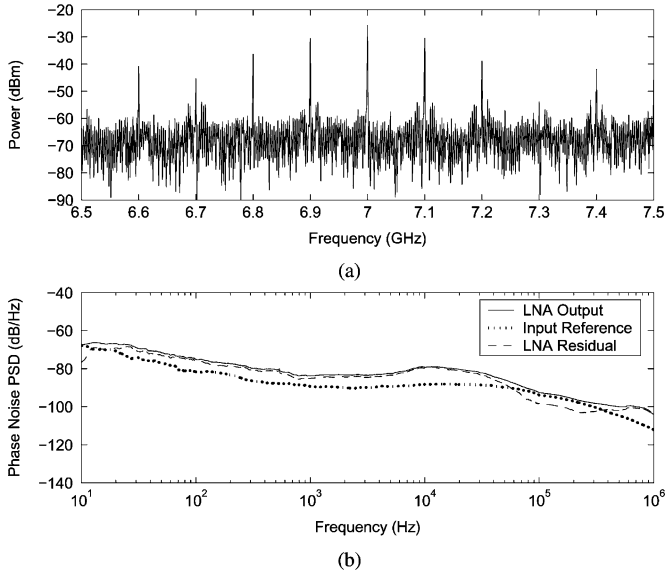

Fig. 16. Measured LNA output. (a) Power spectrum. (b) Phase noise.

an integrated rms jitter $(J_{\rm OUT})$ of about 750 fs from 10 Hz to 1 MHz. The input integrated rms jitter $(J_{\rm IN})$ from 10 Hz to 1 MHz is 420 fs. Also shown in Fig. 16(b) is the residual phase noise added by the switched LNA $(L_{\rm LNA})$, which has been calculated by deducting the input phase noise from the output phase noise (in magnitude) and then converting the result into decibels

$$L_{\rm LNA} = 10\,\log\left(10^{\frac{L_{\rm OUT}}{10}} - 10^{\frac{L_{\rm IN}}{10}}\right) \tag{5}$$

where $L_{\rm OUT}$ and $L_{\rm IN}$ are the measured output and input phase noise, respectively, shown in Fig. 16(b). The integrated rms jitter added by the switched LNA $(J_{\rm LNA})$ from 10 Hz to 1 MHz can thus be calculated from the switched LNA residual phase noise $(L_{\rm LNA})$ to be about 620 fs. Note that this satisfies the relationship

$$J_{\rm OUT}^2 = J_{\rm LNA}^2 + J_{\rm IN}^2. \tag{6}$$

Table II summarizes the proposed LNA's performance in comparison with other recently reported broadband LNAs. To aid the comparison, a figure of merit (FOM) suitable for the broadband amplifiers has been calculated and is defined as

$$\text{FOM [GHz/mW]} = \frac{|S_{21}|[1] \times \text{BW [GHz]}}{(\text{NF}[1] - 1) \times P_{\rm DC}\,[\text{mW}]} \tag{7}$$

where $|S_{21}|[1]$ is the power gain in magnitude, BW [GHz] is the bandwidth in gigahertz, $(\text{NF}[1] - 1)$ is the excess NF in magnitude, and $P_{\rm DC}$ [mW] is the dc power consumption in milliwatts. For the FOM calculation, the 3-dB bandwidth is considered, while the NF is the maximum value within the 3–10-GHz frequency range. The unity current gain frequency f_T or the unity power gain frequency $f_{\max}$ of the CMOS process (i.e., technology cost) could not be included in the FOM since it is not explicitly reported in most of the previously published work. As can be seen from Table II, our proposed LNA exhibits a good

TABLE II
SUMMARY OF LNA'S PERFORMANCE IN COMPARISON WITH OTHER WORK

Reference	CMOS process	Chip area (mm^2)	DC power (mW)	S_{21} (dB)	Bandwidth (GHz)	NF (dB)	FOM (GHz/mW)	Pulsed Operation?
[18]	130 nm	0.88	37.8/6.86	20.47/11.03	0.4–10.5/0.7–10.9	3.29/4.25	19.33/6.32	No
[20]	130 nm	0.031	14.4	12.4	0.1–14	2.7–3.7	12.48	No
[25]	90 nm	0.12	20.4	12.7	0.1–20	3.3–5.5	12.98	No
[26]	130 nm	0.435	26	15	0.0–12	2.3–4.5	8.63	No
[27]	90 nm	0.41	12.5	15.4	0.0–21	4.4–6.0	19.54	No
This Work	**130 nm**	**0.50**	**18/10**	**16 $\pm$ 0.75**	**1–10.6**	**3.9$\pm$0.28**	**15.07**	**Yes**

balance between performance metrics, and thus a relatively high FOM compared to other work.

IV. CONCLUSION

A novel fast switching noise-cancelling LNA has been developed in 0.13-μm CMOS for 3.1–10.6-GHz UWB applications. A new noise-cancelling technique with inductive degeneration and series inductive peaking has been employed to simultaneously achieve a flat sub-4-dB NF and a flat gain of 16.6 dB for frequencies up to 10 GHz. Large resistors used for dc biasing that lead to long charging time constants are bypassed, allowing the output voltage to settle within only 1.3 ns for fast switching speeds of up to 200 MHz. The phase noise and jitter added by the switched LNA were characterized, and the measured output integrated rms jitter is about 750 fs from 10 Hz to 1 MHz, while the input integrated rms jitter is 420 fs. The circuit consumes less than 10 mW of average power at 50% duty cycle and occupies an active chip area of less than 0.5 mm^2.

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