2-W Broadband GaN Power-Amplifier RFIC Using the f_T Doubling Technique and Digitally Assisted Distortion Cancellation

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***Abstract*—The method of derivative superposition is enhanced with digital techniques to cancel the intermodulation distortion generated by a 2-W power amplifier (PA) RF integrated circuit over a broad band of 6 GHz. Two amplifiers were fabricated and tested: a baseline PA without distortion cancellation and a PA with digitally assisted distortion cancellation to demonstrate the effectiveness of the new technique. The PAs are biased in class-A mode and have an $OP_{1\mathrm{dB}}$ of 31 dBm and a P_{SAT} of 33 dBm. Measurements reveal that the output third-order intercept point (OIP3) of the PA with digitally assisted distortion cancellation can be increased to 50.25±3.75 dBm between 1–6 GHz relative to the OIP3 of the baseline PA, which is 40.25±2.75 dBm over the same frequency span. The level of distortion cancellation is not only dependent on the frequency of the incident signal, but also on its power level. Data is presented that shows how the proposed digitally assisted distortion cancellation method also improves the OIP3 of the PA when the RF input power level is taken into account.**

***Index Terms*—Digitally assisted RF circuits, distortion cancellation, gallium–nitride (GaN), power amplifiers (PAs), RF integrated circuit (RFIC).**

I. Introduction

MAXIMIZING one performance metric of a circuit can adversely impact another one of its metrics and vice-versa. For power amplifiers (PAs), the metrics that are often at odds are power efficiency on one side and linearity and broadband performance on the other. PAs that use class E and F topologies have excellent power efficiency [1], [2] and are attractive for mobile phones, for example, because they are battery operated. Meanwhile, in cases where linearity and broadband performance are paramount, the class-A topology is a suitable choice [3], [4] if there is enough dc power available and if proper measures are taken to dissipate the excess heat. Applications that benefit from highly linear low-distortion class-A amplifiers include engineering and scientific test equipment because that equipment has to produce much less distortion than the circuits under test.

Several methods exist to improve the linearity of amplifiers, including predistortion, feedforward, optimal biasing, and derivative superposition (DS). Predistortion is the most common, where the input signal is distorted such that it is the inverse of the amplifier nonlinearity [5]–[10]. Feedforward techniques have also been used [11]–[14], typically achieving higher linearity. However, an additional error amplifier is needed, increasing dc power and reducing efficiency. In optimal biasing, the transistor is precisely biased such that the third-order nonlinearity coefficient is reduced to zero [15], [16], and as a result, this last method can be sensitive to bias variations.

DS can significantly reduce third-order intermodulation distortion (IMD) in amplifiers [17]–[20]. The DS method relies on a network of auxiliary transistors to produce IMD products that are out-of-phase relative to the IMD products of the amplifier. Thus, when the two sets of IMD products are summed, they cancel each other out. Since the only circuitry that is needed are a few auxiliary transistors, DS is particularly well suited for use in RF integrated circuit (RFIC)-based amplifiers because it does not require too much additional chip area. Previous works have shown that applying DS to an amplifier can increase its IIP3 by over 10–20 dB [18], [21]–[23] compared with a baseline amplifier without DS.

Despite the DS method's successes, the amount of IMD cancellation is sensitive to the bias voltage of the auxiliary transistors and small variations in those bias voltages can move a PA using DS away from the optimal IP3. In such a situation, the PA can revert back to an IP3 that is close, or even identical, to the IP3 of a baseline PA that does not use DS. The sensitivity of DS to the bias voltages is due, to a notable extent, on the fact that the magnitude and phase of the IMD products depend on the frequency and power level of the incident RF signal.

This paper presents a digital-assist technique that uses a microcontroller to make DS more robust and less sensitive to transistor bias voltages. This is demonstrated through the design, fabrication, and measurement of a 2-W GaN PA with digitally assisted distortion cancellation using the DS method. Test results are shown for three different cases: a baseline PA without distortion cancellation, the distortion-cancelling PA *without* digital assist, and for the distortion-cancelling PA *with* digital assist. The measurements clearly show a sustained improvement in the OIP3 of the digitally assisted PA compared

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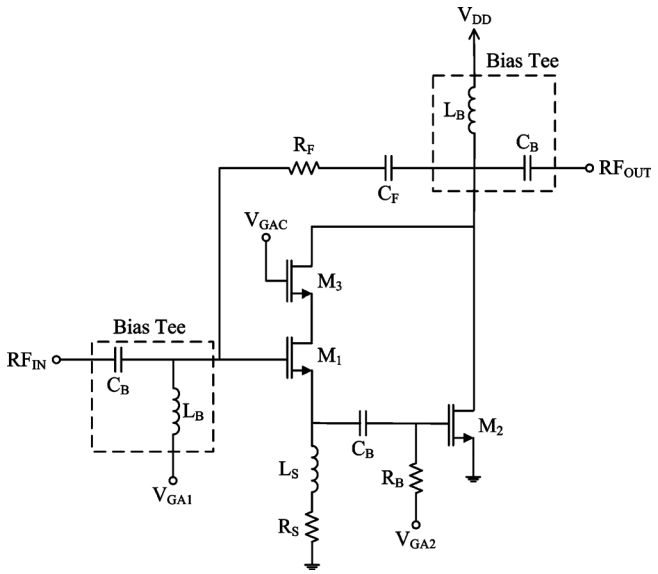

Fig. 1. Circuit schematic of the baseline PA.

to the basic distortion-cancelling PA without digital assist (DC-PA) even as the input signal's frequency and power level change.

II. PA Circuit Description

The baseline PA without distortion cancellation is shown in Fig. 1. That PA is described in detail in [24] and a brief overview of the PA's operation is given here. Transistors M_1 and M_2 constitute a Darlington-type stage (f_T doubler), a topology that has been shown to improve the frequency response of the devices [25]–[27]. M_1 together with L_S and R_S constitute a source–follower sub-circuit and the output signal is fed to M_2, which is in a common-source configuration. Device M_3 is stacked above M_1 to allow for different drain voltages to be used for M_1 and M_2 by changing the channel resistance of M_3 through its gate bias voltage, $V_{\rm GAC}$. The amplifier uses shunt–shunt feedback through R_F and C_F for wideband operation and to help with impedance matching at the input and output ports.

Before describing the low-distortion PA circuit, a short description of the DS method is presented to give some context for the subsequent discussion. First, we recall that the drain-to-source current, $i_{\rm DS}$, of a field-effect transistor (FET) in saturation can be written as the power series

$$i_{\rm DS} = I_{\rm DS} + g_{m1}v_{\rm GS} + g_{m2}v_{\rm GS}^2 + g_{m3}v_{\rm GS}^3 + \cdots \quad (1)$$

where $I_{\rm DS}$ is the bias or quiescent drain–source current, $v_{\rm GS}$ is the gate–source voltage, and

$$g_{mn} = \frac{1}{n!}\frac{\partial^n i_{\rm DS}}{\partial V_{\rm GS}^n}. \quad (2)$$

The higher order terms in the series, $V_{\rm GS}^n$, describe the distortion produced by the circuit. The DS method, when used for third-order IMD cancellation, starts from the observation that the sign of the g_{m3} coefficient in (1) can change from positive to negative depending on the transistor's gate bias voltage. The idea, then, is to use auxiliary transistors to generate IMD products with the same magnitude, but opposite phase relative to the IMD products produced by the amplifier. When the two sets of IMD products are added, they cancel out and the result is, ideally, a distortion-free signal at the output of the overall circuit.

To add distortion cancellation to the PA in Fig. 1, two auxiliary common-source devices M_{1A} and M_{2A} are inserted in parallel to M_1 and M_2, respectively, as shown in Fig. 2. An auxiliary transistor is not directly associated with M_3 because M_3 has the same drain current as M_1. Therefore, the distortion produced by M_1 and M_3 can be mitigated with just one auxiliary device, M_{1A}. The drain voltage of M_{1A} and M_{2A} is supplied through transistor M_B.

Transistors M_1 and M_2 in the main signal path are always in saturation because it is a class-A amplifier. For those devices, the g_{m3} coefficient in (1) is negative. Therefore, the devices in the auxiliary path are biased near pinch-off so that their g_{m3} term is positive. In this manner, the IMD tones produced in the main path and the auxiliary path will have opposite phases and will cancel when they are combined at node E before the output bias tee in Fig. 2. Since the auxiliary transistors operate near pinch-off, their dc power consumption is small compared to the transistors in the main signal path. In fact, the dc-bias current of the auxiliary path is less than 1% of that of the main signal path. As a result, this particular distortion-cancelling arrangement adds negligible dc power, having only a minor effect on the amplifier's power efficiency ($<$1%).

Table I summarizes the transistor gate dimensions, inductor values, capacitor values, and resistor values used in the design of the PA. All of these devices are integrated on-chip, using thin-film nichrome resistors, metal–insulator–metal (MIM) capacitors, and spiral inductors.

III. Distortion Cancellation With Digital Assist

While the distortion-cancelling PA has an OIP3 that is up to 14 dB higher relative to the baseline PA (see Section IV), the basic DS technique has some limitations as noted earlier. One problem is that the magnitude and phase of the IMD tones produced in the main path of the amplifier change as a function of the input signal's frequency and power level $(f_{\rm in}, P_{\rm in})$. Once the gate bias voltages of the auxiliary transistors in Fig. 2 have been set for maximum IMD cancellation, those optimal gate voltages are only useful for a very small set of frequencies and power levels around $(f_{\rm in}, P_{\rm in})$. Therefore, the degree of IMD cancellation is very sensitive to small changes in the gate voltages of the auxiliary transistors.

To address the above challenges and thereby obtain an amplifier with a robust distortion-cancellation mechanism, we have employed digital techniques to optimally bias the auxiliary transistors for maximum IMD cancellation over a wide band. The concept is to adjust the dc bias voltages V_{GA1}, V_{GA2}, V_{GA1A}, V_{GA2A}, and V_{GACA} to obtain the best IP3 based on the incident signal's frequency and power level. This digital control procedure allows us to achieve a high IP3 from 1 to 6 GHz.

A block diagram of the digital-assist network is shown in Fig. 3 and a flowchart of the algorithm implemented by the microcontroller is shown in Fig. 4. First, the frequency and power

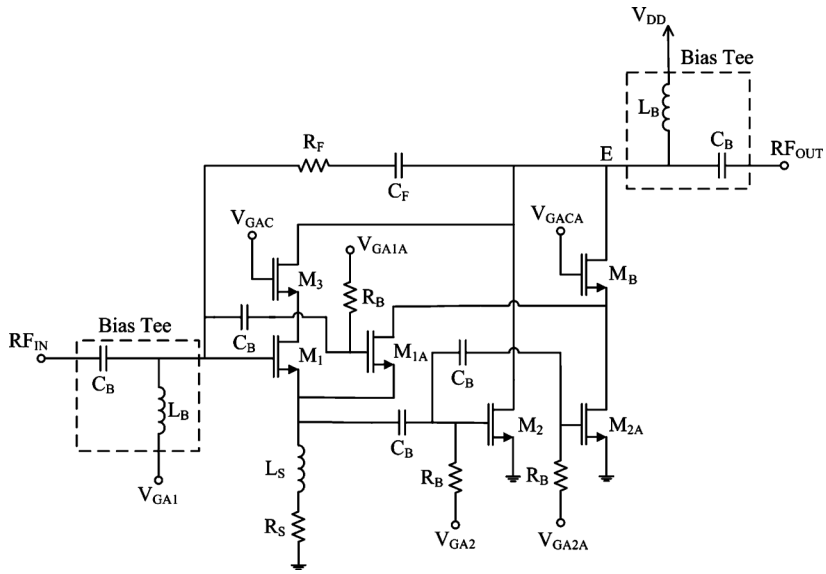

Fig. 2. Circuit schematic of the complete PA with distortion cancellation.

TABLE I
SUMMARY OF COMPONENT VALUES FOR THE PA

Transistor	$(W/L)_{1,2}$	$(W/L)_3$	$(W/L)_{1A,2A}$	$(W/L)_{3A}$
Size (μm)	600/0.8	600/0.8	160/0.8	320/0.8
Component	L_S	R_S	R_F	C_F
Values	0.3 nH	8 Ω	255 Ω	2.5 pF
	R_B	C_B		
	1.2 kΩ	6 pF		

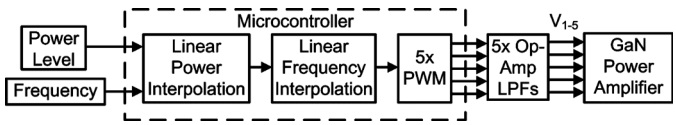

Fig. 3. Block diagram of the digital dc-bias control setup.

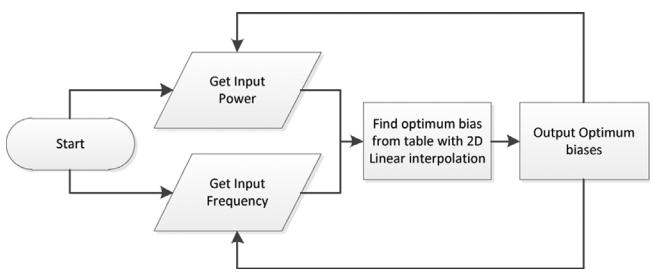

Fig. 4. Algorithm flowchart.

of the input signal to the amplifier are entered to the microcontroller chip. A lookup table in the microcontroller memory contains the optimal gate bias voltages of the transistors in Fig. 2 that yield a maximum OIP3 at different frequency and power points. The voltages stored in the lookup table are found through measurements carried out at regular frequency and power intervals.

If the signal frequency or power is not among the stored frequencies and power levels in the lookup table, the microcontroller enters an interpolation routine to find the optimal bias voltages based on the nearest measured values stored in the table. Once the bias voltages have been computed, the corresponding voltages are applied to the PA.

The bilinear interpolation technique implemented in the microcontroller consists of finding the closest measured frequency and power level below and above those indicated by the input switches. If the indicated frequency and/or power level is equal to an entry in the read-only-memory (ROM) table, that entry was used as the closest frequency and/or power level. A pair of bias voltages are then interpolated in the power variable for the closest frequency below the indicated frequency (f_1), producing V_{f_1}, and the closest frequency above (f_2), giving V_{f_2}. The voltages V_{f_N}, $N = 1, 2$ can be expressed as

$$V_{f_N} = K_{P_N} \times (V_{hp_N} - V_{lp_N}) + V_{lp_N} \tag{3}$$

where V_{hp_N} and V_{lp_N} are the bias voltages at the closest power levels measured above and below the selected power level, respectively. K_{P_N} is a scaling factor given by the indicated power level P_{ind}

$$K_{P_N} = \frac{P_{\text{ind}} - P_{\text{low}}}{P_{\text{high}} - P_{\text{low}}}. \tag{4}$$

Next, the calculated pair of voltages V_{f_1} and V_{f_2} are interpolated further to obtain a single dc-bias voltage V_{bias}. This process effectively performs interpolation over the two dimensions (frequency and power) to arrive at a suitable bias voltage V_{bias}

$$V_{\text{bias}} = K_f \times (V_{f_2} - V_{f_1}) + V_{f_1} \tag{5}$$

where K_f is a scaling factor given by the indicated frequency f_{ind}

$$K_f = \frac{f_{\text{ind}} - f_1}{f_2 - f_1}. \tag{6}$$

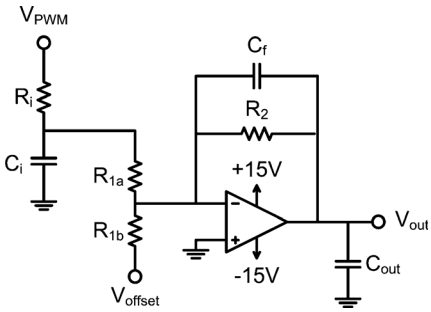

Fig. 5. Circuit schematic of active *RC* LPF.

The microcontroller chip used in this study cannot directly produce the negative voltages required by the PA. Instead, the microcontroller digitally encodes the voltage values using pulse-width modulated (PWM) waveforms. The PWM modules have 10-bit precision, which, in this study, can be used to produce gate voltages in increments as small as 5.3 mV. An active *RC* low-pass filter (LPF) with negative gain shown in Fig. 5 is used between the microcontroller and the PA to convert the PWM waveforms to the desired analog gate bias voltages. With this setup, dc-bias voltages V_{GA1}, V_{GA2}, V_{GA1A}, and V_{GA2A} can be produced in the range from -5.3 to 1.2 V, while V_{GACA} can be generated within the range from 2.0 to 8.0 V.

The digital-assist network consisting of the microcontroller chip and the five opamp LPFs consumes a total of approximately 270 mW of dc power. This is less than 5% of the dc power consumption of the PA, having a small effect on the amplifier's power efficiency. Furthermore, the digital-assist network can be fully integrated in a digital CMOS chip for a low-power implementation, minimizing its impact on efficiency. In sum, the digitally assisted distortion cancellation technique can enhance the linearity of the amplifier without significantly reducing the power efficiency.

IV. Experimental Results

The PA with digitally assisted distortion cancellation and the baseline PA were fabricated using a 0.8-μm GaN HFET process at the Canadian Photonics Fabrication Centre (CPFC), National Research Council, Ottawa, ON, Canada. Microphotographs of the digitally assisted PA and the baseline PA are shown in Figs. 6 and 7, respectively. The digitally assisted PA occupies an area of 1.03 mm^2 excluding bond pads, while the baseline PA occupies 0.83 mm^2 excluding bond pads. Both PAs were measured on-wafer using coplanar-waveguide probes while external bias tees were used to supply the dc and RF signals to the chip. The drain supply voltage was 20 V in each case.

A. Baseline PA

The output power versus input power response of the PA was measured at different frequencies and the results at 4 GHz are plotted in Fig. 8. The PA has a power gain of 12.5 dB, an output $P_{1\mathrm{dB}}$ of 30.25 dBm, and a P_{SAT} of 33.8 dBm at that frequency. The measured drain efficiency (η) of the PA versus input power is also shown in Fig. 8 at 4 GHz. The PA has an efficiency of about 19% at its $P_{1\mathrm{dB}}$ and the efficiency increases to 35% as the amplifier is driven harder and approaches P_{SAT}.

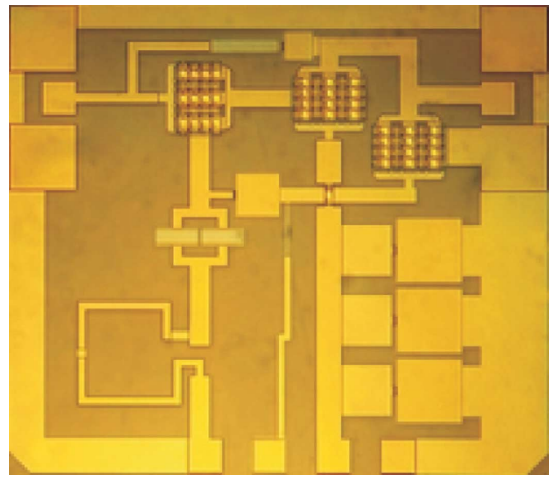

Fig. 6. Microphotograph of the baseline PA.

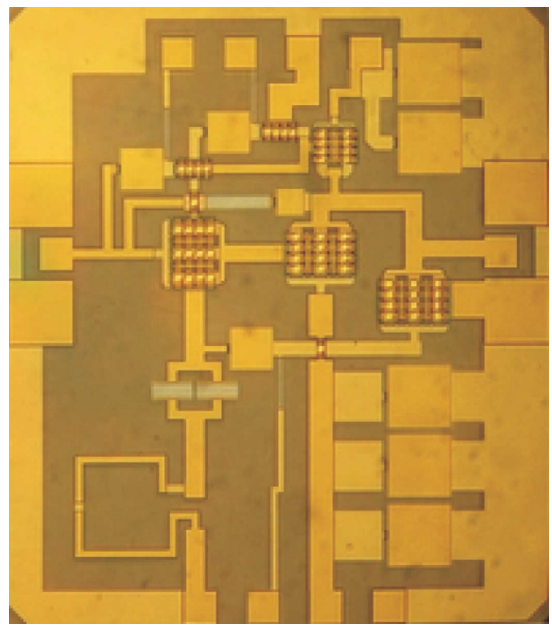

Fig. 7. Photograph of the distortion-cancelling PA.

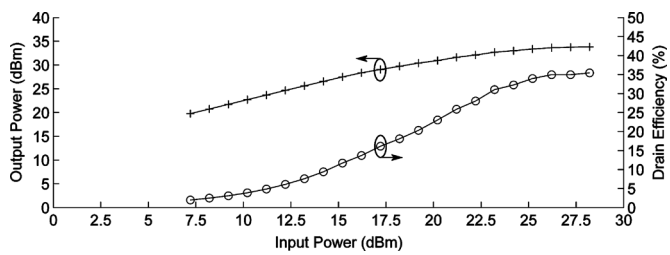

Fig. 8. Baseline PA's measured power response and drain efficiency. Data taken at 4 GHz.

Fig. 9 shows the baseline PA's $P_{1\mathrm{dB}}$ and P_{SAT} as a function of frequency from 1 to 6 GHz. Both of these metrics have good flatness over the entire band: the P_{SAT} is 33$\pm$0.8 dBm, while the $P_{1\mathrm{dB}}$ is 31.3$\pm$1 dBm. Furthermore, the amplifier's power gain (Fig. 10) is 12.2$\pm$0.2 dB over the band. Good agreement between measured and simulated results is observed in Figs. 9 and 10. Predrawn device layouts and microstrip interconnects

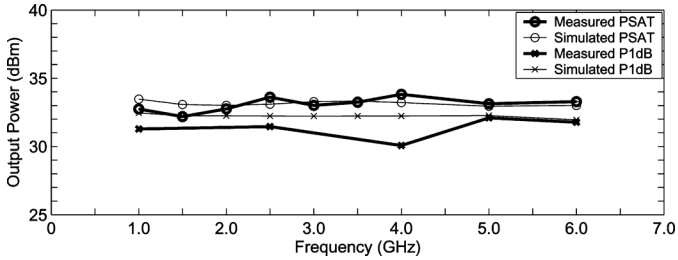

Fig. 9. Baseline PA's measured $P_{\rm SAT}$ and $P_{\rm 1dB}$ versus frequency.

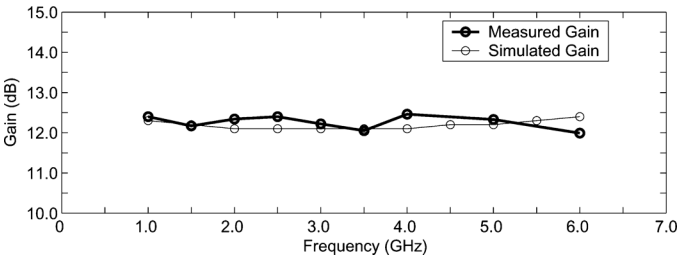

Fig. 10. Measured gain from 1 to 6 GHz.

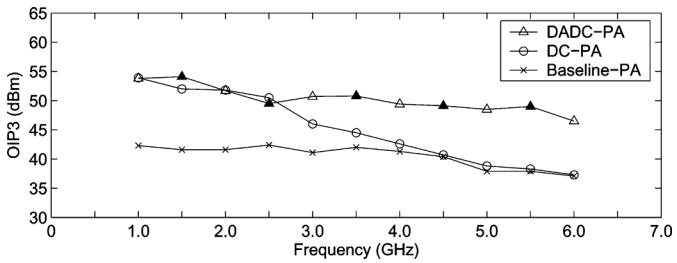

Fig. 11. Measured OIP3 versus frequency using optimum bias voltages at 1 GHz for the DC-PA. Solid (filled) markers indicate points obtained using interpolated bias voltages.

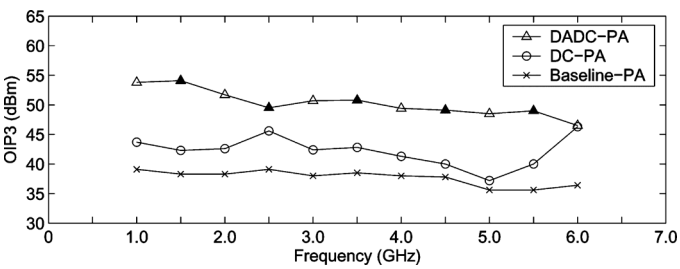

Fig. 12. Measured OIP3 versus frequency using optimum bias voltages at 6 GHz for the DC-PA. Solid (filled) markers indicate points obtained using interpolated bias voltages.

characterized and modeled by the foundry were used as is in this design to achieve the best model-to-hardware correlation.

B. PA With Digitally Assisted Distortion Cancellation

Extensive two-tone tests were carried out to demonstrate how the IP3 of the distortion-cancelling PA is substantially improved through the proposed digital-assist technique. The PA's IP3 was measured under the following two conditions:

Case 1) without digital assist;

Case 2) with digital assist.

The purpose of Case 1) was to determine the optimal bias voltages of the devices in the PA that yielded the best OIP3. The two tones were spaced at 10 MHz and their center frequency and power level were evenly distributed over a 2-D space of points $(f_{\rm in}, P_{\rm in})$. For demonstrative purposes, the range of

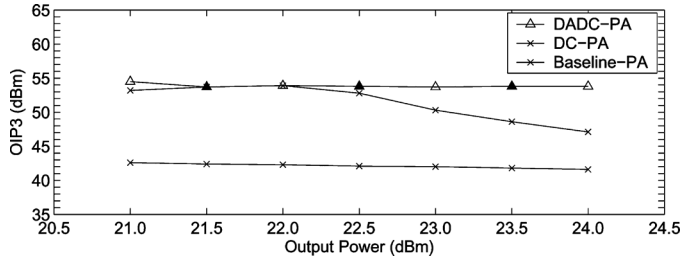

Fig. 13. Measured OIP3 versus $P_{\rm out}$ at 1 GHz. Optimum bias voltages at 22 dBm used for DC-PA. Solid (filled) markers indicate points obtained using interpolated bias voltages.

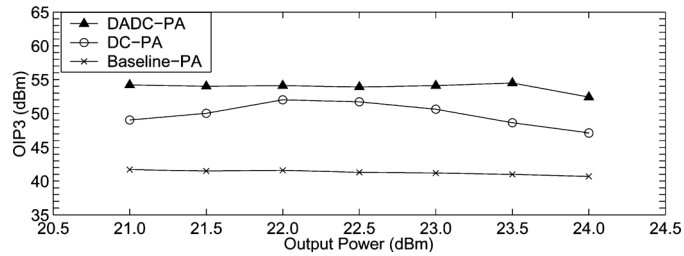

Fig. 14. Measured OIP3 versus $P_{\rm out}$ at 1.5 GHz. Solid (filled) markers indicate points obtained using interpolated bias voltages.

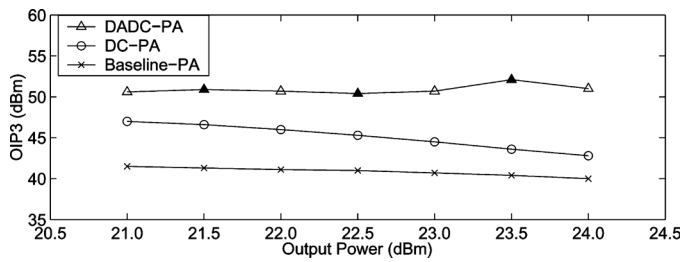

Fig. 15. Measured OIP3 versus $P_{\rm out}$ at 3 GHz. Solid (filled) markers indicate points obtained using interpolated bias voltages.

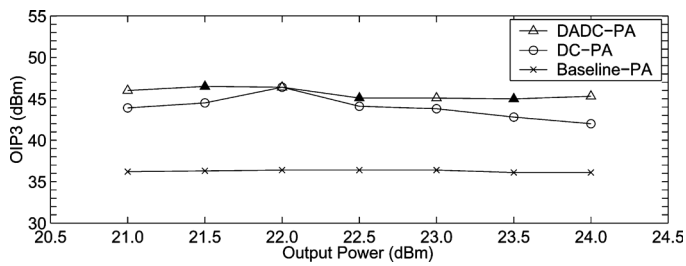

Fig. 16. Measured OIP3 versus $P_{\rm out}$ at 6 GHz. Optimum bias voltages at 22 dBm used for DC-PA. Solid (filled) markers indicate points obtained using interpolated bias voltages.

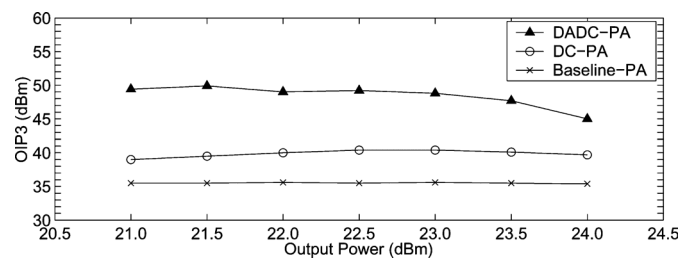

Fig. 17. Measured OIP3 versus $P_{\rm out}$ at 5.5 GHz. Solid (filled) markers indicate points obtained using interpolated bias voltages.

$f_{\rm in}$ was from 1 to 6 GHz with a $\Delta f_{\rm in} = 1$ GHz, while the range of $P_{\rm in}$ was from 9 to 12 dBm using a $\Delta P_{\rm in} = 1$ dBm. The chosen $\Delta f_{\rm in}$ and $\Delta P_{\rm in}$ values are relatively large in order

TABLE II
SUMMARY OF BROADBAND PA CHARACTERISTICS

Characteristic	**This work**	[28]	[29]	[30]	[31]	[32]
GaN Technology	**0.8 μm**	0.2 μm	N/A	0.25 μm	0.15 μm	0.2 μm
Circuit Area (mm^2)	**1.03**	4.8	N/A	2.08	6	2.89
Supply Voltage (V)	**20**	30	28	40	20	15
Bandwidth (GHz)	**1–6**	DC–20	0.35–8	0.25–3	9–19	1–4
P_{SAT} (dBm)	**33 $\pm$ 0.8**	30 to 36	38.2	39.2	–	32
Gain (dB)	**12.2 $\pm$ 0.2**	12	9 $\pm$ 1	20	13	14.5
OP_{1dB} (dBm)	**31.3**	32.5	37.1	38.5	27	31
OIP3 (dBm)	**50.25**	42.6	49	51	see note[1]	44.3
Efficiency	**Max: 37% (η)**	10–15% (PAE)	20% (PAE)	see note[2]	–	see note[3]

[1] IMD: 30 dBc at 26 dBm output power.
[2] DC bias current: 750mA
[3] DC bias current: 400mA

to demonstrate the efficacy of the interpolation routine when the PA has to operate with the in-between points. With an average gain of 12 dB, the PA produced 21–24 dBm of RF output power, $P_{\rm out}$, meaning it was operating at a backoff (BO) power from 10 to 7 dB from its $P_{\rm 1dB}$. When the tests for Case 1) were completed, the bias voltages of the auxiliary transistors were stored in the microcontroller's memory. For the measurements in Case 2), the digital system in Fig. 3 executed the interpolation routine to produce the necessary bias voltages for the PA at any desired $(f_{\rm in}, P_{\rm in})$ within the outer limits of the 2-D space specified above. The interpolation routine was executed in particular for the in-between points of $f_{\rm in} = \{1.5\ {\rm GHz}, 2.5\ {\rm GHz}, 3.5\ {\rm GHz}, 4.5\ {\rm GHz}, 5.5\ {\rm GHz}\}$ and $P_{\rm in} = \{9.5\ {\rm dBm}, 10.5\ {\rm dBm}, 11.5\ {\rm dBm}\}$.

In the plots that follow, experimental results are presented for the following three cases: the baseline PA, the distortion-cancelling PA without digital assist (DC-PA), and the digitally assisted distortion-cancelling PA (DADC-PA). Solid (filled) markers in the DADC-PA plots indicate measured results at intermediate frequency and power points, obtained using the bias voltages generated by the interpolation routine.

In Fig. 11, the measured OIP3 of the baseline PA versus frequency (at $P_{\rm out} = 22$ dBm) has good flatness from 1 to 6 GHz and has an average value of 40.25 dBm. The OIP3 of the DC-PA is 54 dBm at 1 GHz, a significant improvement of 13.75 dB relative to the OIP3 of the baseline PA at that frequency. However, the DC-PA's OIP3 starts to drop after 1 GHz and is nearly identical to the OIP3 of the baseline PA after 4.5 GHz. This is because the bias voltages of the DC-PA were optimized for maximum OIP3 at 1 GHz and they remained fixed at that value as the frequency changed. Meanwhile, using digital control, the DADC-PA is able to maintain its OIP3 at an average value of 50.25 dBm from 1 to 6 GHz. Thus, the OIP3 of the DADC-PA is 10 dB better, on average, than the OIP3 of the baseline PA over the band.

Fig. 12 shows the measured OIP3 for the baseline PA, DC-PA, and DADC-PA (at $P_{\rm out} = 22$ dBm), but this time, the DC-PA's bias voltages have been optimized for maximum OIP3 at 6 GHz. The OIP3 of the DADC-PA is the same as before. Yet, as expected, the OIP3 of the DC-PA is best at 6 GHz, while at all other frequencies, the OIP3 falls back to a value closer to that of the baseline PAs.

Fig. 13 shows the measured OIP3 as a function of the output RF signal power $(P_{\rm out})$ taken at 1 GHz. The OIP3 of the baseline PA is constant at 42 dBm. The bias voltages of the DC-PA were optimized to obtain a maximum OIP3 of 54 dBm at a representative $P_{\rm out} = 22$ dBm. As a result, we observe that the OIP3 of the DC-PA is best in the vicinity of $P_{\rm out} = 22$ dBm, but drops by 7 dB down to 47 dBm when the $P_{\rm out}$ increases to 24 dBm. Using digital control, on the other hand, we can maintain the OIP3 of the DADC-PA fixed at 54 dBm even as the PA is delivering more RF output power.

In Fig. 14, we observe what happens to OIP3 as a function of $P_{\rm out}$ when the test frequency changes from 1 to 1.5 GHz. While the OIP3 of the DC-PA never reaches its former high value of 54 dBm, the DADC-PA is able to keep its OIP3 at 54 dBm throughout, except at $P_{\rm out} = 24$ dBm, where it drops slightly to 52 dBm. Fig. 15 illustrates how the measured OIP3 versus $P_{\rm out}$ is affected when the test frequency is further increased to 3 GHz. In this case, the OIP3 of the DC-PA is well below 50 dBm (43 dBm at $P_{\rm out} = 24$ dBm), while the DADC-PA is able to keep its OIP3 at about 51 dBm throughout.

Further measurement results on the dependence of OIP3 versus power taken at 6 GHz are shown in Fig. 16. The bias voltages of the DC-PA were optimized for maximum OIP3 at the representative $P_{\rm out} = 22$ dBm. Fig. 17 shows the measured OIP3 versus $P_{\rm out}$ when the test frequency changes from 6 to 5.5 GHz. In both cases, we observe that using digital assist increases and stabilizes the OIP3 of the PA to a nearly constant level as a function of $P_{\rm out}$. In the above plots, note that the OIP3 of the DADC-PA is consistent with the results in Figs. 11 and 12, which shows the frequency response of the DADC-PA's OIP3.

The above tests convincingly show the effectiveness of the proposed digital-assist technique. This approach mitigates the sensitivity that the basic DS method has to changes in signal frequency and input power level, leading to a highly robust distortion cancelling mechanism. Table II summarizes the performance of this PA with that of other broadband GaN amplifiers reported in the literature [28]–[32].

V. CONCLUSIONS

Removing the sensitivity of the DS method to bias voltage variations in the auxiliary transistors and the main circuit is

critical for the widespread industrial use of the technique. The DS method can potentially become the method of choice for linearizing monolithic amplifiers because it requires very little additional space on-chip. In this paper, we demonstrated that, through digital assist techniques, the DS method becomes very robust and can improve and maintain amplifier's IP3 performance even as the input signal's frequency and power level change.

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