Design of a Low-Voltage and Low-Distortion Mixer Through Volterra-Series Analysis

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***Abstract*—The factors that impact the intermodulation distortion performance of an active downconverting mixer are investigated. Through a Volterra-series analysis of the RF transconductor stage of the mixer, design principles are formulated to maximize the mixer's $\mathbf{IIP_3}$. To verify the theoretical analysis, a 0.3–1.2-GHz low-voltage mixer operating from a 0.9-V supply was designed, fabricated, and tested. The mixer employs a common-gate common-source RF transconductor stage with simultaneous distortion and noise cancellation. Experimental results reveal that the mixer can yield an $\mathbf{IIP_3}$ of -0.8 dBm, a double-sideband noise figure below 4.8 dB, and a maximum conversion gain of 8.8 dB.**

***Index Terms*—CMOS, distortion, downconverter, low power, low voltage, mixers, RF integrated circuit (RFIC) design, Volterra series.**

I. Introduction

As WITH other active RF circuits, the intermodulation distortion (IMD) performance of an active mixer is closely related to its dc power consumption. Normally, when the supply voltage of a circuit is reduced, the power of the incident RF signals to the circuit has to be lowered to keep the IMD tones at sufficiently low levels. While the imperative to reduce the dc supply voltage of RF circuits in mobile applications continues unabated, the linearity and IMD performance requirements of the system remain largely intact. To this end, several active mixer topologies have been reported to meet the competing requirements of low dc supply voltage operation and low IMD [1]–[7].

This paper provides a detailed analysis and discussion on how the RF transconductor used in a low-voltage active mixer impacts the linearity of the entire circuit. Using a Volterra-series analysis, we arrive at a set of principles to aid the design of low-distortion active mixers. The transconductor stage used here is a common-gate common-source (CG-CS) topology because, in addition to its low noise figure (NF), it can be simultaneously designed for low distortion operation [8]–[10], and it is this last property of the transconductor circuit that will be explored in detail in subsequent sections of this paper.

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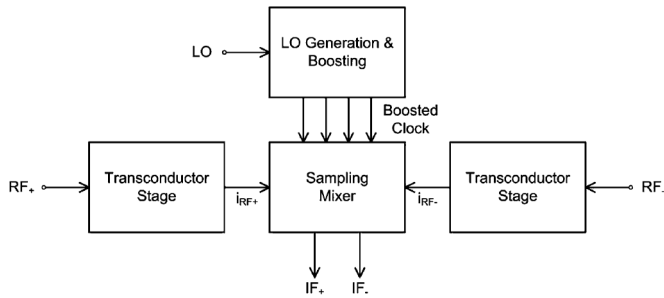

Fig. 1. Block diagram of the proposed low-voltage downconverting mixer.

II. Wideband Downconverting Mixer

The block diagram of the proposed low-voltage low-noise downconverter described in this work is shown in Fig. 1 and the schematic of the mixer core and RF transonductor circuits is found in Fig. 2. The downconverter consists of three main blocks: the RF transconductors, a double-balanced ring mixer, and the clock signal processing circuitry. The entire RF integrated circuit (RFIC), excluding the off-chip IF output buffer, runs from a 0.9-V dc source.

A parallel NMOS-PMOS transistor pair is used to implement the switches in the ring mixer because of its superior ON–OFF characteristic that results, among other things, in better noise performance and better port-to-port isolation. To provide the mixing core with a good differential clock [local oscillator (LO)] signal, a nonoverlapping clock generator was used to generate the hard-switching differential clock signals. The cost of using two transistors per switch, however, is that a larger LO signal is needed than if a single-transistor switch is used. To that end, a boosting circuit [11] was employed to double the amplitude of the clock signal fed to the mixer. Four identical clock boosters were needed and the schematic diagram of a single booster circuit is shown in Fig. 3. A charge storage capacitor, C_b, and a pMOS transistor, M_b, are stacked above a CMOS inverter to elevate the LO output voltage swing. The timing diagram in Fig. 4 helps illustrate the operation of the clock booster circuit.

The pMOS transistor M_b and the charge storage capacitor C_b keep the voltage at node V_b greater than or equal to V_{DD}. When

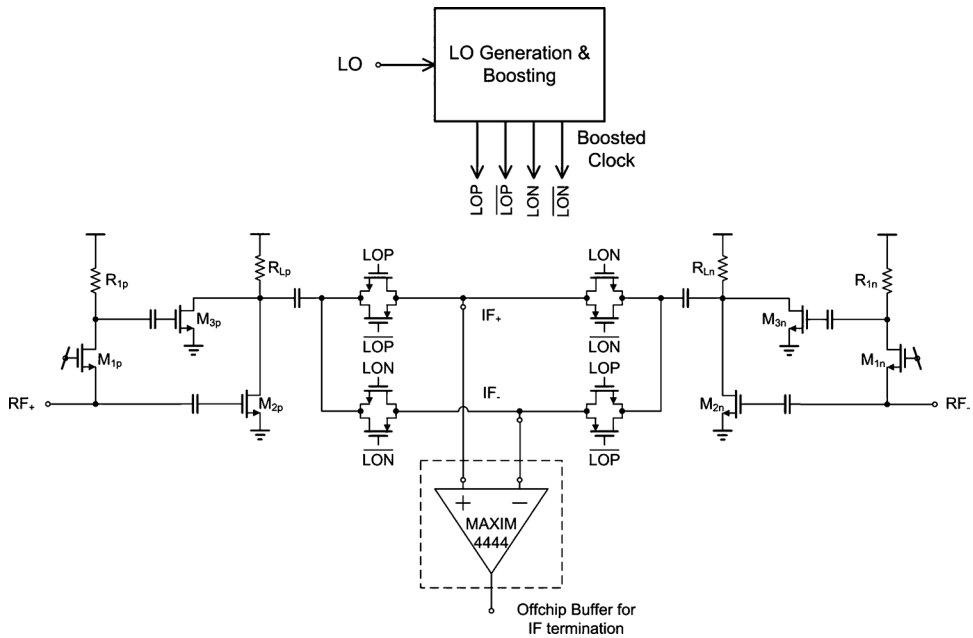

Fig. 2. Low-voltage downconverter circuit schematic (only partial dc biasing shown).

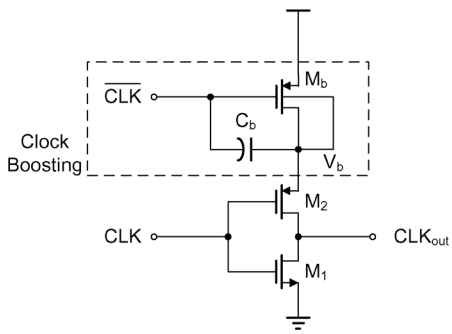

Fig. 3. Clock-boosting circuit.

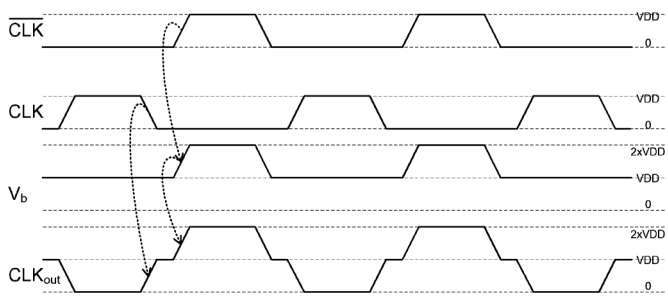

Fig. 4. Timing diagram to illustrate of the clock-boosting circuit.

the CLK signal is high at V_{DD}, the pMOS transistor M_2 in the inverter is turned off while the M_b is turned on because $\overline{\text{CLK}}$ is at 0 V, and therefore, $V_b = V_{DD}$. When the CLK signal is low at 0 V, M_2 is turned on while M_b is turned off because $\overline{\text{CLK}}$ is now at V_{DD}. Due to conservation of charge, the voltage across C_b must increase, which boosts V_b to $2 \times V_{DD}$, and hence, the output clock signal CLK_{out} will also be at $2 \times V_{DD}$. Although additional clock jitter is induced by this procedure, simulations have indicated that this phase noise degradation contributes very little to the overall noise performance of the mixer.

The RF transconductors, one on the left-hand side and one on the right-hand side of the mixer core, are identical and consist of a common-gate (CG) transistor followed by two common-source (CS) transistors. These circuits provide the necessary differential RF signal currents to the mixing core. The CG transistor provides a good input match over a wideband while the CS transistors provide signal gain and are also used to cancel the thermal noise generated in the channel of the CG transistor. This transconductor configuration has been used extensively in noise-canceling low-noise amplifiers (LNAs) [12] and broadband mixer designs [9], [10].

By virtue of being at the front-end of the downconverter, and the use of a hard-switching LO signal, the RF transconductors have a significant impact on the NF and linearity (i.e., the IP_3 and $P_{1\text{ dB}}$) of the entire circuit. An interesting and important feature of the transconductor used here is its ability to not only cancel the noise, but also the IMD generated by the CG transistor [8], [13], [14]. Our analysis will show through a Volterra-series computation that low-distortion circuit operation can be achieved even in a low dc voltage supply environment using a different distortion-canceling mechanism from that discussed in previous works.

III. Nonlinear Analysis of the Mixer's Transconductance Stage

To design low-distortion mixers, it is first necessary to understand the nonlinear phenomena that cause distortion. A highly successful mathematical framework for modeling the nonlinear response of different types of RF circuits is the Volterra-series analysis [15]–[17]. In the system shown in circuit in Fig. 1, the RF transconductor stage has a dominant role on the overall distortion produced by the downconverter. Fig. 5 is a close-up view of the CG-CS transconductor that is analyzed in this section.

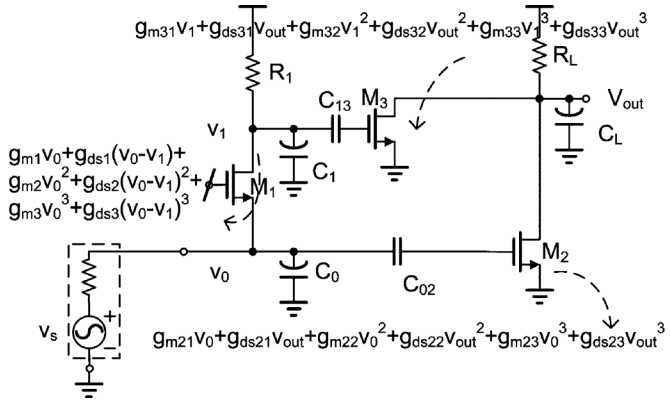

Fig. 5. Simplified schematic of the CG-CS transconductor for linearity analysis.

Similar to the formulation presented in [18], the voltages at the source (V_0) and drain (V_1) of transistor M_1 in Fig. 5 can be written as

$$\begin{aligned} V_0 &= A_1(\omega) \circ V_s + A_2(\omega_1, \omega_2) \circ V_s^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \\ V_1 &= B_1(\omega) \circ V_s + B_2(\omega_1, \omega_2) \circ V_s^2 + B_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \end{aligned} \quad (1)$$

where $A_1(\omega_1)$, $A_2(\omega_1, \omega_2)$, and $A_3(\omega_1, \omega_2, \omega_3)$ model the first-, second-, and third-order nonlinear response of M_1 at the source terminal due to the applied input V_s. Similarly, the B_n's model the nth-order nonlinear responses at the drain of M_1, the ω's represent the dependent frequencies and each $\circ$ symbol denotes the Volterra operand.

The starting point to derive the A_n and B_n kernels is to write the KCL equations at nodes V_0 and V_1, which are

$$i_{m1} + Y_0(\omega) V_0 = Y_s (V_s - V_0) \quad (2)$$

$$i_{m1} = Y_1(\omega) V_1 \quad (3)$$

where i_{m1} is the current through transistor M_1, $Y_0 = sC_0$ is the parasitic admittance at node V_0, $Y_s = 1/R_s$ is the admittance of the signal source, and $Y_1 = 1/R_1 + sC_1$ is the parasitic admittance at node V_1. Equations (2) and (3) are solved recursively to obtain the A_n and B_n kernels (for a derivation, see the Appendix)

$$\begin{aligned} A_1(\omega_1) &= V(\omega_1) \left(g_{ds1} + Y_1(\omega_1) \right) Y_s \\ B_1(\omega_1) &= V(\omega_1) (g_{m1} + g_{ds1}) Y_s \end{aligned} \quad (4)$$

$$\begin{aligned} A_2(\omega_1, \omega_2) = & -V(\omega_1 + \omega_2) Y_1(\omega_1 + \omega_2) \\ & \times \Big\{ g_{m2} A_1(\omega_1) A_1(\omega_2) \\ & + g_{ds2} \Big[A_1(\omega_1) A_1(\omega_2) + B_1(\omega_1) B_1(\omega_2) \\ & - \overline{A_1(\omega_1) B_1(\omega_2)} \Big] \Big\} \end{aligned}$$

$$B_2(\omega_1, \omega_2) = \frac{-A_2(\omega_1, \omega_2)}{Y_1(\omega_1 + \omega_2)} \left(Y_0(\omega_1 + \omega_2) + Y_s \right) \quad (5)$$

and

$$\begin{aligned} A_3(\omega_1, \omega_2, \omega_3) = & -V(\omega_1 + \omega_2 + \omega_3) \times Y_1(\omega_1 + \omega_2 + \omega_3) \\ & \times \Big[2 g_{m2} \overline{A_1(\omega_1) A_2(\omega_2, \omega_3)} \\ & + 2 g_{ds2} \Big(\overline{A_1(\omega_1) A_2(\omega_2, \omega_3)} \\ & + \overline{B_1(\omega_1) B_1(\omega_2, \omega_3)} \\ & - \overline{A_1(\omega_1) B_2(\omega_2, \omega_3)} \\ & - \overline{B_1(\omega_1) A_2(\omega_2, \omega_3)} \Big) \\ & + g_{m3} A_1(\omega_1) A_1(\omega_2) A_1(\omega_3) \\ & + g_{ds3} \left(A_1(\omega_1) A_1(\omega_2) A_1(\omega_3) \right. \\ & - 3 \overline{A_1(\omega_1) A_1(\omega_2) B_1(\omega_3)} \\ & + 3 \overline{A_1(\omega_1) B_1(\omega_2) B_1(\omega_3)} \\ & \left. - B_1(\omega_1) B_1(\omega_2) B_1(\omega_3) \right) \Big] \end{aligned} \quad (6)$$

and

$$B_3(\omega_1, \omega_2, \omega_3) = \frac{-A_3(\omega_1, \omega_2, \omega_3)}{Y_1(\omega_1 + \omega_2 + \omega_3)} \times \left(Y_0(\omega_1 + \omega_2 + \omega_3) + Y_s \right) \quad (7)$$

where

$$g_{mk} = \frac{1}{k!} \frac{\partial^k i_{m1}}{\partial V_0^k} \quad (8a)$$

$$g_{dsk} = \frac{1}{k!} \frac{\partial^k i_{m1}}{\partial (V_1 - V_0)^k}. \quad (8b)$$

This analysis examines the nonlinear distortion produced by the device transconductance and which is modeled by g_{m1}, g_{m2}, and g_{m3}. Furthermore, the distortion produced at the device output is also considered through the nonlinear conductance and that, in turn, is modeled by g_{ds1}, g_{ds2}, and g_{ds3}.

The distortion produced by M_2 and M_3 in Fig. 5 must also be accounted for. To that end, the output voltage V_{out} can be computed recursively to the input voltage V_s according to the equation

$$V_{\text{out}} = K_1(\omega) \circ V_s + K_2(\omega_1, \omega_2) \circ V_s^2 + K_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \quad (9)$$

where the K_n Volterra operators are given by

$$\begin{aligned} K_1(\omega_1) = & \frac{Z_L(\omega_1)}{1 + Z_L(\omega_1)(g_{ds31} + g_{ds21})} \\ & \times \left[g_{m31} B_1(\omega_1) + g_{m21} A_1(\omega_1) \right] \\ K_2(\omega_1, \omega_2) = & \frac{Z_L(\omega_1 + \omega_2)}{1 + Z_L(\omega_1 + \omega_2)(g_{ds31} + g_{ds21})} \\ & \times \left[g_{m31} B_2(\omega_1, \omega_2) + g_{m32} B_1(\omega_1) B_1(\omega_2) \right. \\ & + g_{m21} A_2(\omega_1, \omega_2) + g_{m22} A_1(\omega_1) A_1(\omega_2) \\ & \left. + (g_{ds32} + g_{ds22}) K_1(\omega_1) K_1(\omega_2) \right] \end{aligned} \quad (10)$$

Note that the $K_3(\omega_1,\omega_2,\omega_3)$ kernel, shown in (11) as follows:

$$K_3(\omega_1,\omega_2,\omega_3)=\frac{Z_L(\omega_1+\omega_2+\omega_3)}{1+Z_L(\omega_1+\omega_2+\omega_3)(g_{ds31}+g_{ds21})} \times \Big[g_{m21}A_3(\omega_1,\omega_2,\omega_3) + g_{m31}B_3(\omega_1,\omega_2,\omega_3) + g_{m33}\prod_{i=1}^{3}B_1(\omega_i) + 2g_{m32}\overline{B_1(\omega_1)B_2(\omega_2,\omega_3)} + g_{m23}\prod_{i=1}^{3}A_1(\omega_i) + 2g_{m22}\overline{A_1(\omega_1)A_2(\omega_2,\omega_3)} + 2(g_{ds32}+g_{ds22})\overline{K_1(\omega_1)K_2(\omega_2,\omega_3)} + (g_{ds33}+g_{ds23})\prod_{i=1}^{3}K_1(\omega_i)\Big]. \quad (11)$$

contains the terms $g_{m21}A_3(\omega_1,\omega_2,\omega_3)$ and $g_{m31}B_3(\omega_1,\omega_2,\omega_3)$. Yet, we also know from (6) and (7) that $A_3(\omega_1,\omega_2,\omega_3)$ and $B_3(\omega_1,\omega_2,\omega_3)$ have opposite sign, which is significant because g_{m21} and g_{m31} can be designed to cancel out the A_3 and B_3 kernels in $K_3(\omega_1,\omega_2,\omega_3)$. Not only is the IMD performance of the transconductor stage dependent on g_{m21} and g_{m31}, so is its noise performance as noted earlier. The basic relationship [8], [12] between the transconductances that yields optimal noise cancellation is

$$\kappa=\frac{R_1}{R_s}=\frac{g_{m21}}{g_{m31}}. \quad (12)$$

The second-order distortion produced by the transconductor is also dependent on the above κ factor. This is easily seen by noting that the kernels $A_2(\omega_1,\omega_2)$ and $B_2(\omega_1\omega_2)$ in (5) have opposite sign and that they reappear in the $K_2(\omega_1\omega_2)$ kernel multiplied by g_{m21} and g_{m31}.

The third-order IMD produced by M_1 can be canceled at the output node in Fig. 5 by searching for the gate–source bias voltages for transistors M_2 and M_3 that will force the circuit satisfy the following ratio:

$$\zeta=\frac{g_{m33}}{g_{ds23}+g_{ds33}}=\left|\frac{K_1(\omega_1)}{B_1(\omega_1)}\right|^3. \quad (13)$$

From the design point of view, to benefit from this distortion cancellation technique, the cubic of the ratio between the voltage gain at the output of the CG-CS circuit (i.e., $K_1(\omega_1)$) and the output of the CG circuit (i.e., $B_1(\omega_1)$) needs to match with the ratio of the nonlinear device characteristics according to (13). To reduce the search space of possible bias voltages for M_2 and M_3, the devices were biased with the same gate voltage, but this only for convenience and is not a strong rule. The optimal gate bias voltage can be found with the aid of a graph by defining

$$\zeta_l=\frac{g_{m33}}{g_{ds33}+g_{ds23}} \quad (14)$$

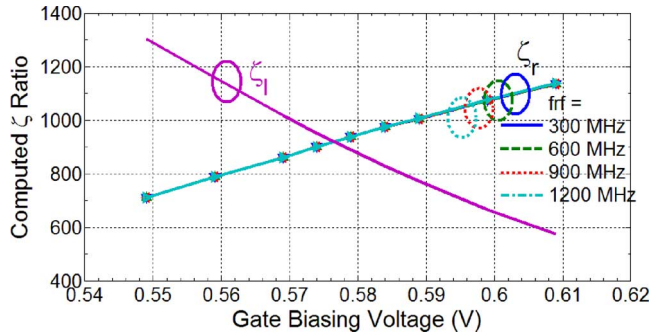

Fig. 6. Graph used to find the bias point of transistors M_2 and M_3 for best distortion cancellation.

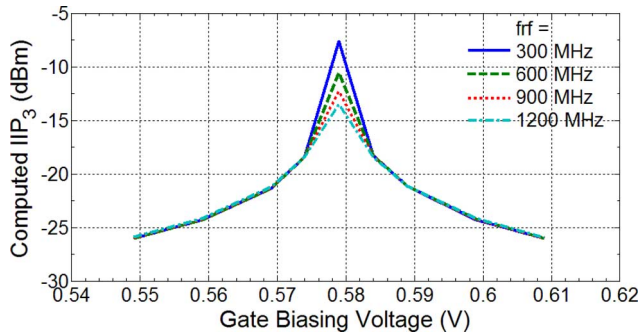

Fig. 7. Computed IIP_3 of the RF transconductor based on the Volterra-series analysis.

$$\zeta_r=\left|\frac{K_1(\omega_1)}{B_1(\omega_1)}\right|^3. \quad (15)$$

The plot of ζ_l and ζ_r is shown in Fig. 6. The optimal bias point for maximum distortion cancellation is when $\zeta_l=\zeta_r$, which is at a gate bias voltage of 0.579 V for the devices used in this paper. Note that ζ_r was computed at different frequencies because $K_1(\omega_1)$ and $B_1(\omega_1)$ are frequency-dependent quantities.

Using the foregoing Volterra analysis, a theoretical expression to calculate the third-order intermodulation intercept point (IIP_3) of the transconductor circuit can be found [15], [19] and is given by

$$\mathrm{IIP}_3(2\omega_i-\omega_s)=\frac{1}{6}\frac{1}{Z_{\mathrm{out}}}\frac{|K_1(\omega_s)|}{|K_3(\omega_i,\omega_i,-\omega_s)|} \quad (16)$$

where $2\omega_i-\omega_s$ is the third-order IMD tone produced by the mixing of ω_s and ω_i, which are closely spaced in frequency (1 MHz). Equation (16) can be used to compute the gate bias voltage of M_2 and M_3 that will yield the best IIP_3 at a specific frequency. We carried out such a computation for the circuit at hand and the results are plotted in Fig. 7. For simplicity, we changed the voltage of M_2 and M_3 simultaneously, but they can be varied independently and the IIP_3 would be graphed as a 3-D surface instead of a 2-D plot. The results in Fig. 7 predict that the optimal gate bias voltage for the transistors is around 0.58 V and is independent of frequency, which is consistent with Fig. 6 and is a prediction that is borne out by experiment, as will be discussed shortly.

IV. Experimental Results

To validate the proposed theory and analysis, the downconverting mixer was fabricated using a 130-nm CMOS process

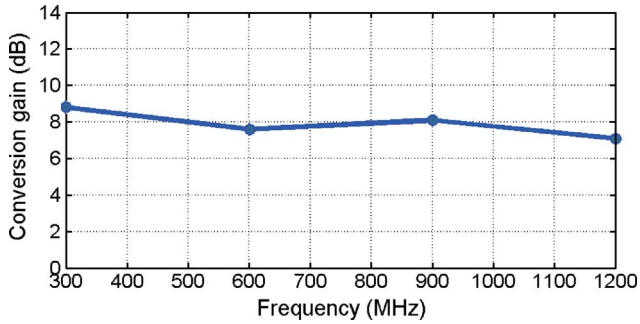

Fig. 8. Measured conversion gain of the mixer across the RF input frequency.

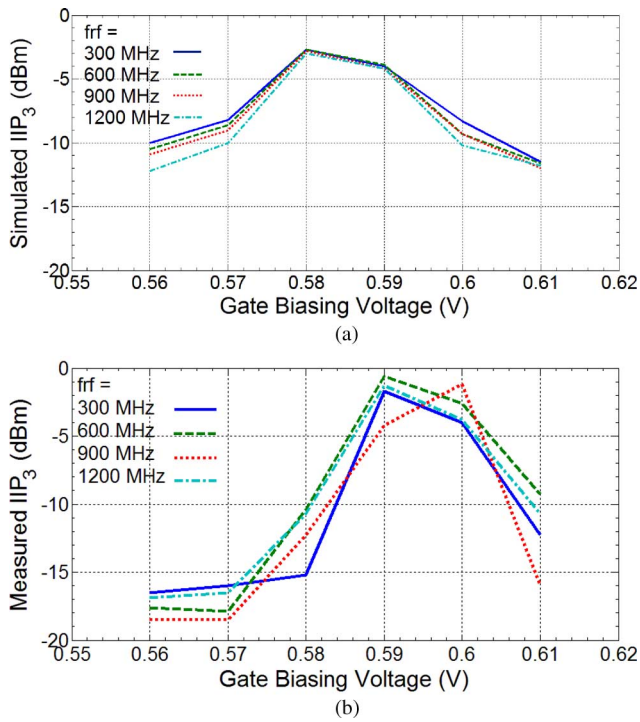

Fig. 9. IIP_3 of the CG-CS active balun versus gate bias voltage. (a) Simulated IIP_3 of the mixer as a function of transistor gate bias and RF input frequency. (b) Measured IIP_3 of the mixer as a function of transistor gate bias and RF input frequency.

and the RFIC was subsequently tested. For the measurements, the RF input frequency ranged from 300 to 1200 MHz and the IF frequency was kept fixed at 20 MHz. A passive balun is used before the differential RF input ports to generate the differential input signal.

The maximum conversion gain of the mixer was measured at 8.8 dB at a frequency of 300 MHz while the minimum was 7.1 dB at 1200 MHz and the average was 8 dB over the band. A plot of the conversion gain versus frequency is shown in Fig. 8.

The IIP_3 of the downconverter was measured using a series of two-tone tests in which the tones were kept 1 MHz apart and their center frequency swept between 300–1200 MHz in steps of 300 MHz. Furthermore, the IIP_3 was measured as the gate bias voltage of transistors $M_{2p,n}$, and $M_{3p,n}$ in Fig. 2 was varied in simultaneous fashion. The results of those measurements are plotted in Fig. 9(b) and they reveal that the optimal gate voltage for $M_{2p,n}$ and $M_{3p,n}$ to obtain maximum IIP_3 is between 0.59–0.6 V, which is very close to the theoretical value of 0.58 V predicted by Fig. 7. While the peak IIP_3 in Fig. 9(b)

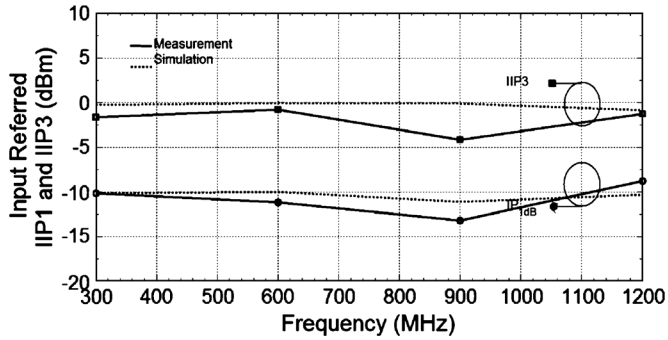

Fig. 10. IIP_3 and $\mathrm{IP}_{1\ \mathrm{dB}}$ across the RF input frequency.

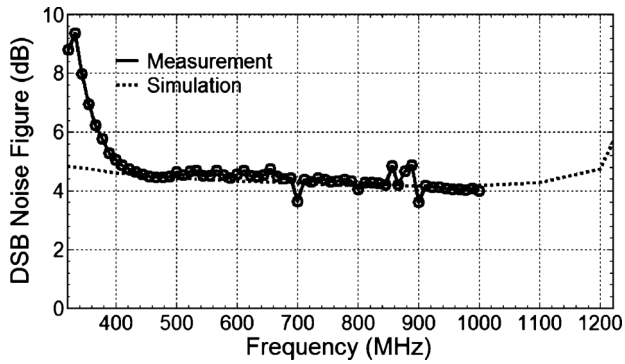

Fig. 11. Measured and simulated DSB NF across the RF input frequency.

is -0.8 dBm and the peak IIP_3 in Fig. 7 is -7.5 dBm what is more important is that both plots are consistent about the required bias voltage for best IIP_3 because it is this variable that the RFIC designer will control to maximize the IIP_3.

With the $M_{2p,n}$ and $M_{3p,n}$ gate voltages fixed at 0.59 V, the measured and simulated IIP_3 of the downconverter is plotted versus frequency in Fig. 10 along with its $\mathrm{IP}_{1\ \mathrm{dB}}$. The IIP_3 varies from -4.2 to -0.8 dBm, while the $\mathrm{IP}_{1\ \mathrm{dB}}$ is from -13.2 to -8.8 dBm over the frequency band. Both metrics are well behaved and have the same general dependence with frequency.

The double-sideband (DSB) noise figure (NF) $(\mathrm{NF}_{\mathrm{DSB}})$ was measured and is compared with simulation in Fig. 11. To measure the NF of the circuit, a spectrum analyzer is configured into the mode of measuring the DSB noise of a down-conversion mixer. A thermal noise source is attached to the RF input port and the corresponding DSB noise data at the output of the IF buffer is measured and extracted using the Y-factor method. Since a passive balun was used at the RF input port during measurements, the noise contribution of the balun was accounted for in the reported noise data. Similarly, the noise generated by the off-chip buffer is also deducted from the measured noise data even though it is attenuated by the RF-to-IF voltage gain. The $\mathrm{NF}_{\mathrm{DSB}}$ is below 4.8 dB for frequencies above 400 MHz. Below 400 MHz, the NF increases significantly due to losses in the off-chip circuitry, particularly the bias T, and $1/f$ noise also contributes to the overall degradation in NF at the lower end of the band. The NF simulations, like all others in this paper, were carried out on the post-layout extracted circuit using full *RC* parasitic modeling.

Fig. 12 shows the reflection coefficient of the downconverter at the RF port. The input match is better than -15 dB up to

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

		This Work	[3]	[5]	[20]	[21]	[7]
CMOS node		130 nm	180 nm	65 nm	180 nm	90 nm	180 nm
Supply voltage	(V)	0.9	1.8	1.0	1.1	1.2	1.0
Frequency range	(GHz)	0.3−1.2	0.8−1.1	1−10.5	3−5	0.1−3.85	0.3−4
Conversion Gain	(dB)	8.8	35	12.8	8.7	12.1	14
DSB Noise Figure	(dB)	≤4.8	9.8	7.6	14.6 to 21.6†	8.4 to 11.5†	11.0
IP_{1dB}	(dBm)	−13.2 to −8.8	−25.0	−15.0	−19.5 to −10.5	−12.83	-
IIP_3	(dBm)	−4.2 to −0.8	−9.2	−7.1	−10.7 to −0.7	-	4.1
Power consumption	(mW)	24.0	3.8	5.0	8.4	9.8	6.6

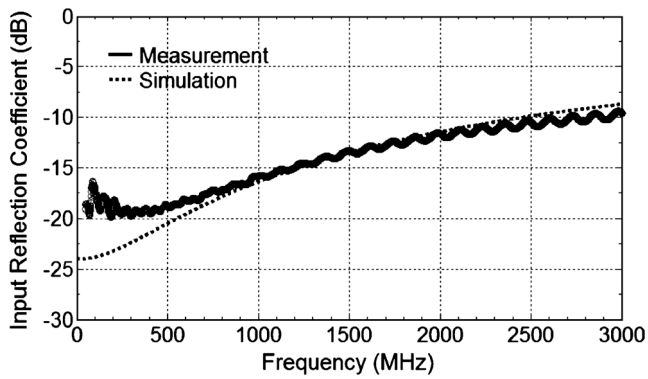

Fig. 12. Measured and simulated input reflection coefficient across the RF input frequency.

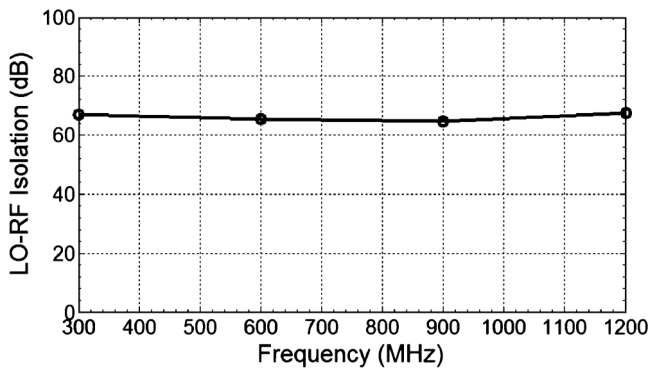

Fig. 13. Measured LO-RF isolation versus LO frequency.

1200 MHz. The measured LO-port to RF-port isolation is plotted in Fig. 13 and is below 60 dB over the band of interest.

The entire circuit draws 26.7 mA of current from a 0.9-V supply, and hence, consumes a static power of 24.0 mW. Table I compares this work with other similar works in CMOS and Fig. 14 shows a microphotograph of the chip. The chip occupies an area of 0.7 mm × 0.8 mm. To demonstrate the noise-canceling advantage of the CG-CS noise canceling transconductor, a high CS transconductance value was chosen in spite of our low-voltage constraint. As we are aggressively trading off power consumption for noise performance, the power consumption could also be greatly reduced if a higher NF can be tolerated. If the same transconductance is achieved with lower current consumption, then the design approach taken here is even more attractive.

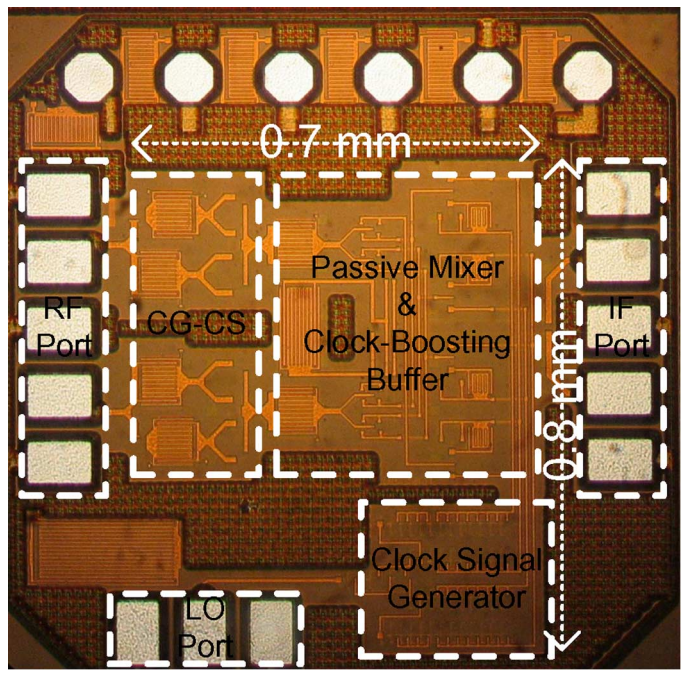

Fig. 14. Microphotograph of the fabricated RFIC. The chip occupies an area of 0.7 mm × 0.8 mm.

V. CONCLUSION

A detailed Volterra-series analysis of distortion phenomena in a low-voltage wideband downconverter mixer has been carried out. A chip was fabricated and tested and the measured results confirm the validity of the analysis and design technique. The insights gained through the analysis are applicable to other mixer configurations, particularly those that make use of CG-CS transconductor stages at the RF input.

APPENDIX
DERIVATION OF THE VOLTERRA OPERATORS

To obtain (4)– (6), the matrix inverse of the generic KCL kernel in (2) and (3), denoted as A^{-1}, is first computed using (17),

$$A^{-1} = \begin{pmatrix} g_{m1}+g_{ds1}+Y_0(\sum\omega)+Y_s(\sum\omega) & -g_{ds1} \\ g_{m1}+g_{ds1} & -(g_{ds1}+Y_1(\sum\omega)) \end{pmatrix}^{-1} \quad (17)$$

$$V(\sum\omega)=\frac{1}{(g_{m1}+g_{ds1})Y_1(\sum\omega)+(g_{ds1}+Y_1(\sum\omega))\,(Y_0(\sum\omega)+Y_s(\sum\omega))} \tag{20}$$

From the generic KCL (2) and (3), the first-, second-, and third-order KCL equations can be found to be all of the form $Ax=b$,

$$A\begin{pmatrix}A_1(\omega_1)\\B_1(\omega_1)\end{pmatrix}=\begin{pmatrix}Y_s\\0\end{pmatrix} \tag{18}$$

$$\begin{aligned}\begin{pmatrix}A_1(\omega_1)\\B_1(\omega_1)\end{pmatrix}&=A^{-1}\begin{pmatrix}Y_s\\0\end{pmatrix}\\&=V(\omega_1)\begin{pmatrix}(g_{ds1}+Y_1(\omega_1))\,Y_s\\(g_{m1}+g_{ds1})Y_s\end{pmatrix}\end{aligned} \tag{19}$$

where for notation simplicity, define the term $V(\sum\omega)$, as shown in (20), at the top of this page. For the computation of $A_2(\omega_1,\omega_2)$ and $B_2(\omega_1,\omega_2)$, we use the following expression in (21):

$$\begin{aligned}\begin{pmatrix}A_2(\omega_1,\omega_2)\\B_2(\omega_1,\omega_2)\end{pmatrix}=&A^{-1}\,[-(g_{m2}+g_{ds2})A_1(\omega_1)A_1(\omega_2)\\&+g_{ds2}A_1(\omega_1)B_1(\omega_2)\\&-g_{ds2}B_1(\omega_1)B_1(\omega_2),\\&-(g_{m2}+g_{ds2})A_1(\omega_1)A_1(\omega_2)\\&+g_{ds2}A_1(\omega_1)B_1(\omega_2)\\&-g_{ds2}B_1(\omega_1)B_1(\omega_2)]\\=&V(\omega_1+\omega_2)\Big[-(g_{m2}+g_{ds2})A_1(\omega_1)A_1(\omega_2)\\&+g_{ds2}(\overline{A_1(\omega_1)B_1(\omega_2)}\\&-B_1(\omega_1)B_1(\omega_2))\Big]\\&\times\begin{pmatrix}Y_1(\omega_1+\omega_2)\\-(Y_0(\omega_1+\omega_2)+Y_s)\end{pmatrix}\end{aligned} \tag{21}$$

and for the computation of $A_3(\omega_1,\omega_2,\omega_3)$ and $B_3(\omega_1,\omega_2,\omega_3)$, we use

$$\begin{pmatrix}A_3(\omega_1,\omega_2,\omega_3)\\B_3(\omega_1,\omega_2,\omega_3)\end{pmatrix}=A^{-1}\times S\times\begin{pmatrix}1\\1\end{pmatrix} \tag{22}$$

where S is given by (23)

$$\begin{aligned}S=&-2(g_{m2}+g_{ds2})\overline{A_1(\omega_1)A_2(\omega_2,\omega_3)}\\&-2g_{ds2}\overline{B_1(\omega_1)B_1(\omega_2,\omega_3)}\\&+2g_{ds2}(\overline{A_1(\omega_1)B_2(\omega_2,\omega_3)}\\&+\overline{B_1(\omega_1)A_2(\omega_2,\omega_3)})\\&-(g_{m3}+g_{ds3})A_1(\omega_1)A_1(\omega_2)A_1(\omega_3)\\&+3g_{ds3}\overline{A_1(\omega_1)A_1(\omega_2)B_1(\omega_3)}\\&-3g_{ds3}\overline{A_1(\omega_1)B_1(\omega_2)B_1(\omega_3)}\\&+g_{ds3}B_1(\omega_1)B_1(\omega_2)B_1(\omega_3).\end{aligned} \tag{23}$$

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