Extending the bandwidth of low-noise microwave amplifier through digital assist

D. Stewart and C. E. Saavedra

The 3 dB bandwidth of a low-noise amplifier (LNA) is increased by 23% from a range of 1–6.7 GHz to a range of 1–8.25 GHz through digital assist. The LNA has a multi-stage topology and the gate bias voltages are dynamically optimised in real-time to obtain the best gain and noise figure as a function of the signal input frequency.

Introduction: Although digital assist (DA) has been successfully used to improve the performance of microwave power amplifiers (PAs) [1–3], the application of DA to low-noise amplifiers (LNAs) has been less studied to date. This is partly because LNAs, by virtue of being small-circuits, are easier to model and optimise before production compared with PAs. By tapping the enormous computational processing power available in today's smartphones, microwave circuit designers now have the means to significantly improve the performance of small-signal circuits like LNAs at virtually zero extra cost. In this Letter, we experimentally demonstrate a DA technique that extends the 3 dB bandwidth of a radio-frequency integrated circuit (RFIC) LNA designed in-house. In the proposed method, the frequency of the incident microwave signal is detected with an on-chip frequency discriminator and a microcontroller subsequently adjusts the bias voltages of the LNA, in real-time, to yield the best gain at the frequency of interest. Measurements show that the LNA's noise figure (NF) and input match are almost unchanged whether the DA circuitry is on or off.

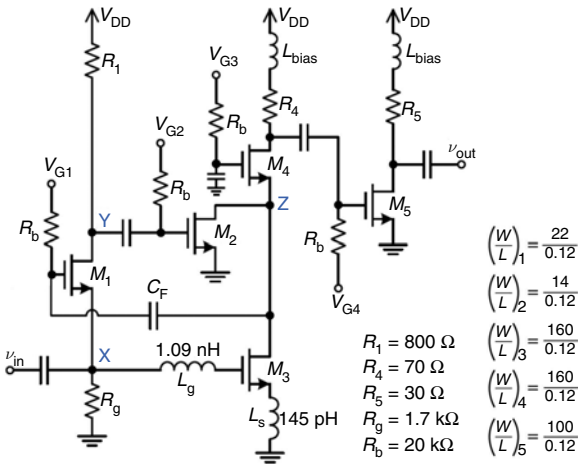

Fig. 1 *Schematic diagram of LNA (device dimensions in μm)*

RFIC design: Fig. 1 is the schematic diagram of the LNA circuit that we designed as a test case for the proposed DA method. The LNA is a multi-stage circuit that employs the concept of noise-cancellation to obtain a wideband frequency response [4, 5]. Transistors M_1 to M_3 constitute the first amplification stage and it is also where the noise-cancellation occurs. The signal of interest, v_{in}, splits into two parallel paths and is amplified by M_1 and M_2 in the top path and is also amplified by M_3 in the bottom path. When the signals from each path are summed at node Z, they add constructively in the current domain. The NF of the LNA is dominated by the thermal noise generated in the channel of transistor M_1. The noise currents flowing out of M_1 have the same magnitude, but are out-of-phase at nodes X and Y, and when they are summed at node Z, they interfere destructively, thus minimising the NF. Capacitor C_F provides voltage feedback at the LNA input, which reduces the impedance at M_1's source terminal, whereas inductor L_g is used to mitigate the noise contribution of M_3 and for gain peaking at the high frequency-end of the amplifier's operating band. The inductor L_s helps to minimise the input insertion loss of the LNA. The second LNA stage is a common-gate (CG) transimpedance amplifier and uses only one transistor, M_4. Since the first LNA stage produces an output signal current, the CG amplifier's low input impedance makes it a good choice as a load to the first stage. The third and final LNA stage uses device M_5 as a common-emitter amplifier.

The proposed DA method requires knowledge of the input signal frequency to determine the optimal transistor gate bias voltages that will yield the best gain at that frequency point. To this end, we implemented a basic frequency discriminator circuit after the LNA that maps each input frequency to a distinct DC voltage. The discriminator, depicted in Fig. 2, uses a chain of differential amplifiers with active feedback that function as a limiting amplifier [6] to clamp the amplitude of the sampled RF signal to the same level for all frequencies. A one-pole lowpass filter with a 3 dB cutoff frequency below 1 GHz follows the limiting amplifier to discriminate the different input frequencies. The last stage of the discriminator is a broadband, compact, CMOS-based power detector [7] that produces the discriminator's DC output voltage.

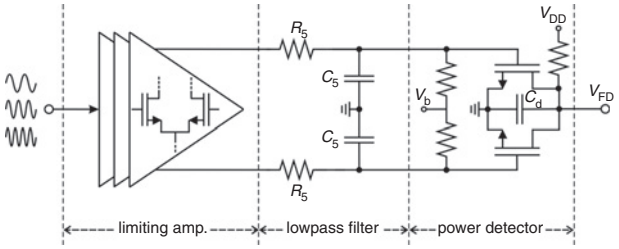

Fig. 2 *Simplified schematic of CMOS frequency discriminator*

DA implementation: The block diagram of the proposed DA method to extend the bandwidth of the LNA is shown in Fig. 3. An analogue-to-digital converter in the microcontroller reads the frequency discriminator's output voltage, V_{FD}. The microcontroller then uses a look-up table (LUT) containing the discriminator's previously characterised V_{FD} against frequency response to determine the frequency of the LNA's input signal. If the acquired voltage V_{FD} is not found in the LUT, a linear interpolation subroutine is executed that uses the two nearest data points in the LUT to estimate the frequency.

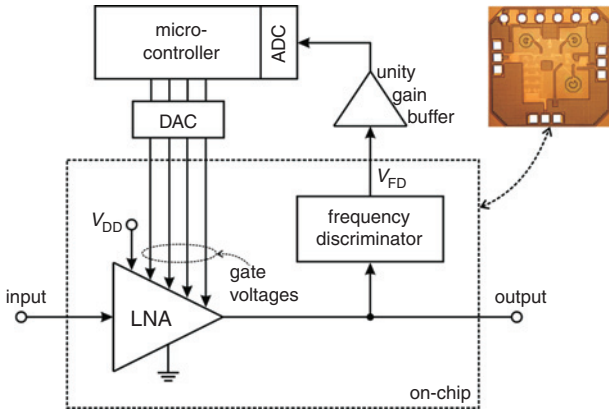

Fig. 3 *Concept to extend bandwidth of LNA through DA*

With the incident frequency established, the next step is to determine the LNA gate bias voltages that yield the best performance at that frequency. The gate bias voltages are applied to the LNA chip after they have been converted to analogue voltages using a digital-to-analogue converter plus a second LUT that contains the optimal gate bias voltages as a function of frequency. The voltage bias data stored in the LUT were found by characterising the baseline LNA (i.e. without DA) at discrete signal frequency points and tuning the gate voltages until the optimal performance was found. To minimise the amount of time spent on characterisation and to keep the LUT to a reasonable size, data were taken at 1 GHz intervals over the range of 1–9 GHz for a total of only nine frequency measurement points. As before, a linear interpolation routine is executed to find the bias voltages when the frequency falls between stored data points.

Experimental results: The RFIC containing the LNA and the frequency discriminator was fabricated using IBM's 8RF-DM 130 nm CMOS process. The microcontroller used in this demonstration was a PIC18F87J11 from Microchip Technology.

Fig. 4 contains a plot of the LNA's measured gain with and without the use of DA. The baseline LNA without DA has a 3 dB bandwidth of 6.7 GHz and, when the DA is applied, the bandwidth is extended to 8.25 GHz. The flattening of the LNA's gain response comes with a

small penalty of 1.5 dB in its peak gain. The plots in Figs. 5 and 6 show the effect that DA has on the LNA's input return loss and its NF, respectively, and we observe that the impact on each metric is negligible.

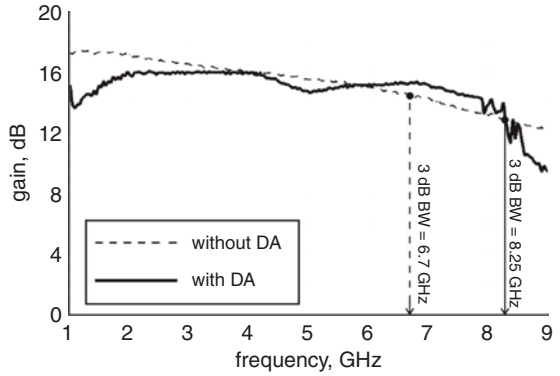

Fig. 4 *LNA measured gain*

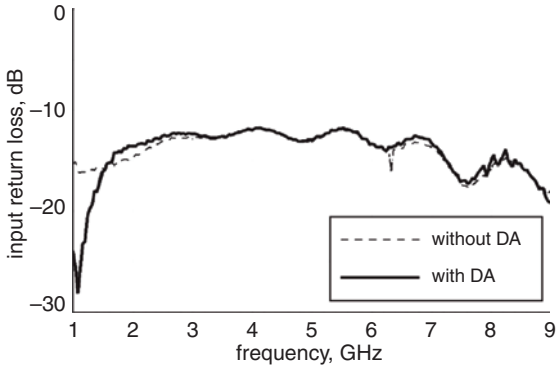

Fig. 5 *LNA measured input return loss*

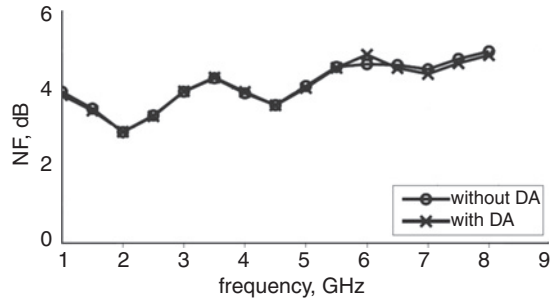

Fig. 6 *LNA measured NF*

The power response and the third-order intermodulation distortion (IMD3) performance of the LNA with DA were measured over the band of interest. At the mid-band frequency of 4 GHz, the LNA's IP_{1dB} is −15.4 dBm and its OP_{1dB} is −0.3 dBm. Using two tones spaced 1 MHz apart and centred at 4 GHz, the LNA's IIP_3 comes out to −5.4 dBm and its OIP^3 is +5.8 dBm.

Conclusion: We have demonstrated a DA method to flatten the gain of a microwave LNA and thereby extend its 3 dB bandwidth by 23% without degrading the LNA's input return loss or its NF. The proposed DA method is not computationally intensive and would be very simple to implement on a smartphone or other modern communications hardware.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Palaskas, Y., Taylor, S., Pellerano, S., Rippke, I., Bishop, R., Ravi, A., Lakdawala, H., and Soumyanath, K.: 'A 5-GHz 20-dBm power amplifier with digitally assisted AM-PM correction in a 90-nm CMOS process', *IEEE J. Solid-State Circuits*, 2006, **41**, (8), pp. 1757–1763

2 Nakatani, T., Rode, J., Kimball, D., Larson, L., and Asbeck, P.: 'Digitally controlled polar transmitter using a watt-class current-mode class-D CMOS power amplifier and guanella reverse balun for handset applications', *IEEE J. Solid-State Circuits*, 2012, **47**, (5), pp. 1104–1112

3 El-Gabaly, A., Stewart, D., and Saavedra, C.: '2-W broadband GaN power-amplifier RFIC using the f_T doubling technique and digitally assisted distortion cancellation', *IEEE Trans. Microw. Theory Tech.*, 2013, **61**, (1), pp. 525–532

4 Bruccoleri, F., Klumperink, E., and Nauta, B.: 'Noise cancelling in wideband CMOS LNAs'. IEEE Int. Solid-State Circuits Conf., San Francisco, CA, USA, February 2002, Vol. 1, pp. 406–407

5 Bevilacqua, A., and Niknejad, A.: 'An ultrawideband CMOS low-noise amplifier for 3.1–10.6 GHz wireless receivers', *IEEE J. Solid-State Circuits*, 2004, **39**, (12), pp. 2259–2268

6 Huang, H.-Y., Chien, J.-C., and Lu, L.-H.: 'A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback', *IEEE J. Solid-State Circuits*, 2007, **42**, (5), pp. 1111–1120

7 Li, C., Gong, F., and Wang, P.: 'A low-power ultrawideband CMOS power detector with an embedded amplifier', *IEEE Trans. Instrum. Meas.*, 2010, **59**, (12), pp. 3270–3278