A 3–10-GHz 13-pJ/Pulse Dual BPSK/QPSK Pulse Modulator Based on Harmonic Injection Locking

Ahmed M. El-Gabaly, *Member, IEEE*, and Carlos E. Saavedra, *Senior Member, IEEE*

***Abstract*—A method is presented to phase-modulate RF pulses through an injection-locking technique. The modulator can produce either binary phase-shift keying or quadrature phase-shift keying modulated wave packets (pulses). The RF pulses are produced using a fast on/off switching technique to power up and power down a tunable ring oscillator whose free-running frequency can be tuned from 3 to 10 GHz. Experiments show that the modulator's minimum energy consumption is 13 pJ/pulse for a carrier frequency of 3 GHz, while its maximum consumption is 18 pJ/pulse when the carrier frequency is 10 GHz. The energy consumption figures are for 2-ns-long pulses with amplitudes of 300 mV at 3 GHz and 200 mV at 10 GHz. The pulse repetition rate is 250 MHz. The measured root-mean-square jitter of the oscillator, integrated from 100 Hz to 1 MHz, is below 3.6 ps. The chip was fabricated in 130-nm CMOS and it occupies a total area of 0.85 mm^2 including bonding pads while the active circuit area is 0.05 mm^2.**

***Index Terms*—Binary phase-shift keying (BPSK), CMOS, clock, delay stage, harmonic injection, injection locking, impulse radio, low energy, monolithic microwave integrated circuit (MMIC), pulse modulation, phase noise (PN), pJ/pulse, quadrature phase-shift keying (QPSK), quadrature oscillator, RF, ring oscillator, ultra-wideband (UWB), wave packets.**

I. Introduction

INJECTION-LOCKED oscillators are regularly used in analog and RF systems to carry out functions such as quadrature signal generation, frequency division, and beam scanning in antenna arrays [1]–[5]. While injection locking is by no means the only viable approach to carry out the aforementioned functions, the competitive advantage of the approach are its minimal area requirements and energy efficiency. The phenomenon of injection locking can also be used to phase modulate a carrier signal. Prior art on injection-locked modulators have used active antennas on printed circuit boards [6] or optoelectronic circuits [7], neither of which is directly applicable to CMOS RF integrated circuits (RFICs). In addition, prior works have focused on continuous-wave (CW) modulation, and none, to our knowledge, have explored pulse modulation.

Manuscript received June 29, 2014; revised September 17, 2014; accepted October 09, 2014. Date of publication November 03, 2014; date of current version December 02, 2014. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) under a grant. This paper is an expanded version from the IEEE MTT-S International Microwave Symposium, Tampa Bay, FL, USA, June 1–6, 2014.

A. M. El-Gabaly was with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, K7L 3N6 Canada. He is now with Peraso Technologies Inc., Toronto, ON, Canada M5J 2L7 (e-mail: ahmed.elgabaly@gmail.com).

C. E. Saavedra is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada K7L 3N6 (e-mail: saavedra@queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2014.2364224

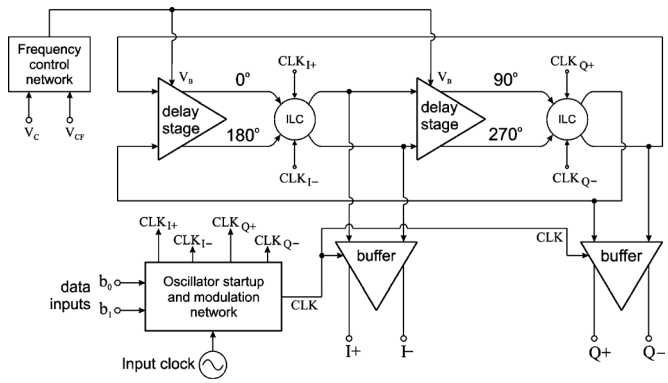


Fig. 1. Block diagram of the dual BPSK and QPSK pulse modulator.

This paper reports on how to generate short-duration carrier pulses that can be modulated with either binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK) modulation through a novel harmonic injection method. The carrier frequency of the pulses is tunable over the range of 3–10 GHz and by injecting brief current impulses at specific places in the ring structure to kick-start the oscillations, the RF pulses have a predictable and consistent phase angle relative to the system clock signal. It is this phenomenon that we exploit to generate BPSK and QPSK modulation. To demonstrate the validity of the concept, we designed and tested a chip fabricated using a standard 130-nm CMOS process. The chip can yield modulated pulses of 2-ns duration at a repetition rate of 250 MHz, while consuming 13 pJ/pulse of energy for an RF pulse frequency of 3 GHz. The maximum energy consumption is 18 pJ/pulse for an RF pulse frequency of 10 GHz. Here, we go beyond the work reported in our recent paper [8] and we develop an analytic model that captures how the circuit produces the phase-modulated signals. We also present additional data that demonstrate the circuit's frequency tuning and QPSK modulation capabilities over the entire 3–10-GHz span.

II. Pulse-Modulator Description

A circuit diagram of the 3–10-GHz pulse modulator is shown in Fig. 1. The quadrature ring oscillator and the output buffers are simultaneously pulsed on and off using a clock signal (CLK). The modulated output signals $(I+, I-, Q+, Q-)$ are taken at the output of the buffers. The carrier frequency is changed by varying the signal path delay around the ring oscillator loop. The system accepts two control voltages: V_C and V_{CF} for coarse and fine frequency tuning, respectively.

0018-9480 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

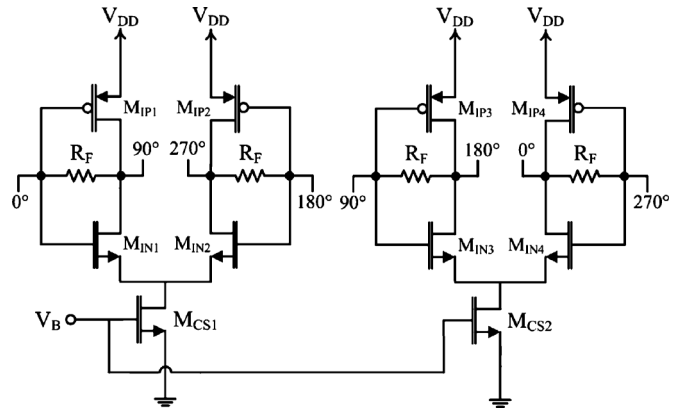


Fig. 2. Schematic diagram of the delay circuits.

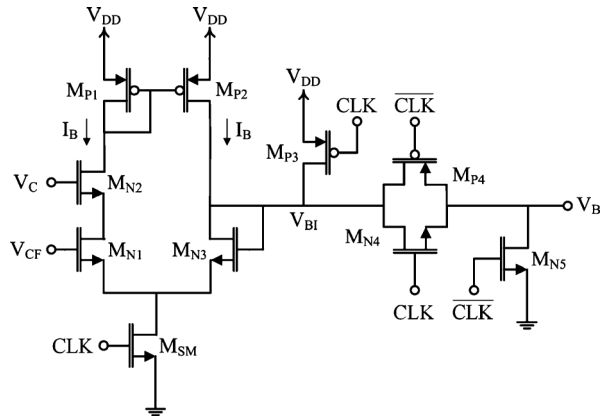


Fig. 3. Circuit schematic of the frequency control network used for the delay stages.

The ring oscillator is stabilized through injection locking to a harmonic of the system clock signal. The injection-locking circuits (ILCs) accept complementary clock signals, $\mathrm{CLK}_{I\pm}$ and $\mathrm{CLK}_{Q\pm}$, and they are used to modulate the output pulses. A startup network is used to produce four clock signals, $\mathrm{CLK}_{I\pm}$ and $\mathrm{CLK}_{Q\pm}$, in a time sequence determined by the input data bits, b_0 and b_1, which modulate the carrier pulses. If two independent bit streams (b_0, b_1) are used to feed data to the modulator, then QPSK modulation is produced, and if only one common bit stream $(b_0, b_1 = b_0)$ is used, then BPSK modulation is produced. This dual BPSK/QPSK modulator does not need passive phase shifting or power splitting/combining structures to produce the in-phase/quadrature-phase (I/Q) signals, and as a result, it occupies only a minimal amount of chip area.

A. Quadrature Ring Oscillator

A quadrature ring oscillator was selected in this design due to its small area footprint and its large frequency tuning range [9]–[12]. In addition, the fast startup time of a ring oscillator makes it particularly useful for short-pulse generation. The ring-oscillator's comparatively high phase noise (PN) can be mitigated by injection locking it to a stable source [13], [14].

Fig. 2 shows the circuit schematic of the delay stages used in the ring oscillator in Fig. 1. The delay stage has two CMOS inverters ($\mathrm{M}_{IP1} - \mathrm{M}_{\mathrm{IN1}}$ and $\mathrm{M}_{IP2} - \mathrm{M}_{\mathrm{IN2}}$) in a differential arrangement. Using CMOS inverters provides a fairly stable output voltage swing over the large variation in bias current as the frequency is tuned from 3 to 10 GHz. Resistor R_F provides shunt–shunt feedback to the inverters, which further stabilizes the amplitude of the sinusoidal output signal. The propagation delay through the CMOS inverters, which establishes the output frequency of the circuit, is determined by the time it takes to charge and discharge the parasitic capacitances at the terminals of the inverters. Thus, frequency tuning in the ring oscillator under discussion occurs through the gate–source voltage of transistor M_{CS1} (and M_{CS2}), which supplies the CMOS inverters with the current needed to charge and discharge the parasitic capacitors.

The frequency control network for the ring oscillator is shown in Fig. 3. The coarse (V_C) and fine (V_{CF}) frequency-tuning voltages are used to change the channel resistance of transistors M_{N1} and M_{N2}. This, in turn, changes how much current, I_B, flows through the current mirror $\mathrm{M}_{P1} - \mathrm{M}_{P2}$ and ultimately establishes the value of the voltages $V_{BI} V_B$ as well. Transistor M_{N2} is 15 times wider than M_{N1}, making its channel resistance significantly smaller. Therefore, the combined resistance of M_{N1} and M_{N2} changes by a smaller amount with V_{CF} compared to V_C, giving rise to smaller variations in current I_B for finer frequency tuning. The rise time of V_{BI} and V_B determines the settling time of the ring oscillator. When V_C is small, the current I_B is low and the rise time of V_{BI} and V_B is large. To mitigate this effect, transistor M_{P3} is used to precharge node V_{BI} to the supply voltage V_{DD} before turning on the ring oscillator. This increases the current I_B at the turn-on instant, allowing voltages V_{BI} and V_B to settle more quickly, producing a shorter startup time for the oscillator. Conversely, to properly switch off the oscillator, transistor M_{N5} is used to quickly discharge node V_B to ground after the turn-off instant.

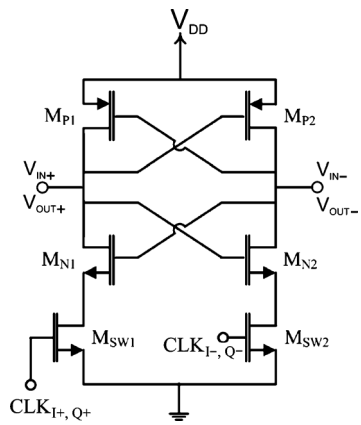


Fig. 4. ILC schematic.

The ILCs in Fig. 1 each have two inverters in a self-reinforcing loop, as shown in Fig. 4. The pMOS devices in the latch have been drawn as a cross-coupled pair and similarly for the nMOS devices. The bias current on the left-hand side of Fig. 4 is controlled by the clock signal CLK_{I+}, while the current on the right-hand side is controlled by CLK_{I-}. Since the ring oscillator uses two delay cells, the latch bias current on the second delay cell is controlled by CLK_{Q+} and CLK_{Q-}.

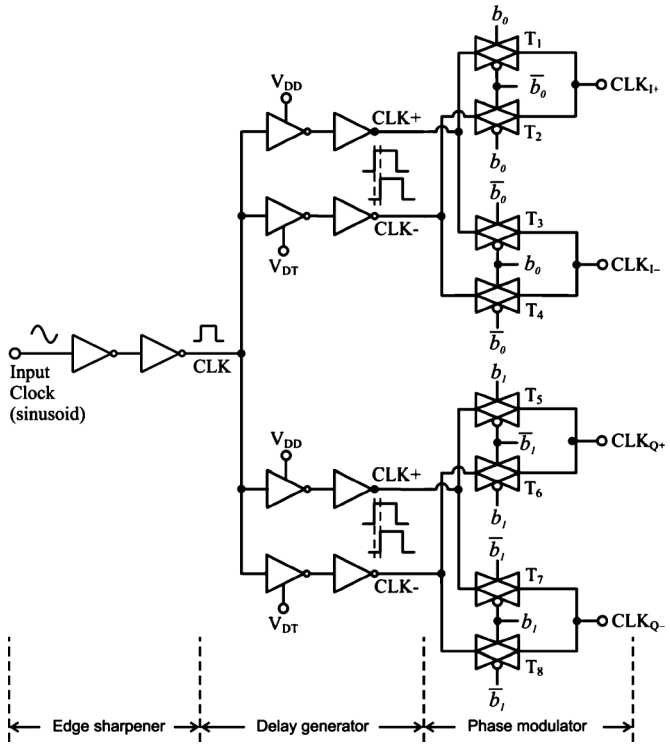


Fig. 5. Circuit schematic of the startup and modulation network.

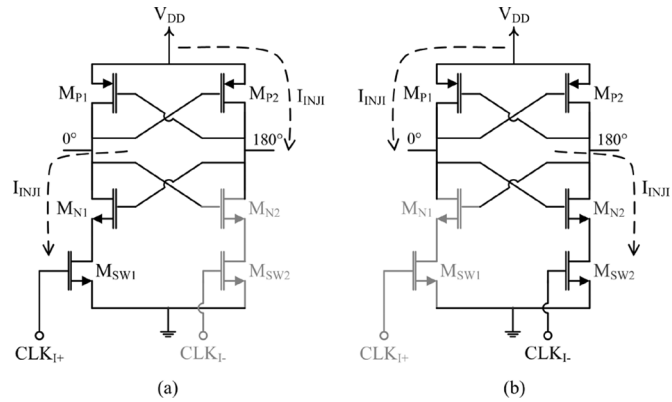


Fig. 6. Injected current $I_{\mathrm{INJ}I}$ flow when: (a) $b_0 = 1$ and (b) $b_0 = 0$.

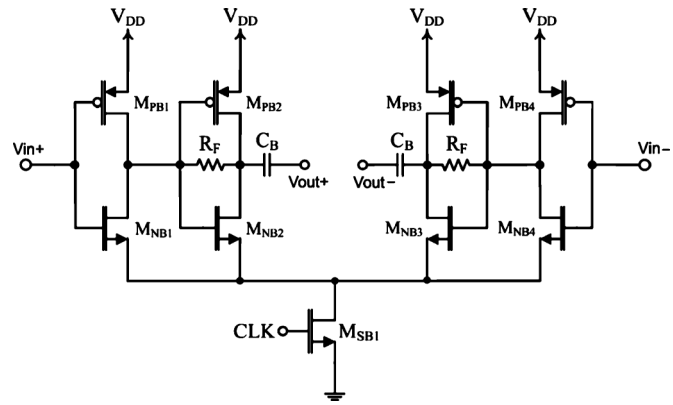


Fig. 7. Buffer circuit schematic.

B. Oscillator Startup Network

To produce very short-duration pulses, the oscillator must turn on and off quickly, and therefore, a startup network was used to speed up the onset of oscillations. The circuit schematic of the startup network, which is also used for modulation, is depicted in Fig. 5. Two CMOS inverters are used to transform a 250-MHz sinusoidal input signal into a square-wave clock, CLK. Afterwards, current-starved inverters split the signal CLK into two signals $\mathrm{CLK}+$ and $\mathrm{CLK}-$ with a very short time delay between them, on the order of tens of picoseconds. The delay between the clocks is controlled through the voltage V_{DT}. Four transmission-gate multiplexers $T_1 - T_2, T_3 - T_4, T_5 - T_6$, and $T_7 - T_8$ are employed to route $\mathrm{CLK}+$ and $\mathrm{CLK}-$ to $\mathrm{CLK}_{I+}, \mathrm{CLK}_{I-}, \mathrm{CLK}_{Q+}$, and CLK_{Q-}, which are used in the ILCs. If data bit $b_0 = 1$, the multiplexers will pass $\mathrm{CLK}+$ and $\mathrm{CLK}-$ through to CLK_{I+} and CLK_{I-}, respectively. Conversely, if $b_0 = 0$, then $\mathrm{CLK}+$ and $\mathrm{CLK}-$ are passed on to CLK_{I-} and CLK_{I+}, respectively. A similar process occurs with the quadrature clock signals, CLK_{Q+} and CLK_{Q-}, when data bit b_1 changes between 1 and 0.

The bias currents of the cross-coupled pairs in the ILCs are switched on and off using a pair of nMOS switches $M_{\mathrm{SW1}} - M_{\mathrm{SW2}}$, as shown in Fig. 4. By turning on one side of each cross-coupled pair just before the other, say, switching on M_{SW1} before M_{SW2}, an initial current $I_{\mathrm{INJ}I}$ flows for a short time through the oscillator nodes, as shown in Fig. 6. In effect, a current impulse is injected at the oscillator nodes, which quickly starts up the oscillations. It also sets the initial phase of the oscillations at the turn-on instant. By setting the same initial oscillation phase at each clock rising edge, the LO pulses are *phase coherent with the input clock* and pulse-to-pulse coherency is maintained.

The triggering order of switches M_{SW1} and M_{SW2} determines the direction of the injected current impulse $I_{\mathrm{INJ}I}$, as illustrated in Fig. 6. If data bit $b_0 = 1$, switch M_{SW1} activates before M_{SW2} and the injected current $I_{\mathrm{INJ}I}$ flows in the direction shown in Fig. 6(a). If $b_0 = 0$, switch M_{SW2} activates before M_{SW1}, reversing the direction of the injected current $I_{\mathrm{INJ}I}$, as depicted in Fig. 6(b). A similar process occurs in the second ILC, which is in the quadrature (Q) signal path and is controlled by data bit b_1. In sum, the data bits b_0 and b_1 determine the direction of the injected current impulses $I_{\mathrm{INJI},Q}$ and the oscillation phase takes on one of four quadrature values to implement quadrature modulation. The current injection method depicted in Fig. 6 can also be used in systems that operate up to 24 GHz and beyond [15].

C. Output Buffers

Fig. 7 contains the schematic of the buffer circuit used to isolate the oscillator ring from the 50-Ω system impedance of the test equipment. The buffer employs a CMOS inverter-based Cherry–Hooper topology $(M_{PB1} - M_{NB1}, M_{PB2} - M_{NB2})$ to obtain broadband frequency response [16], [17]. The feedback resistor R_F reduces the input and output resistance of the second stage $(M_{PB2} - M_{NB2})$, which also helps to increase the frequency response of the buffer because the charge and discharge time of the parasitic capacitances at those nodes is reduced.

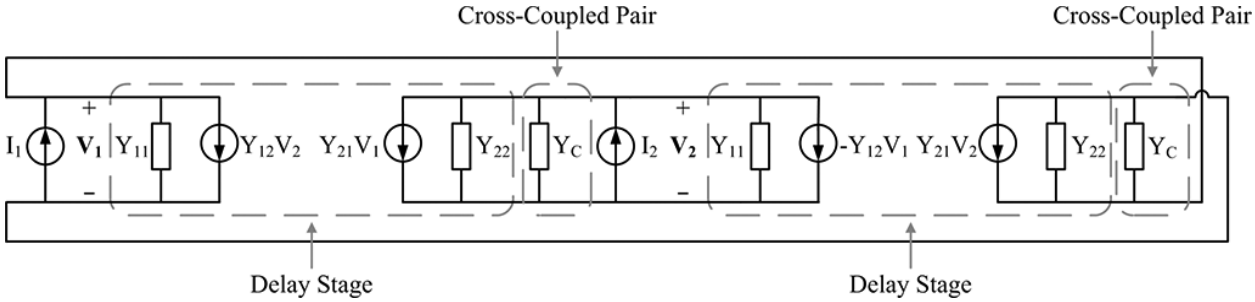


Fig. 8. Linearized Y-parameter model of the two-stage ring oscillator with injected current impulses.

III. Modeling

A linearized circuit model can be used to analyze how the system in Fig. 1 produces the modulated signals and to understand the effect of the shunt–shunt resistive feedback used in the delay stages. The circuit model, which excludes the output buffers, is shown in Fig. 8. We are interested in finding a relationship between the steady-state output voltages, $V_1(t)$ and $V_2(t)$, and the injected current stimuli into the circuit, $I_1(t)$ and $I_2(t)$, which start the oscillations and determine the phase of the output pulses (i.e., the modulation).

The delay stages are modeled using their two-port Y-parameters while the ILC is modeled by Y_C. Those admittances are given by

$$Y_{11} = 1/R_F + 1/R_{\rm IN} + j\omega C_{\rm IN} \tag{1a}$$
$$Y_{12} = -1/R_F - j\omega C_F \tag{1b}$$
$$Y_{21} = G_m - 1/R_F - j\omega C_{G_m} - j\omega C_F \tag{1c}$$
$$Y_{22} = 1/R_F + 1/R_{\rm OUT} + j\omega C_{\rm OUT} \tag{1d}$$
$$Y_C = -G_{mC} + j\omega C_C \tag{1e}$$

where R_F is the feedback resistance, $R_{\rm IN}$ and $C_{\rm IN}$ are the equivalent input resistance and capacitance, and $R_{\rm OUT}$ and $C_{\rm OUT}$ are the equivalent output resistance and capacitance of the delay stage. G_m and G_{mC} denote the dc transconductance of the delay stage and the cross-coupled pair, respectively, and C_C is the parasitic capacitance of the cross-coupled pair. The capacitance C_F is a feedback capacitance consisting of the gate–drain parasitic capacitance of the transistors $C_{\rm GD}$, while the capacitance C_{G_m} captures the frequency dependence of the transconductance due to resistive parasitics at the gate and source for example.

The circuit in Fig. 8 can now be analyzed to find the loop gain of the oscillator, $H(j\omega)$, which yields

$$H(j\omega) = -\left(\frac{Y_{21} - Y_{12}}{Y_{11} + Y_{22} - Y_c'}\right)^2 = -\left(\frac{G_m - j\omega C_{G_m}}{G_L + j\omega C_L}\right)^2 \tag{2}$$

where $G_L = 2/R_F + 1/R_{\rm IN} + 1/R_{\rm OUT} - g_{mC}$ and $C_L = C_{\rm IN} + C_{\rm OUT} + C_C$ are the effective loading conductance and capacitance, respectively, at each node. The loop gain $H(j\omega)$ in (2) must be equal to 1 for steady oscillation (Barkhausen's criterion). This gives the following oscillation frequency ω_0 and transconductance G_m:

$$\omega_0 = \frac{G_L}{C_{G_m}} \tag{3a}$$
$$G_m = \frac{G_L C_L}{C_{G_m}}. \tag{3b}$$

Equation (3a) verifies that the oscillation frequency ω_0 increases with the loading conductance G_L, and thus with smaller values of feedback resistance R_F. This is accompanied with an increase in the transconductance G_m, which occurs due to the drop in the output voltage swing about the trip point of the delay stages.

Letting $I_1(t) = A\delta(t)$ and $I_2(t) = B\delta(t)$, where $A = \pm 1$ and $B = \pm 1$, the output voltages can be written as

$$V_1(t) = A_0 \cos(\omega_0 t + \phi) \tag{4a}$$
$$V_2(t) = A_0 \sin(\omega_0 t + \phi) \tag{4b}$$

where A_0 is a constant and the phase ϕ is given by

$$\phi = \tan^{-1}\left(\frac{BC_L + AC_{G_m}}{AC_L - BC_{G_m}}\right). \tag{5}$$

Equation (5) indicates that the carrier phase depends on the signs of A and B, i.e., the direction of the injected current impulses $I_1(t)$ and $I_2(t)$. The four possible combinations of $A = \pm 1$ and $B = \pm 1$ actually yield four phases (ϕ_1, ϕ_2, ϕ_3, and ϕ_4) given by

$$\phi_1 = \tan^{-1}\left(\frac{C_L + C_{G_m}}{C_L - C_{G_m}}\right) \tag{6a}$$
$$\phi_2 = \tan^{-1}\left(\frac{C_{G_m} - C_L}{C_L + C_{G_m}}\right) = \phi_1 - 90^\circ \tag{6b}$$
$$\phi_3 = \tan^{-1}\left(\frac{-C_L - C_{G_m}}{C_{G_m} - C_L}\right) = \phi_1 - 180^\circ \tag{6c}$$
$$\phi_4 = \tan^{-1}\left(\frac{C_L - C_{G_m}}{-C_L - C_{G_m}}\right) = \phi_1 - 270^\circ. \tag{6d}$$

Quadrature modulation can thus be achieved by manipulating the direction of the current impulses I_1 and I_2 injected into the circuit.

IV. Experimental Results

The pulse modulator was fabricated using a 0.13-μm CMOS process and a photograph of the RFIC is shown in Fig. 9. The chip measures 1 mm $\times$ 0.85 mm including the bonding pads and decoupling capacitors, while the core circuit area is 255 μm $\times$ 195 μm. Chip measurements were carried out on-wafer using a spectrum analyzer and a digital sampling

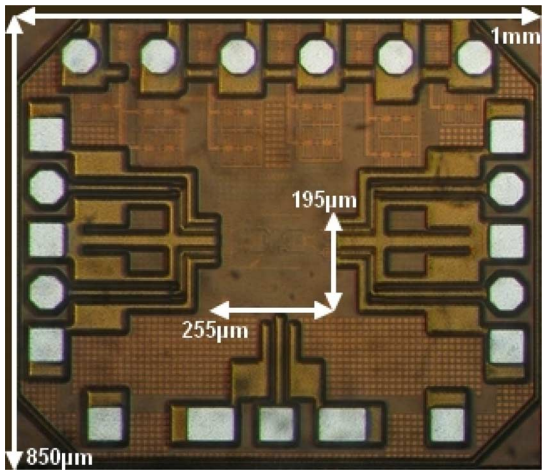


Fig. 9. Photograph of the pulse modulator integrated circuit (IC).

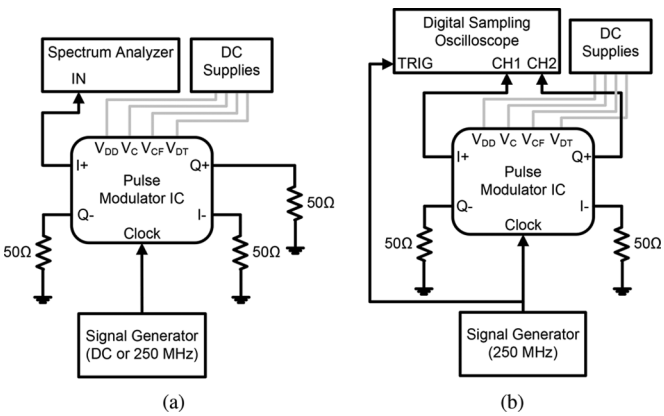


Fig. 10. Measurement setup for the pulse modulator. (a) Frequency spectrum. (b) Time domain.

oscilloscope to observe the output signal in the frequency and time domains, respectively (Fig. 10).

The ring oscillator's free-running frequency can be tuned from 3.15 to 10.07 GHz as the control voltage V_C to the delay stages is varied from 0.58 to 0.93 V. Fig. 11 is a superposition of the measured spectra of the oscillator at various output frequencies. The free-running output power level is about -6.2 dBm at 3.15 GHz, -8.3 dBm at 6.1 GHz, and -10.5 dBm at 10.07 GHz. Fig. 12 contains plots of the oscillator's output power level and signal frequency versus control voltage, V_C. The oscillator produces -8.4 ± 2 dBm of RF output power between 3.15 and 10.07 GHz.

As noted in Section II, the oscillator accepts two control voltages: one for coarse frequency tuning, V_C and another for fine frequency tuning, V_{CF}. Fig. 13 shows the fine-tuning capability of the oscillator at 3.75 and 10.07 GHz. The results indicate that the output frequency can be tuned in increments of 20 MHz for each 0.1-V step in V_{CF} when the following condition holds: 1.0 V $< V_{CF} <$ 1.5 V.

After the oscillator was characterized in CW mode, it was measured in pulsed mode using a 250-MHz clock. The input clock is a periodic sinusoidal signal, which is readily converted on-chip into a 50% duty-cycle digital square wave using the

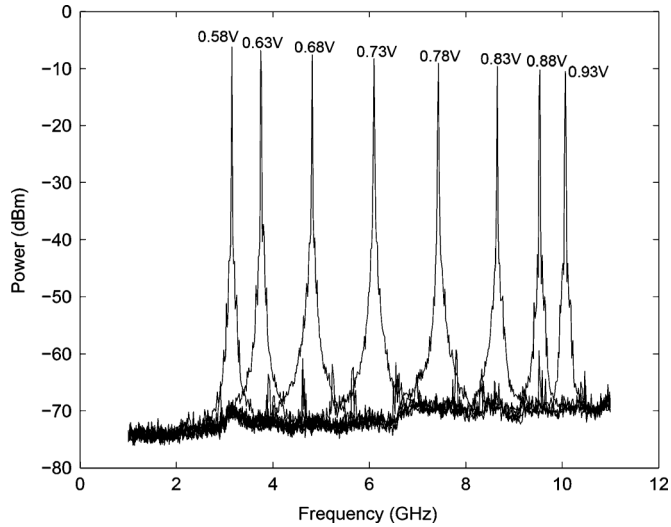


Fig. 11. Measured free-running spectra for different values of tuning voltage V_C.

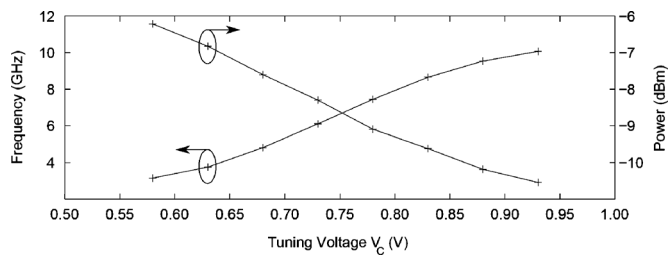


Fig. 12. Measured free-running frequency and output power with different values of V_C.

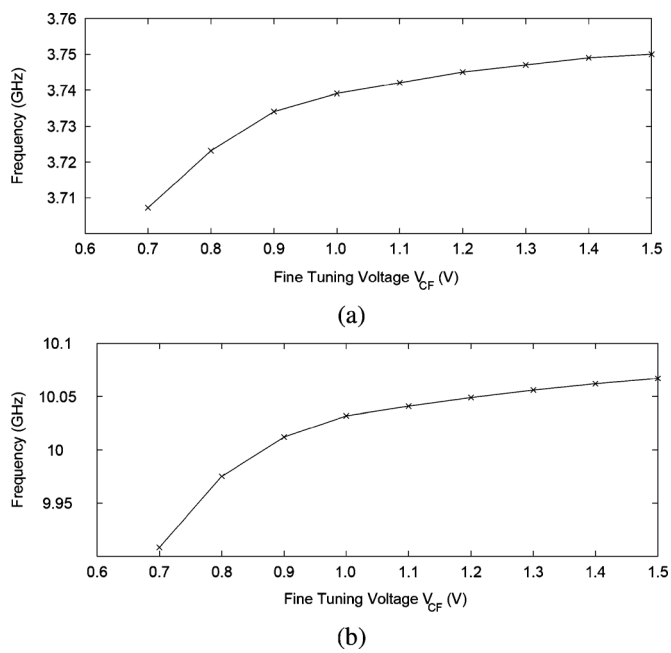


Fig. 13. Variation of the oscillation frequency with the fine tuning voltage V_{CF} at 3.75 GHz ($V_C = 0.63$ V) and 10.07 GHz ($V_C = 0.93$ V).

edge sharpening inverters (Fig. 5). Each pulse is thus generated for a duration of 2 ns and is repeated every 4 ns. The

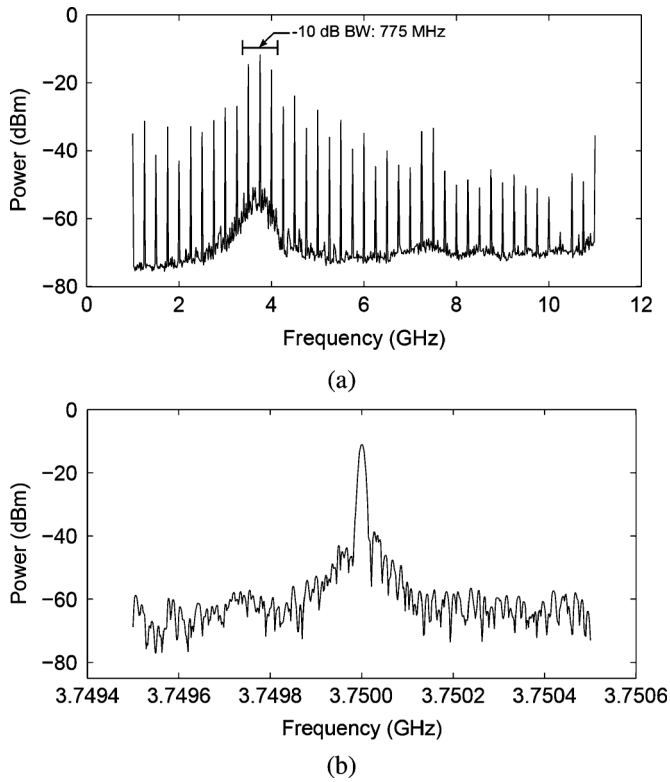


Fig. 14. Measured pulsed output spectrum at 3.75 GHz. (a) 10-GHz span. (b) 1-MHz span.

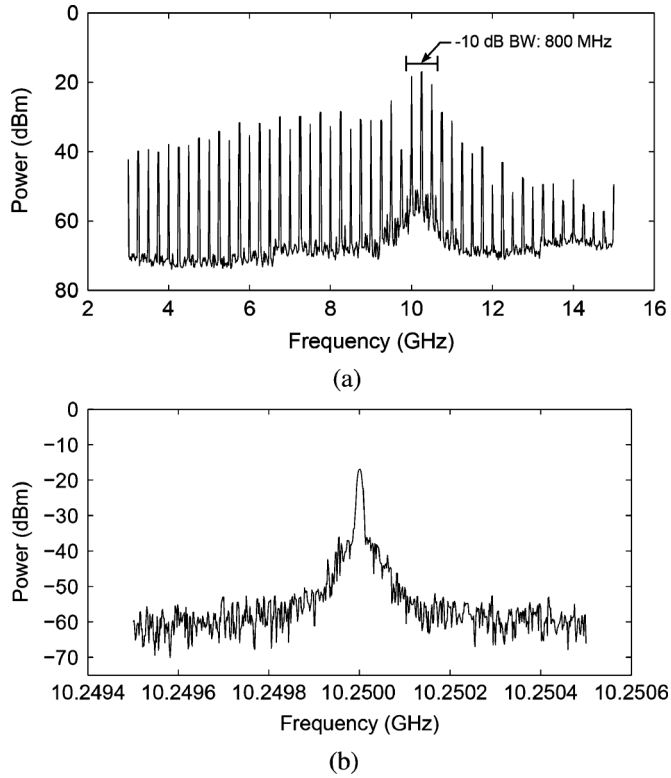


Fig. 15. Measured pulsed output spectrum at 10.25 GHz. (a) 12-GHz span. (b) 1-MHz span.

pulse duration and repetition rate can be tuned by varying the duty-cycle and frequency of the input clock signal. The upper graphs in Figs. 14 and 15 are wideband plots of the oscillator's output spectra at 3.75 and 10.25 GHz, respectively. As expected, the power spectrum exhibits peaks at multiples of the clock frequency and those harmonics of the clock are coherent and well defined. The -10-dB bandwidth of the power spectra is also higher than approximately 775 MHz. The lower graphs in Figs. 14 and 15 are close-up views (1-MHz span) of the pulsed oscillator's spectrum at the corresponding center frequencies, clearly showing stable and locked operation.

Fig. 16 shows the measured PN power spectral density (PSD) of the pulsed oscillator at 3.75 and 10.25 GHz, plus the measured PN of the 250-MHz clock reference. Basic noise theory predicts that the nth harmonic tone of a periodic signal will have a PN that is higher than the PN of the fundamental tone by the amount

$$20\log(n)\ \text{dB}. \tag{7}$$

Considering that pulsing the ring oscillator causes it to become injection locked to a harmonic of the clock signal, we expect that the oscillator's PN will track the PN of the clock signal, but offset by the amount in (7). This prediction is borne out by the plots in Fig. 16. Table I compares the expected and measured PN of the pulsed oscillator. For the calculated PN, we used (7) together with the clock's measured PN of -94 dBc/Hz (at 100-Hz offset). Altogether, the PN measurements show that the integrated root mean square (rms) jitter of the circuit is less than 3.6 ps from 100 Hz to 100 MHz.

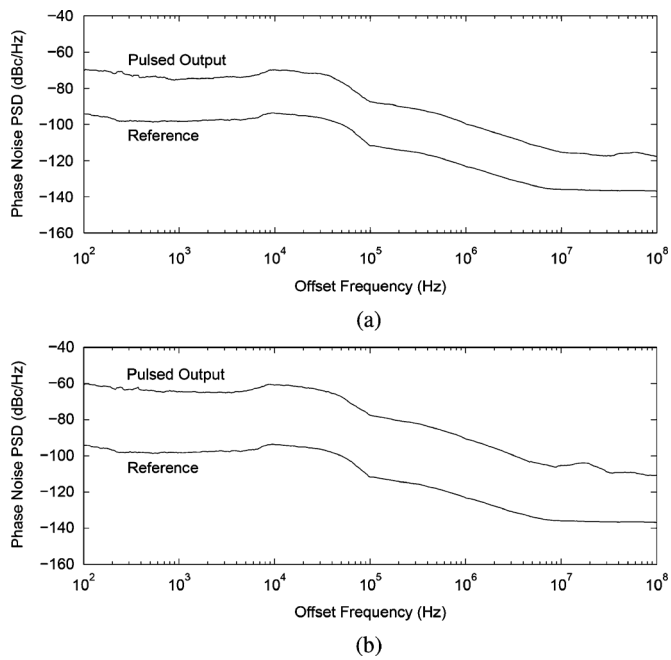


Fig. 16. Measured PN of pulsed output at: (a) 3.75 GHz and (b) 10.25 GHz.

TABLE I
PULSED OSCILLATOR PN

Pulsed Osc. Freq. (GHz)	Harmonic number (n)	Predicted PN (dBc/Hz)	Measured PN (dBc/Hz)
3.75	15	-71	-70
6.75	27	-65	-64
10.25	41	-62	-61

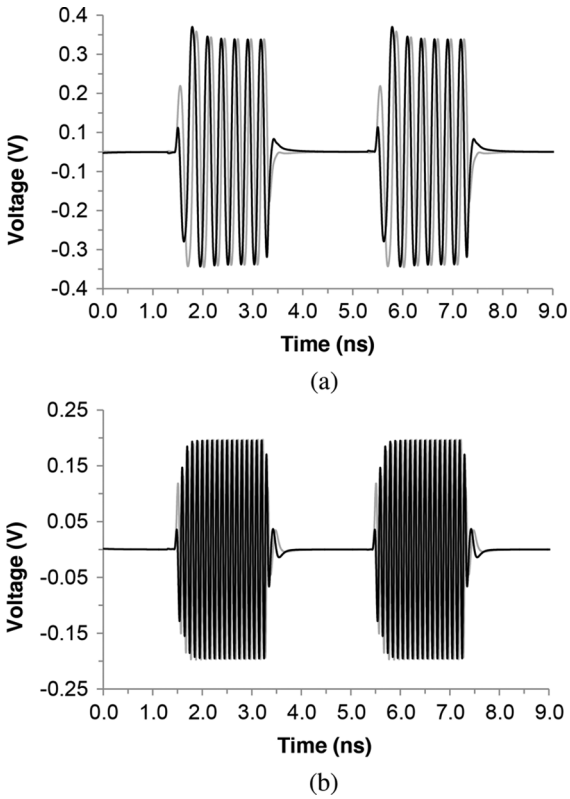


Fig. 17. Simulated pulsed I ($I_+ - I_-$) and Q ($Q_+ - Q_-$) outputs in the time-domain at: (a) 3.75 GHz and (b) 10.25 GHz.

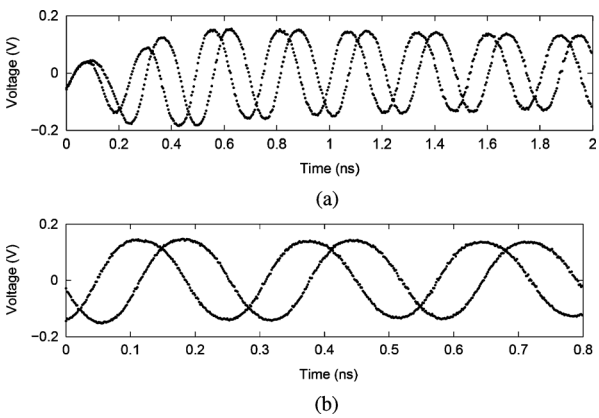


Fig. 18. Measured pulsed $I+$ and $Q+$ outputs in the time domain at 3.75 GHz: (a) from 0 to 2 ns and (b) three cycles starting from 0.96 ns.

Fig. 17 shows the pulsed output simulated in the time-domain at 3.75 and 10.25 GHz with the 250-MHz input clock. It can be observed that the settling time of the oscillations is less than 1 ns, while the fall time is shorter and below 0.5 ns for both frequencies. Figs. 18–20 show the measured time-domain output at 3.75, 6.75, and 10.25 GHz, respectively, over the pulse duration of 2 ns. It is clear that the oscillations settle within 1 ns from the turn-on instant for all frequency bands. Only a few cycles are required for the oscillator to settle. The pulse duration may thus be reduced below 2 ns, allowing the pulse rate to reach more than 500 MHz before overlapping occurs. The phase difference between the $I+$ and $Q+$ outputs is about 92° at 3.75 GHz, 94° at 6.75 GHz, and 95° at 10.25 GHz. Considering that the digital oscilloscope is an equivalent time sampling oscilloscope and not a real-time oscilloscope, it samples the signal

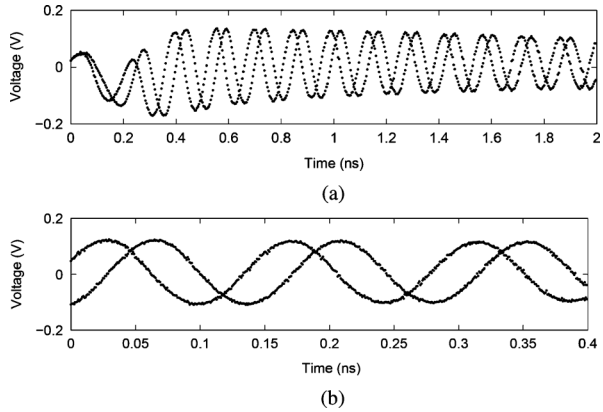


Fig. 19. Measured pulsed $I+$ and $Q+$ outputs in the time domain at 6.75 GHz: (a) from 0 to 2 ns and (b) three cycles starting from 0.96 ns.

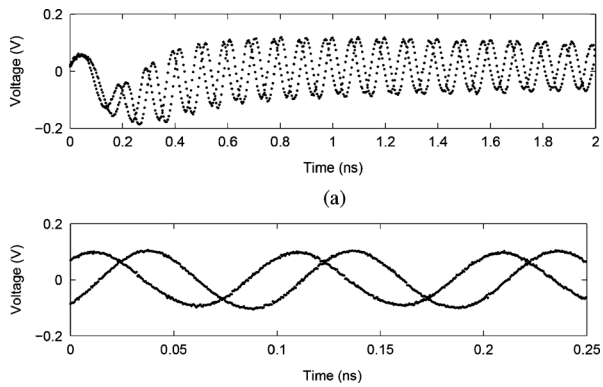


Fig. 20. Measured pulsed $I+$ and $Q+$ outputs in the time domain at 10.25 GHz: (a) from 0 to 2 ns and (b) three cycles starting from 0.96 ns.

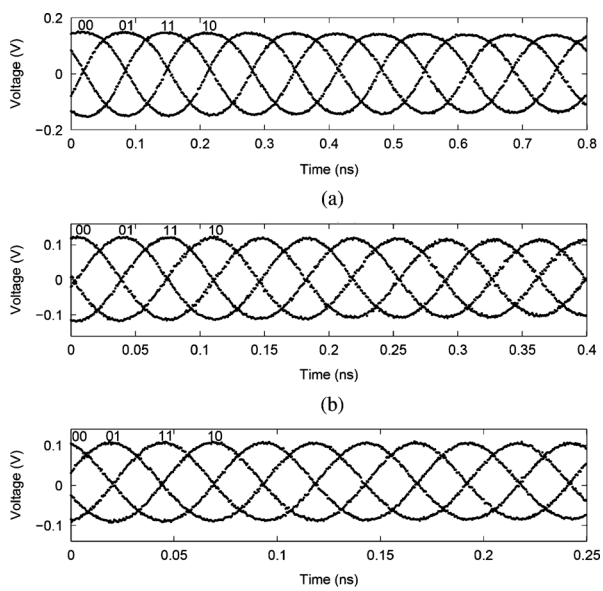


Fig. 21. Measured pulsed $I+$ output in the time domain for the four data patterns and phase states: (a) 3.75 GHz, (b) 6.75 GHz, and (c) 10.25 GHz. Three cycles are shown starting from 0.96 ns.

only once per trigger event. The oscilloscope is thus triggered using the input clock for these measurements [see Fig. 10(b)]. Since the 3.75-, 6.75-, and 10.25-GHz cycles are clearly visible, the generated pulsed oscillations are indeed coherent with the

TABLE II
SUMMARY OF PULSE MODULATOR'S PERFORMANCE IN COMPARISON WITH OTHER WORK

Ref.	CMOS Process	Freq. (GHz)	PRF (MHz)	Energy (pJ/p)	Amplitude (mV)	Duration (ns)	Modulation Format
[19]	0.18 μm	6–10[1]	750	12	30	0.5	BPSK
[20]	0.18 μm	6–10[1]	50	28	673	0.5	OOK
[21]	0.18 μm	3–5[2]	100	16.8	160	3.5	OOK
[22]	90 nm	3–5[2]	500	56	200	2.0	BPSK-PPM
[23]	90 nm	3–10[1]	1800	126	220	0.53	BPSK-PPM
[24]	90 nm	3–10[1]	400	65	60	1.0	BPSK
[25]	130 nm	6–10[1]	2000	51	380	0.5	BPSK
This Work	**0.13 μm**	**3–10[2]**	**250**	**13–18**	**300–200**	**2.0**	**BPSK & QPSK**

[1] Spectrum Bandwidth
[2] Carrier Frequency Range

input clock, and thus pulse-to-pulse coherency is maintained. Furthermore, Fig. 21 illustrates the quadrature signaling capability of the pulsed oscillator with the four time-domain measurements superimposed, one for each phase state. The plots show three oscillation cycles after a delay of 0.96 ns from the start of the pulse, at which time the oscillator has settled. Phases 0°, 90°, 180°, and 270° correspond to the input data patterns $(b_0 b_1)$ of 00, 10, 11, and 01, respectively. A good quadrature phase shift of approximately $90^\circ \pm 3^\circ$ is attained for all three oscillation frequencies.

An oscillator's center frequency will drift due to changes in process, supply voltage, and temperature (PVT). In this work, however, the ring oscillator's wide tuning range of 7 GHz and its large locking bandwidth in pulsed operation are sufficient to counteract the PVT variations. The oscillator's output amplitude and power level are small at startup while the current impulse is injected, yielding a large injected-to-output power ratio for a wide locking bandwidth [1], [15] that ensures phase-coherent pulsed operation. The PVT variations are further mitigated by the fact that the pulses occupy a frequency bandwidth of over 1 GHz, and thus, the integrated power lost into adjacent channels, over a 1-GHz bandwidth, is relatively small. Moreover, it may be possible to calibrate the oscillator's center frequency from time to time over a burst of several pulses using, for example, a frequency lock loop (FLL) [18], at the cost of additional chip area and power consumption. Considering that pulse amplitude and energy consumption are frequency-dependent quantities, these will be impacted by PVT variations in much the same way as the oscillation frequency is impacted.

When the ring oscillator is in CW mode the circuit consumes 23 mW at 3 GHz and 32 mW at 10 GHz. These numbers include the power consumption of the output buffers, which is about 13.5 mW altogether. When the system is pulsed with a 250-MHz clock signal, the average power consumption is about 13 mW at 3 GHz and 18 mW at 10 GHz. The energy consumption per pulse, E_p, is an important metric used to compare the performance of various pulse generators/modulators and it can be calculated using the expression

$$E_p = \frac{P_{\mathrm{AVG}} \times \mathrm{PRT}}{4} = \frac{P_{\mathrm{AVG}}}{\mathrm{PRF} \times 4} \tag{8}$$

where PRT is the pulse repetition time and PRF is the pulse repetition frequency. For the pulse modulator described in this paper, the energy consumption per pulse is less than 13.0 pJ at 3-GHz carrier frequency and 18 pJ at 10 GHz. The bias circuits were implemented using low-power devices to minimize the off-state leakage power to less than 60 nW (estimated).

Table II summarizes the proposed pulse modulator's performance in comparison with other works in the same frequency range. The proposed circuit achieves a low energy consumption of 13–18 pJ/pulse. When the energy consumption per pulse is normalized with respect to the output peak-to-peak voltage, this circuit outperforms other known pulse modulators.

V. CONCLUSION

A new 3–10-GHz short-pulse phase modulator based on harmonic injection locking has been developed in 0.13-μm CMOS for wideband applications. A quadrature ring oscillator employing resistive feedback is switched on and off using a new technique that allows the oscillations to settle within 1 ns. The generated oscillations are also phase locked to the input clock for high pulse-to-pulse coherence and a low integrated rms jitter of less than 3.6 ps is achieved. Furthermore, direct quadrature modulation was demonstrated over a wide frequency range from 3 to 10 GHz. Low power consumption of less than 13 mW at 3 GHz and 18 mW at 10 GHz was achieved with a 250-MHz clock frequency, corresponding to an energy consumption of less than 18 pJ per pulse. The IC occupies a die area of 0.85 mm^2 including bonding pads and decoupling capacitors, while the active circuit area is only 0.05 mm^2.

ACKNOWLEDGMENT

The authors would like to acknowledge the products and services provided by CMC Microsystems that facilitated this research, including computer-aided design (CAD) tools and chip fabrication services.

REFERENCES

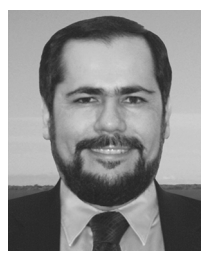
[1] R. Adler, "A study of locking phenomena in oscillators," *Proc. IRE*, vol. 34, no. 6, pp. 351–357, Jun. 1946.
[2] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS *LC*-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 392–393.
[3] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[4] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked *LC* dividers for quadrature generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1425–1433, Sep. 2004.
[5] R. A. York and T. Itoh, "Injection- and phase-locking techniques for beam control [antenna arrays]," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 11, pp. 1920–1929, Nov. 1998.
[6] S. Drew and V. F. Fusco, "Phase modulated active antenna," *Electron. Lett.*, vol. 29, no. 10, pp. 835–836, May 1993.
[7] J. Lasri, A. Bilenca, G. Eisenstein, and D. Ritter, "Optoelectronic mixing, modulation, and injection locking in millimeter-wave self-oscillating InP/InGaAs heterojunction bipolar photo transistors-single and dual transistor configurations," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 10, pp. 1934–1939, Oct. 2001.
[8] A. El-Gabaly and C. Saavedra, "A 3–10 GHz pJ/pulse dual BPSK/QPSK pulse modulator based on harmonic injection locking," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.
[9] A. W. Buchwald and K. W. Martin, "High-speed voltage-controlled oscillator with quadrature outputs," *Electron. Lett.*, vol. 27, no. 4, pp. 309–310, Feb. 1991.
[10] L. Dai and R. Harjani, "A low-phase-noise CMOS ring oscillator with differential control and quadrature outputs," in *IEEE Int. ASIC/SOC Conf.*, 2001, pp. 134–138.
[11] A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.
[12] C. Li and J. Lin, "A 1–9 GHz linear-wide-tuning-range quadrature ring oscillator in 130 nm CMOS for non-contact vital sign radar application," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 1, pp. 34–36, Jan. 2010.
[13] P. Kinget, R. Melville, D. Long, and V. Gopinathan, "An injection-locking scheme for precision quadrature generation," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 845–851, Jul. 2002.
[14] J.-C. Chien and L.-H. Lu, "Analysis and design of wideband injection-locked ring oscillators with multiple-input injection," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1906–1915, Sep. 2007.
[15] A. El-Gabaly and C. Saavedra, "A quadrature pulse generator for short-range UWB vehicular radar applications using a pulsed oscillator and a variable attenuator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2285–2295, Oct. 2011.
[16] T. Nakajima, S. Amakawa, N. Ishihara, and K. Masu, "A scalable wideband low-noise amplifier consisting of CMOS inverter circuits for multi-standard RF receivers," in *3rd Int. Signals, Circuits, Syst. Conf.*, Nov. 2009, pp. 1–4.
[17] A. Shirane, M. Otsuru, S.-Y. Lee, S. Yonezawa, S. Tanoi, H. Ito, N. Ishihara, and K. Masu, "A process-scalable RF transceiver for short range communication in 90 nm Si CMOS," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 455–458.
[18] J. Ryckaert, G. Van der Plas, V. De Heyn, C. Desset, B. Van Poucke, and J. Craninckx, "A 0.65-to-1.4 nJ/burst 3-to-10 GHz UWB all-digital TX in 90 nm CMOS for IEEE 802.15.4a," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2860–2869, Dec. 2007.
[19] V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 394–403, Feb. 2009.
[20] S. Sim, D.-W. Kim, and S. Hong, "A CMOS UWB pulse generator for 6–10 GHz applications," *IEEE Microw. Compon. Lett.*, vol. 19, no. 2, pp. 83–85, Feb. 2009.
[21] A. T. Phan, J. Lee, V. Krizhanovskii, Q. Le, S.-K. Han, and S.-G. Lee, "Energy-efficient low-complexity CMOS pulse generator for multiband UWB impulse radio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3552–3563, Dec. 2008.
[22] M. Cavallaro, G. Sapone, G. Giarrizzo, A. Italia, and G. Palmisano, "A 3-5-GHz UWB front-end for low-data rate WPANs in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 854–865, Apr. 2010.
[23] M. Demirkan and R. Spencer, "A pulse-based ultra-wideband transmitter in 90-nm CMOS for WPANs," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2820–2828, Dec. 2008.
[24] H. Hedayati and K. Entesari, "A 90-nm CMOS UWB impulse radio transmitter with 30-dB in-band notch at IEEE 802.11a system," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4220–4232, Dec. 2013.
[25] L. Zhou, Z. Chen, C.-C. Wang, F. Tzeng, V. Jain, and P. Heydari, "A 2-Gb/s 130-nm CMOS RF-correlation-based IR-UWB transceiver front-end," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 1117–1130, Apr. 2011.

Ahmed El-Gabaly (S'07-M'12) received the B.A.Sc. degree in computer engineering from the University of Waterloo, Waterloo, ON, Canada, in 2005, and the M.Sc. (Eng.) and Ph.D. degrees in electrical engineering from Queen's University, Kingston, ON, Canada, in 2007 and 2011, respectively. His Ph.D. research concerned novel microwave CMOS pulsed circuits [pulse generators and low-noise amplifiers (LNAs)] for ultra-wideband (UWB) automotive radar.

In 2011, he was a Postdoctoral Fellow with the Gigahertz Integrated Circuits Group, Queen's University, where he was involved with research on linear broadband GaN power amplifiers. He is currently an RF Integrated Circuit (RFIC) Design Engineer with Peraso Technologies Inc., Toronto, ON, Canada, where he designs 60-GHz transmitter RFICs in SiGe BiCMOS for high-speed wireless communications.

Dr. El-Gabaly was the recipient of a Natural Sciences and Engineering Research Council (NSERC) of Canada Doctoral Graduate Scholarship (2009–2011).



Carlos E. Saavedra (S'92–M'98–SM'05) received the B.Sc. degree from the University of Virginia, Charlottesville, VA, USA, and the M.Sc. and Ph.D. degrees from Cornell University, Ithaca, NY, USA, all in electrical engineering.

From 1998 to 2000, he was a Senior Engineer with the Millitech Corporation. In 2000, he joined Queen's University, Kingston, ON, Canada, where he is currently a Professor. From 2007 to 2010, he was the Graduate Chair with the Department of Electrical and Computer Engineering, Queen's University.

Dr. Saavedra is an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is a member of the Technical Program Review Committee (TPRC), IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS). He was section chair of the Natural Sciences and Engineering Research Council (NSERC) of Canada Discovery Grants Evaluation Group (2012–2014) and was chair of the IEEE MTT-S Technical Coordinating Committee 22 on Signal Generation and Frequency Conversion (2010–2013). He was a member of the Steering Committee and Technical Program Committee (TPC) of the 2012 IEEE MTT-S IMS and the IEEE RFIC Symposium TPC (2008–2011). He was a recipient of an NSERC Discovery Accelerator Award and was voted third-year ECE professor of the year at Queen's University in 2012 and in 2013.