Digitally assisted CMOS mixer with tight conversion-gain flatness

Shrijeet Mondal, Jiangtao Xu and Carlos E. Saavedra✉

A digital-assist technique is experimentally demonstrated that tightens the conversion-gain (CG) flatness of a CMOS mixer from a baseline level of ±1.5 dB over a 1–12 GHz span to ±1.0 dB over a 1–15 GHz span. The method uses a microcontroller to find the optimal bias point of the mixer that produces the desired CG flatness.

Introduction: Digital-assist (DA) techniques can improve a microwave circuit's performance using on- or off-chip digital hardware. In recent years, DA has been used in RF front-ends to minimise in-phase/quadrature (I/Q) imbalance, distortion and power consumption [1, 2]. At the component level, DA techniques abound for power amplifiers [3–5], low-noise amplifiers [6] and beamformers [7]. In this Letter, we report on a DA technique that uses an off-the-shelf microcontroller to improve the conversion-gain (CG) flatness and frequency bandwidth of a microwave active CMOS mixer. A look-up table with the mixer's baseline CG response as a function of frequency and control voltage is used to interpolate the gain-control voltages that will keep the CG within a user-defined flatness range.

Digitally assisted mixer concept: Suppose that a mixer's CG can be varied by applying a control signal, V_c, at a voltage node. In the proposed DA method, the baseline CG performance of the mixer is characterised over a discrete two-dimensional (2D) space of input frequency, f_{in}, and control voltage values, V_c. The data points are stored in a look-up table (matrix), $\boldsymbol{M}$, where each matrix element $M_{i,j}$ contains a CG value and the i and j indices represent discrete f_{in} and V_c values, respectively. Since the DA technique relies on interpolation, the data points can be taken over a coarse grid in the 2D space. When a user specifies a desired CG value, the microcontroller runs an interpolation algorithm on the data matrix to calculate the necessary V_c values that will keep the CG within a user-defined tolerance window for all input frequencies. The DA algorithm effectively compensates the CG's frequency roll-off by adjusting V_c, thereby extending the mixer's bandwidth from the baseline cut-off frequency of ω_c to the new cut-off frequency ω'_c.

Since the characterisation data contained in $\boldsymbol{M}$ is discretised in both f_{in} and V_c, the DA algorithm requires a bilinear interpolation routine: one for the frequency dimension and another for the voltage dimension. Using Fig. 1 as an aide to explain how to implement such an interpolation routine for the system under discussion, the key steps are:

- the desired CG, G_{in}, at a desired frequency, f_{in}, is read;
- the two closest gain values to G_{in} stored in $\boldsymbol{M}$ are retrieved and labelled G_1 and G_2;
- the two closest frequency values to f_{in} stored in $\boldsymbol{M}$ are retrieved and labelled f_1 and f_2;
- the control voltage values at the four data points (f_1, G_1), (f_1, G_2), (f_2, G_1) and (f_2, G_2) in Fig. 1 are retrieved and correspondingly labelled V_{11}, V_{12}, V_{21} and V_{22};
- the voltage V'_1 between V_{11} and V_{21} is found using the linear interpolation equation

$$V'_1 = \left(\frac{f_2 - f_{in}}{\Delta f}\right)V_{11} + \left(\frac{f_{in} - f_1}{\Delta f}\right)V_{21} \qquad (1)$$

- the voltage V'_2 is found using the equation

$$V'_2 = \left(\frac{f_2 - f_{in}}{\Delta f}\right)V_{12} + \left(\frac{f_{in} - f_1}{\Delta f}\right)V_{22} \qquad (2)$$

- the gain-control voltage that yields the desired G_{in} is found using the equation

$$V_c = \left(\frac{G_2 - G_{in}}{\Delta G}\right)V'_1 + \left(\frac{G_{in} - G_1}{\Delta G}\right)V'_2 \qquad (3)$$

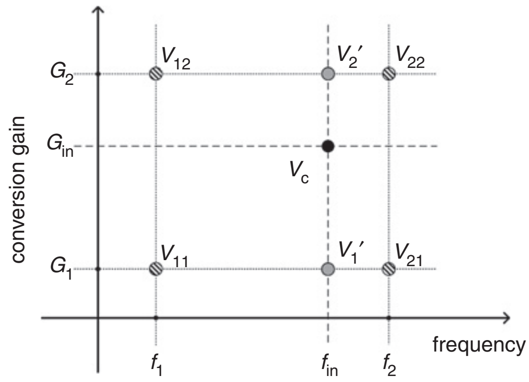

Fig. 1 *Linear interpolation of control voltage*

Fig. 2 contains a system-level representation of the proposed DA mixer, including a high-level flowchart of the algorithm executed by the microcontroller.

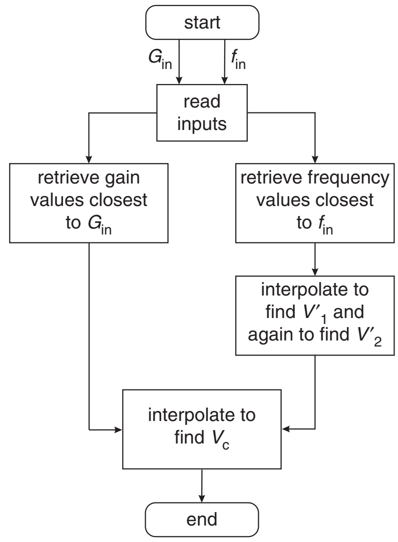

Fig. 2 *High-level block diagram of proposed DA algorithm*

Experimental verification: The mixer described in [8] is used as a test case to verify the efficacy of the proposed DA technique. That mixer, whose block diagram is depicted in Fig. 3, has a 3 dB bandwidth frequency of 12 GHz and its CG ranges from 1 to 17 dB as shown in Fig. 4. The chosen performance target for the mixer with DA was to produce CG curves with a 2 dB bandwidth of 15 GHz. Stated as a gain ripple specification, the goal was to improve the CG ripple from the baseline performance of ±1.5 dB from 1 to 12 GHz to a tighter ripple of ±1 dB from 1 to 15 GHz through DA.

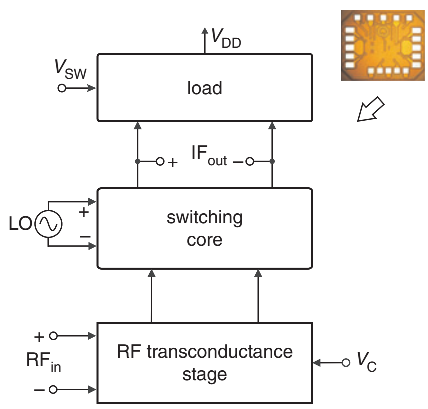

Fig. 3 *Block diagram and microphotograph of mixer used as test case to verify proposed DA technique. For detailed transistor-level schematics of test mixer see [8]*

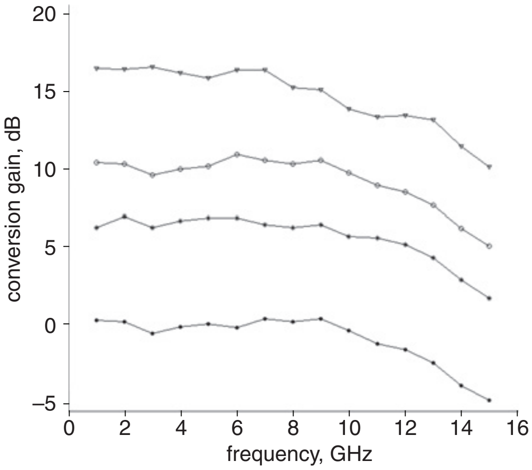

Fig. 4 *Measured baseline CG of test mixer without DA*

The first step was to characterise the test mixer's baseline CG performance as a function of frequency and control voltage(s). The input frequency was swept in 0.5 GHz increments from 1 to 15 GHz. The gain-control voltage was varied so as to yield 1 dB increments in the gain. This particular test mixer has two gain-control voltages: one for coarse and another for fine gain-control. The coarse gain-control voltage, V_{SW}, is a digital signal applied at the load network which toggles the CG between a low range of 0–10 dB and a high range of 7–17 dB. The fine gain-control voltage, V_c, is an analogue signal applied at the RF transconductance stage of the mixer (see Fig. 3) that continuously varies the CG *within* the low- and high-gain regions selected by V_{SW}. The overlap of about 3 dB between the low and high regions ensures that there are no gaps in the CG over control voltage and frequency.

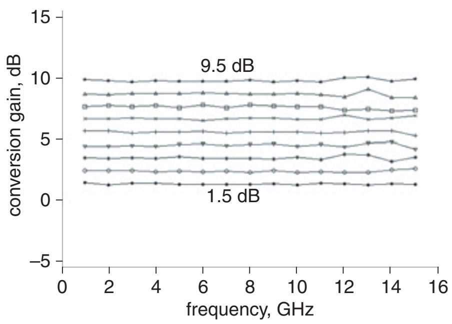

Fig. 5 *Measured CG of test mixer with DA*

A performance summary of the mixer with and without DA is presented in Table 1. The mixer's maximum gain, frequency operating range, input 1-dB compression point ($IP_{1\ dB}$), input third-order intercept point (IIP_3) and noise figures (NF) are presented both at 12 and 15 GHz.

Table 1: Test mixer performance summary

	Units	Baseline mixer	DA mixer
Bandwidth	GHz	1–12	1–15
CG range	dB	1–17	1–10
CG flatness	dB	±1.5	±1
IP_1 dB	dBm	−3.7[a]	−5.3[b]
IIP_3	dBm	+8.6[a]	+6.8[b]
NF	dB	11[a]	14.5[b]

[a]Measured at 12 GHz
[b]Measured at 15 GHz

After the baseline data was collected, it was stored in the ROM of a PIC18F87J11 from Microchip Technology microcontroller, the DA algorithm was run and the CG measured again. The experiment was successful: the CG of the mixer with DA at 1 dB intervals from 1 to 10 dB and each curve has a gain flatness of equal to, or better than, ±1 dB from 1 to 15 GHz is shown in Fig. 5. To accrue the benefit of wider bandwidth, the DA mixer's peak gain will be less than the baseline mixer. Yet, if the design target is not to extend the bandwidth of the mixer but to improve the gain flatness, then the DA mixer can accomplish that while maintaining the baseline mixer's original bandwidth.

Conclusion: A digitally assisted technique implemented on a variable-gain mixer was presented. The operating bandwidth of the mixer was extended from 12 to 15 GHz which shows that DA can enable an end-user to extract more performance from the mixer than it was originally designed for. The CG gain flatness was also improved from the standard ±1.5 –± 1 dB and it can be tightened even further if an application requires it. For prototyping/demonstration purposes, the CG characterisation is done once for each mixer chip. In a production environment, the statistical average of the characterisation data from a sampling of chips per wafer can be used.

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One or more of the Figures in this Letter are available in colour online.

Shrijeet Mondal and Carlos E. Saavedra (*Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada*)

✉ E-mail: saavedra@queensu.ca

Jiangtao Xu (*Department of Microelectronics, Xi'an Jiaotong University, Xi'an, Shaanxi, People's Republic of China*)

References

1 Lopelli, E., Spiridon, S., and van der Tang, J.: 'A 40 nm wideband direct-conversion transmitter with sub-sampling-based output power, LO feedthrough and I/Q imbalance calibration'. IEEE Solid-State Circuits Conf., San Francisco, California, February 2011, pp. 424–426

2 Liu, Y.-H., Huang, X., Vidojkovic, M., Ba, A., Harpe, P., Dolmans, G., and de Groot, H.: 'A 1.9 nJ/b 2.4 GHz multistandard Bluetooth Low Energy/Zigbee/IEEE802.15.6 transceiver for personal/body-area networks'. IEEE Int. Solid-State Circuits Conf., February 2013, pp. 446–447

3 Hsia, C., Zhu, A., Yan, J., Draxler, P., Kimball, D., Lanfranco, S., and Asbeck, P.: 'Digitally assisted dual-switch high-efficiency envelope amplifier for envelope-tracking base-station power amplifiers', *IEEE Trans. Microw. Theory Tech.*, 2011, **59**, (11), pp. 2943–2952

4 El-Gabaly, A., Stewart, D., and Saavedra, C.: '2 W broadband GaN power-amplifier RFIC using the fT doubling technique and digitally assisted distortion cancellation', *IEEE Trans. Microw. Theory Tech.*, 2013, **61**, (1), pp. 525–532

5 Watanabe, M., Snyder, R., and LaRocca, T.: 'Simultaneous linearity and efficiency enhancement of a digitally-assisted GaN power amplifier for 64-QAM'. IEEE RFIC Symp., Seattle, Washington, June 2013, pp. 427–430

6 Stewart, D., and Saavedra, C.: 'Extending the bandwidth of low-noise microwave amplifier through digital assist', *Electron. Lett.*, 2014, **50**, (7), pp. 528–530

7 Szortyka, V., Raczkowski, K., Vandebriel, R., Kuijk, M., and Wambacq, P.: 'Analog baseband beamformer for use in a phased-array 60 GHz transmitter'. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Santa Clara, California, January 2012, pp. 167–170

8 Xu, J., Saavedra, C.E., and Chen, G.: 'A 12 GHz-bandwidth CMOS mixer with variable conversion gain capability', *IEEE Microw. Wirel. Compon. Lett.*, 2011, **21**, (10), pp. 565–567