

Variable 360° Vector-Sum Phase Shifter With Coarse and Fine Vector Scaling

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Abstract—A CMOS vector-sum phase shifter covering the full 360° range is presented in this paper. Broadband operational transconductance amplifiers with variable transconductance provide coarse scaling of the quadrature vector amplitudes. Fine scaling of the amplitudes is accomplished using a passive resistive network. Expressions are derived to predict the maximum bit resolution of the phase shifter from the scaling factor of the coarse and fine vector-scaling stages. The phase shifter was designed and fabricated using the standard 130-nm CMOS process and was tested on-wafer over the frequency range of 4.9–5.9 GHz. The phase shifter delivers root mean square (rms) phase and amplitude errors of 1.25° and 0.7 dB, respectively, at the midband frequency of 5.4 GHz. The input and output return losses are both below 17 dB over the band, and the insertion loss is better than 4 dB over the band. The circuit uses an area of 0.303 mm² excluding bonding pads and draws 28 mW from a 1.2 V supply.

Index Terms—Active phase shifter, active summing junction, clock and data recovery, CMOS, IEEE 802.11n, LTE, monolithic microwave integrated circuit (MMIC), operational transconductance amplifiers (OTAs), phased array, quadrature generation, radar, RFIC, root mean square (rms) error, WiMAX.

I. INTRODUCTION

THERE is continued interest in finding new methods to improve the resolution and accuracy of monolithic microwave integrated circuit (MMIC) phase shifters. That interest is motivated by the critical role that phase shifters have in multiple-input multiple output radio links and phased arrays. Design advances over the past decade have led to significant improvements in the fractional bandwidth of the phase shifters and a reduction in the footprint area of the chips. MMIC phase shifters covering the full 360° using different techniques, such as delay lines [1], [2], signal reflection [3], high-pass/low-pass networks [4], all-pass networks [5], and vector summation [6]–[12].

In vector-sum phase shifters, there often appear unreachable phase angles (phase gaps) at the quadrant edges that limit the phase-step (bit) resolution of digital phase shifters. The objective of this paper is to explore the issue of phase gaps in vector-sum phase shifters and to propose a solution to mitigate them. The general approach taken here is to use a two-step vector-scaling procedure. First, a coarse scaling is carried

out in the current domain using operational transconductance amplifiers (OTAs), and subsequently, fine scaling is done on the signal vector in the voltage domain using a resistive network before the signal vectors are added together. A prototype phase shifter was designed for the 5.4-GHz band and was fabricated using the 130-nm CMOS technology. Experimental test results are presented, which validate the concept.

II. PHASE SHIFTER CONCEPT

Fig. 1 shows the block diagram of the proposed MMIC phase shifter, where the shaded area shows the on-chip circuitry. The phasor diagrams above the shaded area illustrate how a representative input signal is modified as it propagates through the phase shifter. The external 180° power splitter converts the RF input voltage signal, v_{RF} , into a differential waveform. A quadrature generator then produces four equal-amplitude orthogonal voltage signal vectors, $\pm v_I$ and $\pm v_Q$, for the I and Q paths, respectively. A pair of identical OTAs are used to scale the magnitude of the four voltage signal vectors and to convert them into current signals: $\pm i_{I,Q} = \pm G_m v_{I,Q}$, where G_m is the transconductance gain of the OTAs, which is tuned through the analog control voltages $V_{tune,I}$ and $V_{tune,Q}$.

Two single-pole double-throw (SPDT) switches are used to select which I -path vector (the 0° or the 180°) and which Q -path vector (the 90° or the 270°) will be summed together at the output to produce the desired output phase angle. The SPDT switches are controlled using two digital bits, a_2b_2 .

While the minimum gain, G_{min} , of the OTAs can ostensibly be reduced to zero, the problem with doing so is that the phase response of the OTAs at zero gain can be quite different than at moderate to high gain levels, thereby compromising the root mean square (rms) phase and amplitude error performance of the circuit. As a result, there is a practical limit to how small G_{min} should be and that value can be found by observing the phase response of the OTA as a function of its gain.

Suppose now that G_{min} has been established and that the highest gain setting of the OTAs is denoted by G_{max} , then the smallest output angle that the phase shifter would produce in quadrant I is

$$\theta_{min} = \tan^{-1} \left(\frac{G_{min,Q}}{G_{max,I}} \right) \text{ rad} \quad (1)$$

as shown in Fig. 2(a). It is straightforward to see that there will be a range of phase angles that the phase shifter cannot produce between quadrants I and IV and at every other quadrant boundary, as shown in Fig. 2(b). These unreachable output phase angle regions are the so-called phase gaps. The size of the gaps is $\theta_{gap} = 2\theta_{min}$ and they place a limit on the bit

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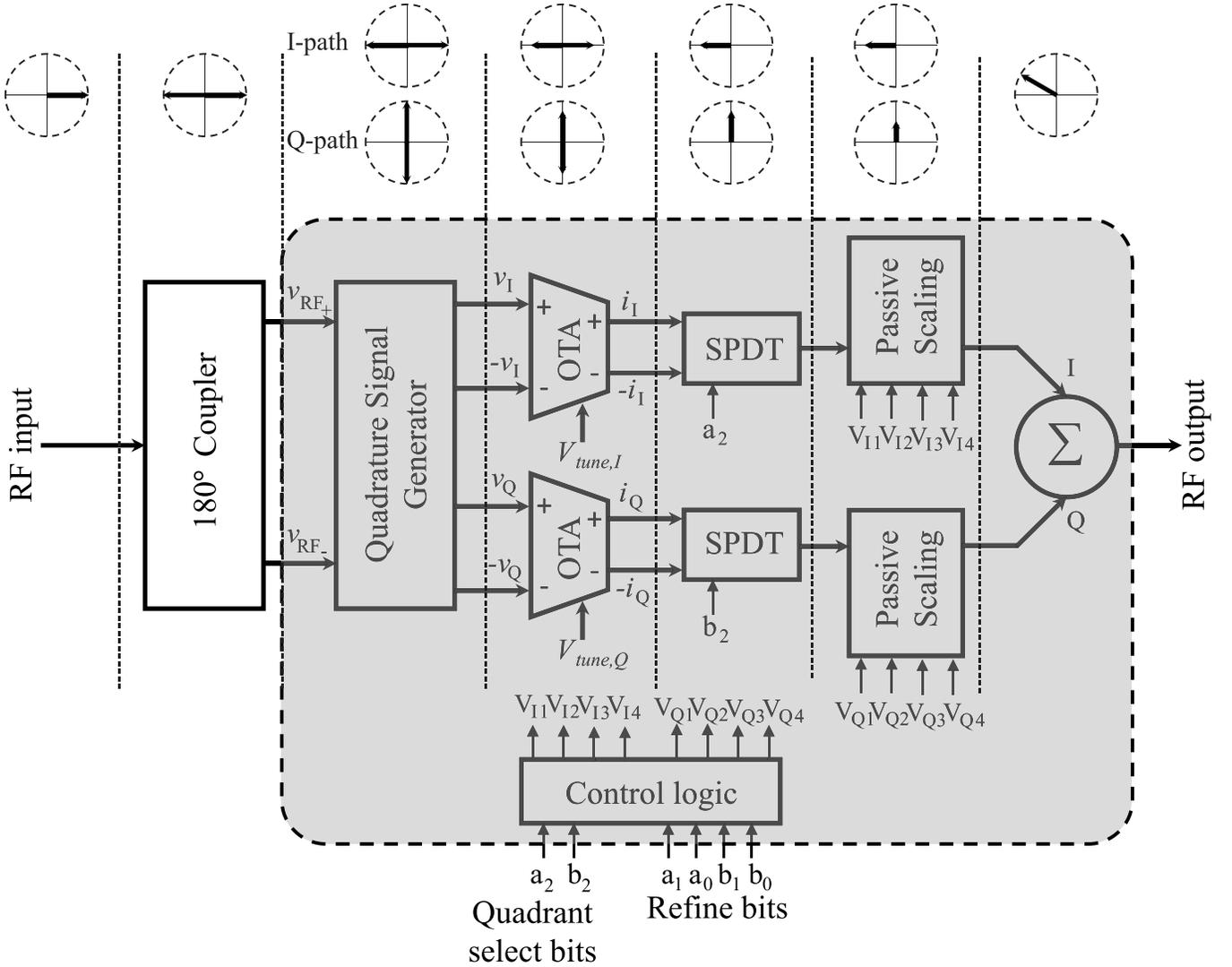


Fig. 1. Block diagram of the 360° vector-sum phase shifter proposed in this paper. Components outside the shaded area are off-chip.

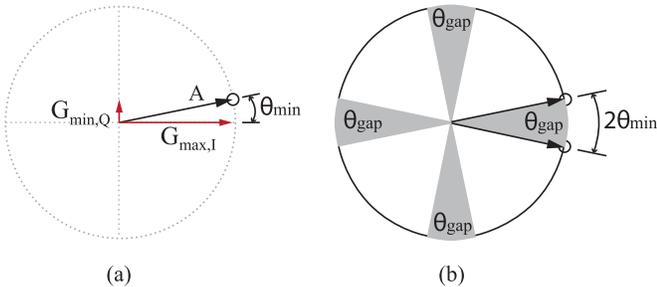


Fig. 2. (a) Minimum output phase angle, θ_{\min} , that can be produced in quadrant I. (b) Phase gaps equal to $2\theta_{\min}$ occur at the quadrant boundaries.

resolution of digital vector-sum phase shifters, since the circuit cannot have a phase step smaller than θ_{gap} . The relationship between the phase gap and the phase-step resolution of the phase shifter is $\theta_{\text{gap}} < 2\pi/2^n$, from which the maximum bit resolution is $\lfloor n \rfloor = \log_2(2\pi/\theta_{\text{gap}})$, where $\lfloor \cdot \rfloor$ denotes the

floor function. With the aid of (1), the expression for the maximum bit resolution, n , of the phase shifter as a function of the amplifier gain tuning range is

$$\lfloor n \rfloor = \log_2 \left[\frac{\pi}{\tan^{-1} \left(\frac{G_{\min,Q}}{G_{\max,I}} \right)} \right]. \quad (2)$$

To reduce the size of θ_{gap} and thereby increase the bit resolution of the phase shifter, the proposed system in Fig. 1 employs the second vector-scaling step after the SPDT switches. This second scaling step is done with a resistive passive network. The final I and Q vectors are added using a summing junction to produce the desired phase-shifted signal.

III. RFIC DESIGN

This section provides design details of the phase shifter's building blocks in sequence from left to right. All circuit components were designed for a center frequency of 5.4 GHz.

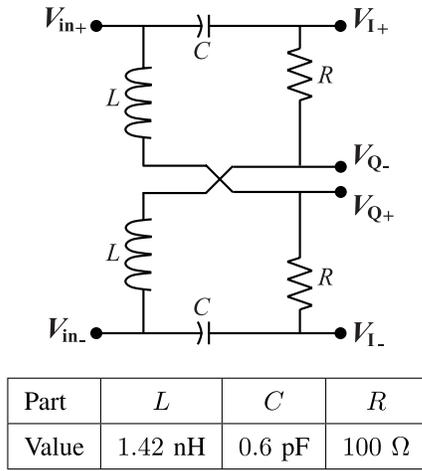


Fig. 3. Schematic of the all-pass quadrature signal generator.

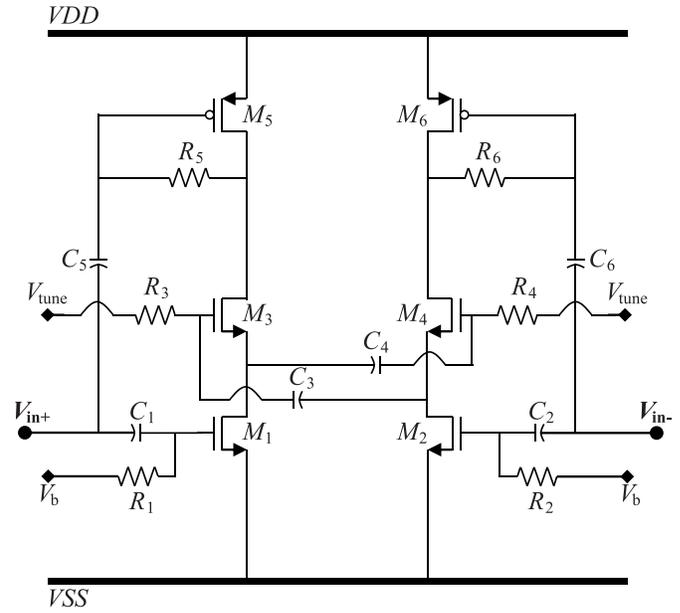
A. Quadrature Signal Generator

The circuit shown in Fig. 3 is used to generate differential quadrature basis vectors for the I and Q signal paths. It is an all-pass network that yields signals with tight amplitude and phase balance over wide bandwidths with a low return loss at the input port [6]. Using the component values shown in Fig. 3, the simulation results predict phase and amplitude imbalances less than 1° and 0.35 dB, respectively, and an input return loss below 16 dB for the quadrature generator over a 1-GHz band centered at 5.4 GHz.

B. OTA Vector-Scaling Stage (Coarse Scaling)

The OTAs convert the incident voltage signals into currents. These signal currents are then scaled by varying the transconductance, G_m , of the OTAs. The OTA schematic is shown in Fig. 4 and is a variant of the circuit reported in [7] and [13]–[15]. Thus, only a basic description of the OTA is given here followed by the information relevant to the phase shifter design. The input signal feeds to M_1/M_2 and M_5/M_6 through C_1/C_2 and C_5/C_6 , respectively. Transistors M_3 and M_4 are cross-coupled to provide feedforward regulation to the OTA for broadband operation and increased linearity. Tuning of the G_m is done by changing the gate voltage of M_3/M_4 at the node labeled V_{tune} in Fig. 4. Triple well nMOS devices are used here to provide source-body isolation for all OTA's devices and better isolation from substrate. Capacitors C_3 and C_4 are for dc blocking, and resistors R_1 – R_6 have a large value and are used for dc biasing.

A key design goal for the OTA for the application at hand is for its gain, G_m , versus V_{tune} relationship to have a linear response, so that the vector scaling also exhibits a linear dependence on the tuning voltage. A simulation of G_m versus control voltage, V_{tune} , at a frequency of 5.4 GHz is shown in Fig. 5. The magnitude of G_m varies linearly from 5.5 to 32 mS as V_{tune} is swept from 0.45 to 0.85 V. Therefore, $\theta_{\text{gap}} = 2 \tan^{-1}(5.5/32) = 0.34 \text{ rad} = 19.5^\circ$ and (2) predicts that the highest resolution that the phase shifter could produce is 4 b which corresponds to a phase step of 22.5° . To improve



Part	$(\frac{W}{L})_{1,2}$	$(\frac{W}{L})_{3,4}$	$(\frac{W}{L})_{5,6}$
Value	$\frac{90 \mu\text{m}}{0.12 \mu\text{m}}$	$\frac{39 \mu\text{m}}{0.12 \mu\text{m}}$	$\frac{90 \mu\text{m}}{0.12 \mu\text{m}}$
Part	R_{1-6}	$C_{1-2,5-6}$	$C_{3,4}$
Value	13.5 k Ω	2.4 pF	1.68 pF

Fig. 4. Schematic of the tunable feedforward-regulated OTA for coarse vector scaling.

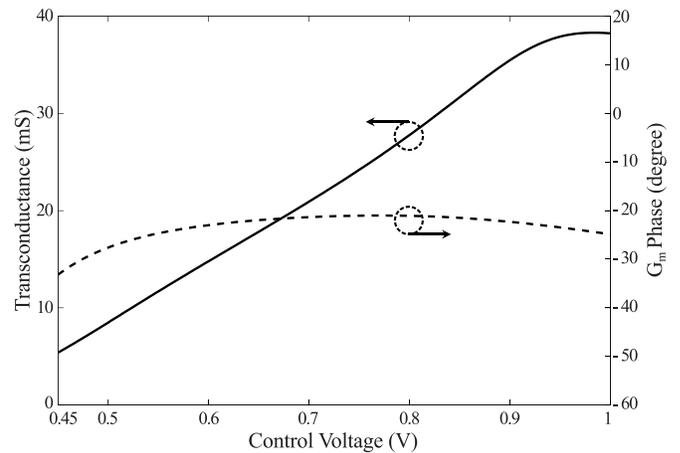


Fig. 5. Simulation results for amplitude and phase variations of the OTA versus control voltage.

the resolution of the phase shifter, the second scaling circuit is used to reduce the value of G_m . That circuit is described further below after the SPDT switches.

C. SPDT Switches

Two SPDT switches, connected to the OTAs' outputs, choose between the four quadrants. To keep the insertion loss of the switches below 1 dB, two series nMOS transistor, M_7 and M_8 , are used to provide a low channel resistance.

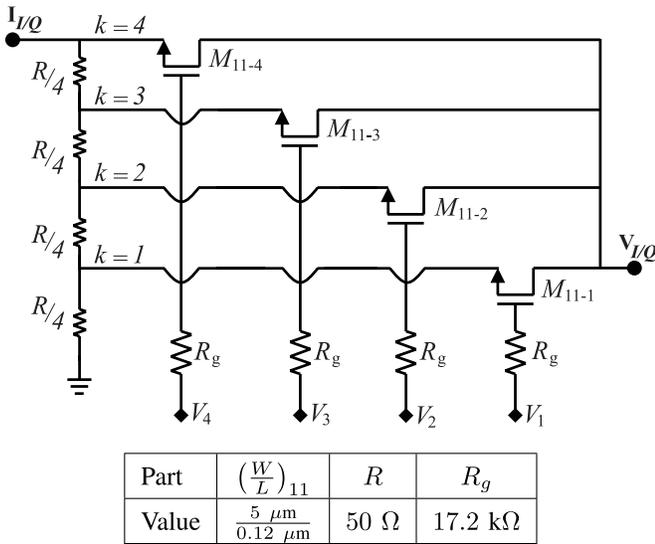


Fig. 8. Schematic of the four-resistor network used for fine vector scaling.

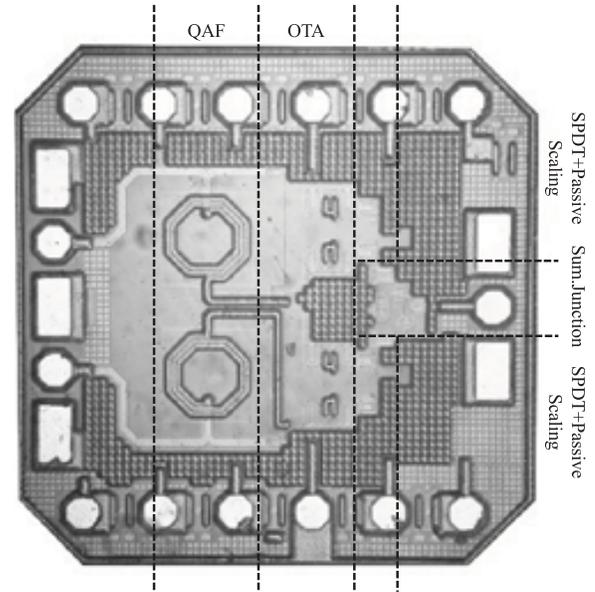


Fig. 10. Microphotograph of the fabricated active phase shifter.

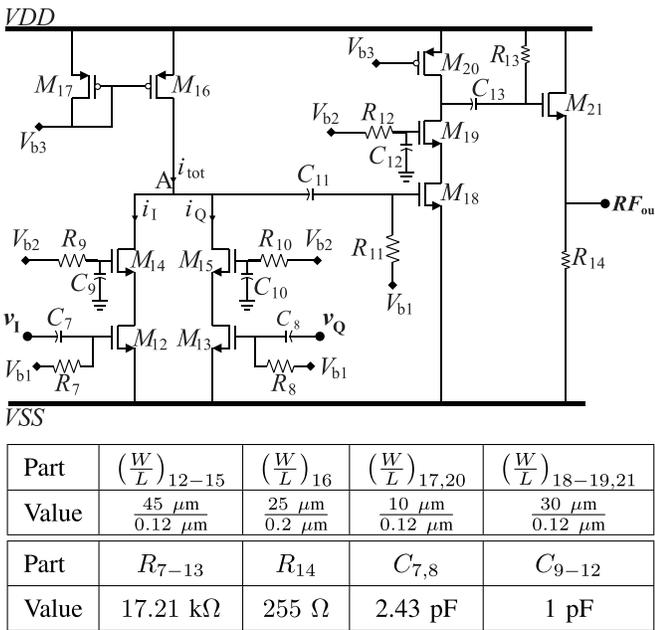


Fig. 9. Schematic of the vector-summation circuit.

transistors M_{14} and M_{15} are added at node A and are fed to a transimpedance amplifier. A source-follower (M_{21}) is used as a buffer to isolate the phase shifter from the 50- Ω impedance environment of the measurement system.

IV. EXPERIMENTAL RESULTS

The OTA-based active phase shifter is fabricated using the Global Foundries (formerly IBM) 0.13- μm CMOS process. A microphotograph of the fabricated chip is shown in Fig. 10. The chip core occupies an area of 0.303 mm^2 excluding bonding pads. The circuit draws a maximum of 28 mW of dc power from a 1.2 V supply.

An Agilent 8510C vector network analyzer was used for measuring the insertion phase and gain of the chip in different

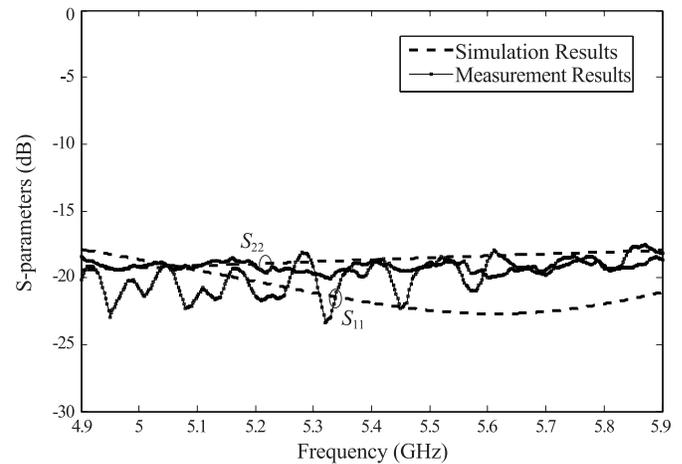


Fig. 11. Measurement and simulation results for input and output return losses.

phase settings. The chip’s differential input signals are fed by an external hybrid coupler, Krytar 4010180 with around 0.5 dB loss in 5-GHz band.

As noted earlier, the input and output matching circuitries of the phase shifter are independent of the phase shifter’s phase setting. Therefore, the input and output reflection coefficients, S_{11} and S_{22} , are provided for just one phase setting. Fig. 11 shows the input and output return losses. The measurement and simulation results agree for both S_{11} and S_{22} . The return losses are better than 15 dB in the frequency band of interest. Required tuning voltages for I and Q paths, $V_{\text{tune},I}$ and $V_{\text{tune},Q}$, are varied with 10-mV quantization steps, and their values and digital controls (refine bits) are provided in a lookup table.

Fig. 12 shows the unwrapped measured insertion phase response for 64 different phase states spaced 5.625° apart (6-b resolution). Both the measured and ideal relative insertion

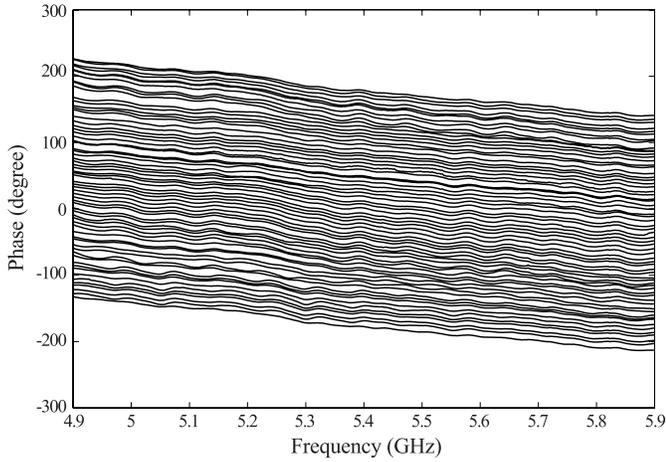


Fig. 12. Measured insertion phase for 64 output phases.

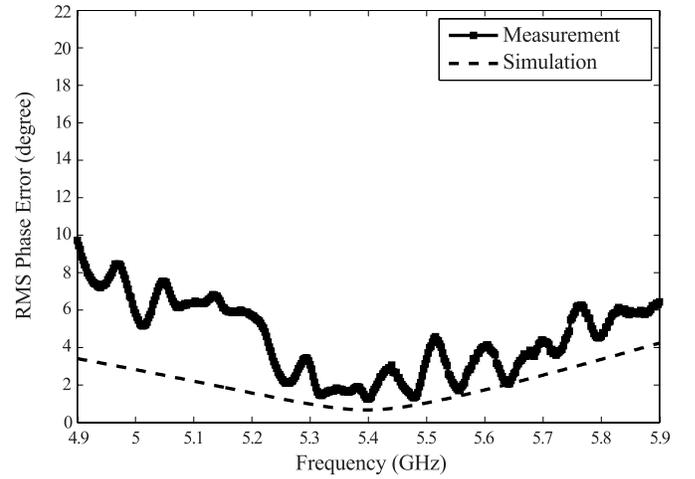


Fig. 14. RMS phase error.

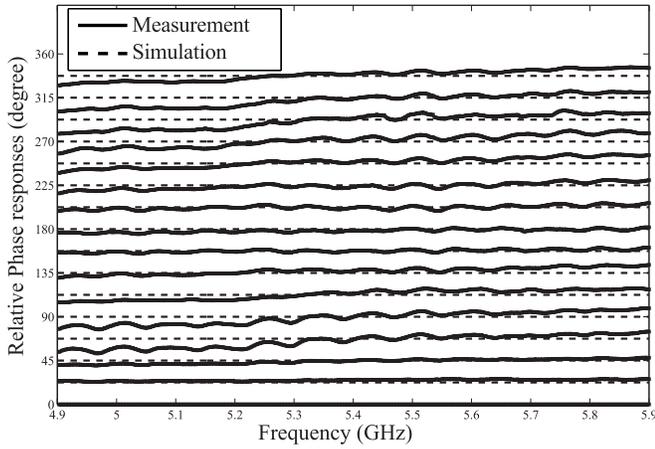


Fig. 13. Measured (solid lines) and ideal (dashed lines) relative insertion phase for 16 out of 64 possible states.

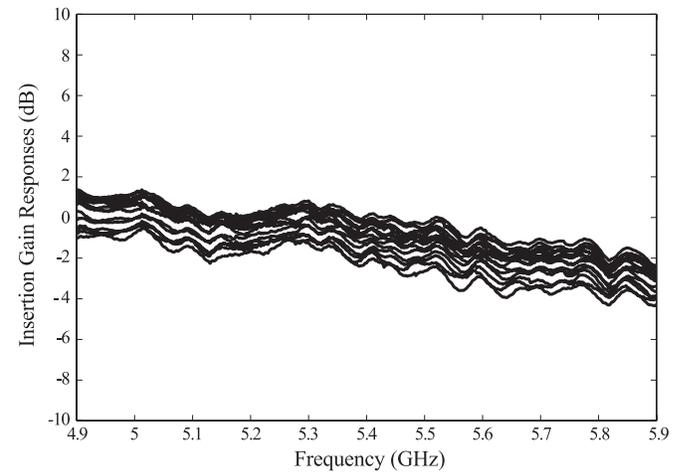


Fig. 15. Measured insertion gain for 16 states out of 64 phase settings (for more clear demonstration).

phases of the circuit are shown in Fig. 13. Only 16 out of the 64 possible curves are shown to avoid an overcrowded plot. As expected, the best agreement between the measured and ideal curves in Fig. 13 occurs at the design frequency of 5.4 GHz.

The rms phase error of a phase shifter can be calculated using (7), where N is equal to number of phase states (64 in this paper) and $\theta_{\Delta i}$ is the difference between the phase angle produced by the phase shifter and the expected theoretical value. The rms phase error of the proposed phase shifter is 1.25° at 5.4 GHz. The rms phase error as a function of frequency is shown in Fig. 14. The simulated and measured group delays are 0.11 and 0.14 ns, respectively,

$$\theta_{\Delta, \text{RMS}} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^N |\theta_{\Delta i}|^2} \quad (7)$$

$$A_{\Delta, \text{RMS}} = \sqrt{\frac{1}{N} \times \sum_{i=1}^N |A_{\Delta i}|^2} \quad (8)$$

Fig. 15 shows the insertion gain responses for some of the phase states (16 states are chosen for better illustration). The rms gain error, calculated using (8) for all 64 settings, is always

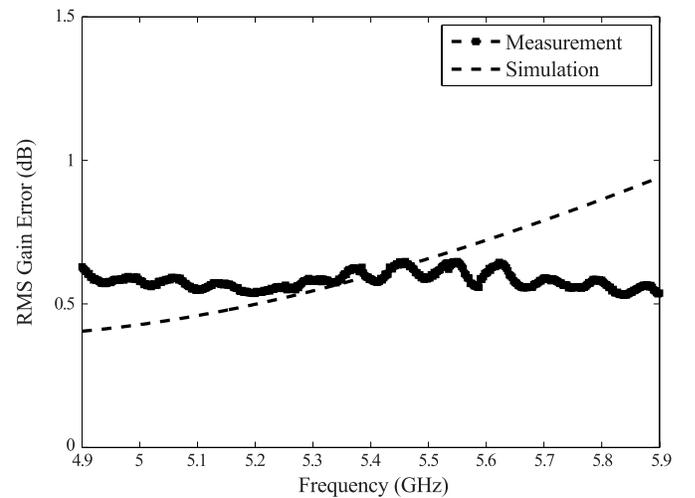


Fig. 16. RMS amplitude error.

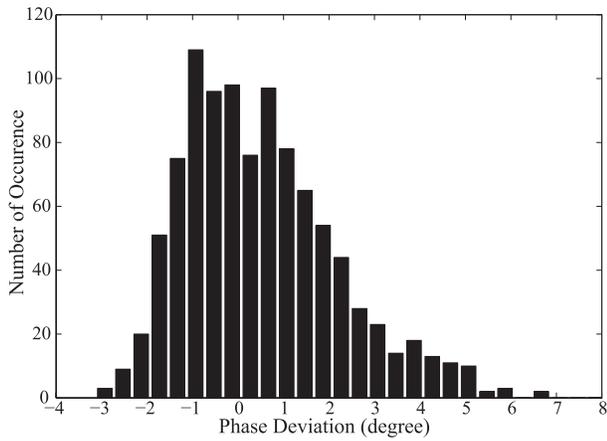
less than 0.7 dB, as shown in Fig. 16. The degradation of the measurement results from the simulations is <0.5 dB and experiences its maximum as it reaches the frequency band's edges. Here, $A_{\Delta i}$ is the deviation of the gain response in each

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

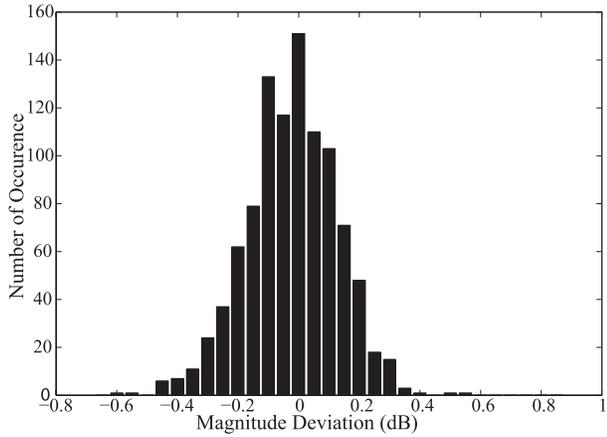
	units	This work	[6]	[7]	[8]	[9]	[10]
Frequency band	GHz	4.9–5.9	6–18	2–3	2.3–4.8	15–35	0.5–6
Phase range/resolution	degree / degree	360 / 5.625	360 / 22.5	360 / –	360 / 5.625	360 / 22.5	360 / –
RMS phase error	degree	1.25-9.7	2.7-10	1-5	1.04-1.4	4.2-13	≤ 7
RMS amplitude error	dB	0.5-0.7	0.5-1.7	0.75-1.2	0.2-1.1	1-2.2	≤ 0.95
Insertion gain	dB	$-0.1 \pm 1.15^*$	-1.15 ± 0.95	$1.5 \pm 1.5^*$	$-1 \pm 1^*$	-4.25 ± 9.25	9 ± 1
Input P_{1dB}	dBm	-12.9 ± 1	-5.4	-13.5	1.8 ± 1.2	-6.25	-19.5 ± 2.5
Supply voltage	V	1.2	1.5	2	1.8	1.8	1.5
DC power	mW	28	8.7	24	19	25.2	27.5
Chip area	mm ²	0.303**	0.45	0.38	0.652**	0.19**	1.21
$A_{\Delta,RMS} \times \theta_{\Delta,RMS}$	dB -°	0.625-6.8	1.35-17	0.75-6	0.21-1.54	4.2-28.6	6.65

* at the mid-band frequency

** core size



(a)



(b)

Fig. 17. Distribution of (a) phase and (b) magnitude deviation with mismatch in Monte Carlo simulation with 1000 runs.

phase state from the average insertion gain in decibel scales. The measured maximum peak to peak insertion gain error is -1.24 to 1.06 dB at 5.4 GHz, while its average value is -1 dB.

A Monte Carlo simulation was carried out to examine the effect of device mismatches on the amplitude and phase variations of the phase shifter. Fig. 17 shows the Monte Carlo results for a representative phase state of 0° . The standard deviation of the phase angle for eight phase states

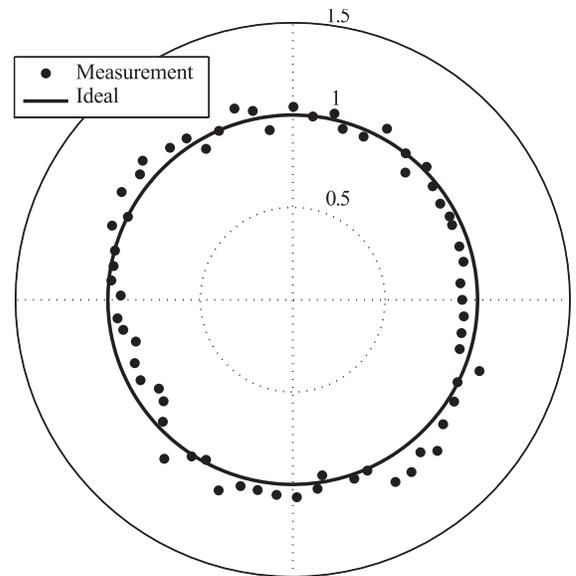


Fig. 18. Measured constellation diagram of the phase shifter.

around 360° is always less than 1.7° , which is well below the resolution of the phase shifter (5.625°). Meanwhile, the standard deviation of the amplitude variation is below 0.15 dB. The 72.5% of the occurrences (out of 1000 runs) were less than 0.25 of the least significant phase shift ($\pm 1.2^\circ$) away from the mean value of that state. The polar plot, shown in Fig. 18, shows the uniform distribution for all 64 constellation states of the phase shifter, normalized to the average insertion gain.

Fig. 19 shows the measured output power versus input power to study the linearity performance of the phase shifter at 5.4 GHz. The input-referred 1-dB compression point is -12.9 dB. The simulation results show that the 1-dB compression point variation, for all the phase states, is less than ± 1 dB. This is in accordance with the 2-dB insertion gain variation in different phase settings, reported by the measurements. The simulation result for the noise figure is also around 20 dB for all phase states.

A summary of the phase shifter's performance is outlined in Table I, in conjunction with a comparison with some of the previously reported designs in the similar CMOS technology.

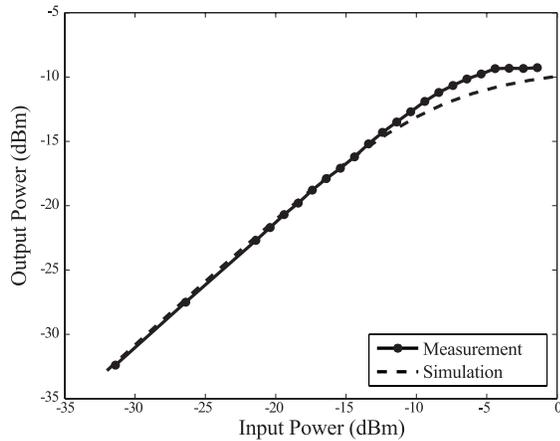


Fig. 19. Measured P1-dB compression point for the 0° phase setting.

Table I also includes the calculation of a basic metric

$$A_{\Delta, \text{RMS}} \times \theta_{\Delta, \text{RMS}} \quad (9)$$

for each circuit consisting of the product of the rms amplitude and phase errors. The metric is calculated at the center frequency and has the units of [dB][°].

V. CONCLUSION

A high-accuracy low rms error phase shifter based on the vector-sum method is demonstrated in this paper. The use of coarse and fine scaling of the signal vectors is critical to reducing phase gaps between quadrants and for reducing terms phase and amplitude errors. Experimental tests on a fabricated prototype showed that terms phase error reached down to 1.25°, and terms amplitude error was 0.7 dB at the center frequency of 5.4 GHz, thereby validating the approach.

ACKNOWLEDGMENT

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