A Wideband and High-Linearity *E*-Band Transmitter Integrated in a 55-nm SiGe Technology for Backhaul Point-to-Point 10-Gb/s Links

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***Abstract*— This paper presents the design of a wideband and high-linearity *E*-band transmitter integrated in a 55-nm SiGe BiCMOS technology. It consists of a double-balanced bipolar ring mixer which upconverts a 16–21-GHz IF signal to the 71–76- and 81–86-GHz bands by the use of a 55/65-GHz local oscillator signal, followed by a broadband power amplifier which employs 2-way output power combining using an integrated low-loss balun transformer. The transmitter exhibits an average conversion gain of 24 dB and 22 dB at the 71–76- and 81–86-GHz bands, respectively, with an output 1-dB compression point greater than 14 and 11.5 dBm at each band. A maximum output power of 16.8 dBm is measured at 71 GHz. The dc power consumption is 575 mW. The presented transmitter is used to demonstrate the transmission of a 10.12-Gb/s 64 quadrature amplitude modulated signal with a spectral efficiency of 5.06 bit/s/Hz, which makes it suitable for use in future high-capacity backhaul and fronthaul point-to-point links.**

***Index Terms*— BiCMOS, *E*-band, integrated circuits (ICs), millimeter waves, mixer, power amplifier (PA), SiGe, 64 quadrature amplitude modulation (QAM), wireless communications.**

I. Introduction

THE emergence of high-speed portable devices has greatly increased the demand for data bandwidth in wireless networks. The telecommunications industry responded by introducing 4G/LTE wireless networks nearly half a decade ago. To meet the much higher data traffic flow expected after 2020, standards for a fifth-generation (5G) wireless communications network are being developed [1]. Additionally, it is essential to develop ultrahigh speed mm-wave backhaul links at *E*-band (71–76 and 81–86 GHz) not only for 5G networks that are at least half a decade away but also for 4G/LTE networks to meet data traffic demands in the immediate future. A concept that has gained much attention in millimeter-wave link design is to move the away from the remote radio heads, as shown in Fig. 1. This allows for a more efficient and dynamic arrangement of the cells, but it implies that the link between the radio head and the baseband processing unit (also known as fronthaul) must carry common public radio interface data, with capacities in the order of 10 Gb/s and very low latency requirements (<1 ms) [2], [3].

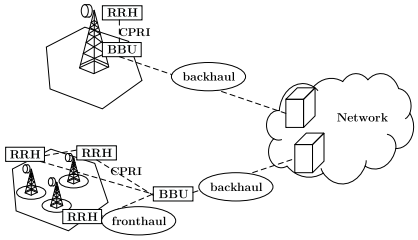

Fig. 1. Fronthaul and backhaul network architecture.

There are still important challenges when designing *E*-band integrated transmitter front-ends that need to be addressed. In order to provide full-duplex operation, for example, a wideband design which covers the complete *E*-band is desired, which enables flexible link frequency planning and frequency-division duplex (FDD) operation. Additionally, to provide the required multi-Gb/s throughput with an efficient channelization that fulfills the ECC and ETSI recommendations [4], [5], high order modulations like 32 or 64 quadrature amplitude modulation (QAM) should be used. In turn, this requires the transmitter to operate at a certain power back-off (typically 7–10 dB), which sets a high linearity requirement throughout the whole bandwidth.

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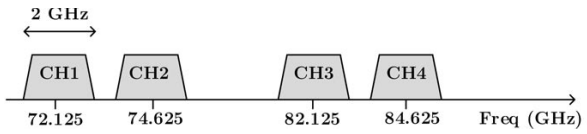


Fig. 2. Considered *E*-band channel distribution.

The interest in multi-Gb/s wireless data links by industry has motivated the design of *E*-band integrated circuits (ICs) using cost-effective CMOS and SiGe BiCMOS technologies from individual circuit blocks to transceiver chip sets [6]–[12]. A packaged SiGe-based transceiver is described in [11] that yields bitrates of up to 20 Gb/s using 32-QAM modulation. It uses different chipsets to cover the 71–76- and 81–86-GHz bands. The transmitter in [10] covers the full *E*-band, yields a bitrate of 3 Gb/s using 64-QAM modulation and it has a saturation output power of 12 dBm. The transceiver in [13] delivers 6 Gb/s with 8-PSK modulation in the 81–86-GHz band using a GaAs mm-wave front-end. The commercial solution reported in [14] transmits up to 3 Gb/s using different chipsets for the 71–76- and 81–86-GHz bands plus an external GaAs power amplifier (PA). Other commercial products based on monolithic microwave ICs and SiGe chipsets are available from companies like Gotmic (Part No. gTSC0023) or Sivers IMA (Part No. FC2121E).

This paper considers a super-heterodyne transmitter with an IF of 17.125/19.625 GHz, a channel bandwidth of 2 GHz and capable of covering the complete *E*-band. It presents the design and measurement results of the mm-wave part of the transmitter circuit: upconverter mixer and PA. This paper is organized as follows. Section II gives the main considerations for the system design. Section III describes the transmitter architecture at block level. Section IV presents the design of the *E*-band upconverter mixer. Section V deals with the design of the PA and Section VI presents the measurement results. Finally, Section VII concludes this paper.

II. System Design Considerations

A. Link Requirements and Frequency Plan

The considered transceiver must operate in full-duplex communication mode and provide a data rate of at least 10 Gb/s in each direction in order to meet the requirements of future backhaul and fronthaul links. The chosen duplexing mode is cross-band FDD, using one of the lower (71–76 GHz) and upper (81–86 GHz) bands to transmit in each direction. This way, the TX and RX channels are spaced by at least 10 GHz, which simplifies the design of the diplexer and fulfills the ECC recommendation [4]. Additionally, to avoid crosstalk and interference between closely deployed links, apart from traditional solutions such as different antenna polarization and so on, the bandwidth is divided into four 2-GHz channels as shown in Fig. 2.

B. Modulation Scheme

In order to transmit at the required 10-Gb/s rate over a 2-GHz channel, a spectral efficiency of at least 5 b/s/Hz is required. In an mm-wave point-to-point link with no significant multipath propagation, a single carrier QAM with a low complexity equalizer provides a good tradeoff between transceiver complexity and performance. Therefore a 64-QAM modulation scheme has been selected for this paper, which allows for the extra overhead introduced by frame headers, coding and root-raised-cosine filter roll-off factor.

The chosen channel bandwidth with such a high spectral efficiency goes beyond the current state-of-the-art considered by the ETSI and therefore the specifications like the spectral mask are not standardized yet [5].

TABLE I

Parameters Considered for the Link Budget Analysis

Parameter	Value
Frequency (f)	86 GHz
Channel bandwidth (B)	2 GHz
Receiver temperature (T)	290 K
Receiver noise figure (NF_{RX})	7.5 dB
Antenna gain ($G_{ANTENNA}$)	52 dBi
Diplexer insertion loss ($L_{DIPLEXER}$)	1 dB
Die to waveguide interconnection loss ($L_{INTERCONN}$)	2 dB
Other loss (L_{OTHER})	4 dB
Coding gain @ BER=10^{-6}	4 dB

TABLE II

Required P_{TX} Versus Rain Rate, to Receive the 64-QAM Signal at 1-km Distance With BER = 10^{-6}

Rain rate (mm/h)	0	20	25	30	35	40	45
Minimum P_{TX} (dBm)	-13.4	-3.3	-1.6	0	1.5	3	4.4

C. Link Budget

A link budget analysis must be performed to assess the required output power, assuming the link parameters summarized in Table I. The noise power and received signal power at the receiver input are given by (1) and (2), respectively, where k is the Boltzmann constant, L_{FS} is the free-space loss given by the Friis formula (3), L_{ATM} is the loss due to atmospheric absorption (0.4 dB/km at the *E*-band) and L_{RAIN} depends on the rain rate (R) in mm/h and can be calculated using (3) for horizontal polarization (worst case) and 86 GHz [15].

An objective SNR of 26.5 dB is required to obtain a bit error rate of 10^{-6} with 64-QAM modulation [16], which sets the required power at the output of the transmitter (P_{TX}). Table II shows the required P_{TX} to achieve the objective SNR at a distance of 1 km for different rain rates.

$$P_{\mathrm{NOISE}} = 10\log(\mathrm{kTB}) + \mathrm{NF_{RX}} = -73.47 \quad \mathrm{dBm} \tag{1}$$

$$\begin{aligned} P_{\mathrm{SIGNAL}} = {} & P_{\mathrm{TX}} - 2L_{\mathrm{INTERCONN}} - 2L_{\mathrm{DIPLEXER}} \\ & + 2G_{\mathrm{ANTENNA}} - L_{\mathrm{FS}} - L_{\mathrm{ATM}} \\ & - L_{\mathrm{RAIN}} - L_{\mathrm{OTHER}} \end{aligned} \tag{2}$$

$$\begin{aligned} L_{\mathrm{FS}} = {} & 92.44 + 20\log(d[\mathrm{km}]) \\ & + 20\log(f[\mathrm{GHz}]) \end{aligned} \tag{3}$$

$$L_{\mathrm{RAIN}}[\mathrm{dB/km}] = 1.2398R[\mathrm{mm}/h]^{0.7006}. \tag{4}$$

Furthermore, it is necessary to operate the transmitter at a certain back-off below its maximum output power, so as

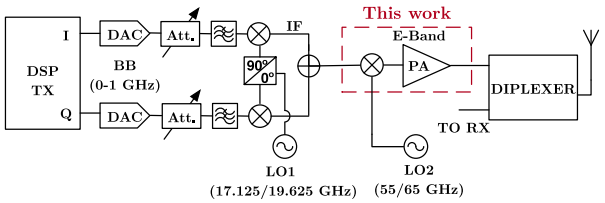


Fig. 3. Architecture of the E-band transmitter.

not to distort the signal significantly as well as to reduce the spectral regrowth and fulfill the spectral mask for this kind of link. For 64-QAM, with a roll-off factor of 15%, this back-off requirement is in the order of 9–10 dB below the output 1-dB compression point (OP_{1dB}) [17], which sets a high linearity requirement on the PA. Thus, a transmitter with an OP_{1dB} higher than 14 dBm is required for the considered link. With such a transmitter, according to Table II, it would be possible to transmit 10 Gb/s at 1-km distance for rain rates below 45 mm/h. This rain rate is not exceeded more than 0.01% of the time in a big part of Europe and North America [18].

III. Transmitter Architecture

The proposed transmitter has the super-heterodyne architecture shown in Fig. 3. The digital baseband (BB) signal is generated by a field programmable gate array (FPGA) which is connected to two digital-to-analog converters (DAC) that generate the analog in-phase (I) and quadrature (Q) BB signals. The DACs have 14-b resolution and a typical sampling speed of 2.5 Gs/s, which is enough to sample the 0–1-GHz signals and relaxes the stopband requirements of the low-pass filters (they need $f_{pass} = 1$ GHz and $f_{stop} = 1.25$ GHz). The output connection of the DACs is typically dc-decoupled from the rest of the blocks. This, together with other analog effects like $1/f$ noise can degrade a portion of the signal located near 0 Hz, which significantly affects the quality of multigigabit signals with high order modulations as described in [19]. To mitigate this effect, a waveform structure with two digital subbands is chosen, centered at -500 and 500 MHz and each with a bandwidth of 1 GHz.

Two variable attenuators are placed to adjust the signal level depending on the DAC output power and to compensate for nonfrequency-selective I/Q amplitude imbalance if necessary. An active I/Q upconverter converts the signal to an IF of 17.125 or 19.625 GHz. This value is selected because it balances the tradeoff between frequency (low enough so as not to complicate the design of the IF blocks) and bandwidth (the required relative bandwidth is below 25%). A second mixer converts the IF signal to the 71–76- or 81–86-GHz bands using a 55/65-GHz local oscillator (LO). This way it is possible to transmit the signal in any of the 4 channels described in Section II. Additionally, with this architecture the mm-wave LO frequency falls far away from the band of interest, which makes the LO feedthrough in the upconverter a less critical issue. It does not affect the saturation of the PA because the gain is much lower at those frequencies, and the remaining spurs are easily filtered out by the diplexer. The PA covers the whole 71–86-GHz band and it must provide enough gain

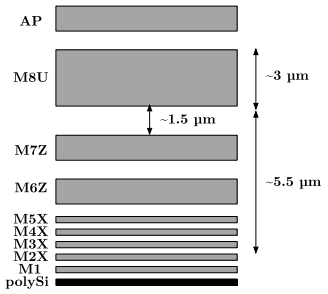


Fig. 4. Simplified metal stack of the BiCMOS 55-nm process.

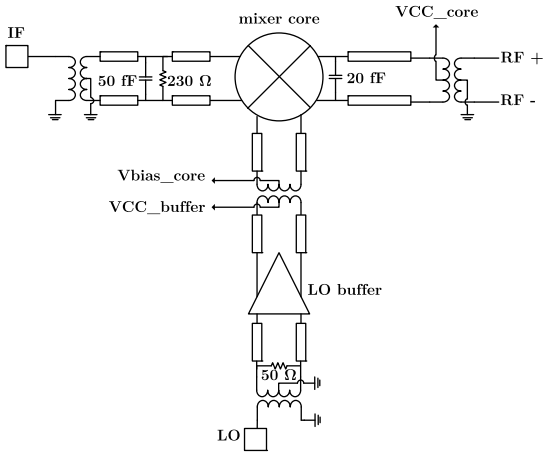


Fig. 5. Block diagram of the E-band mixer.

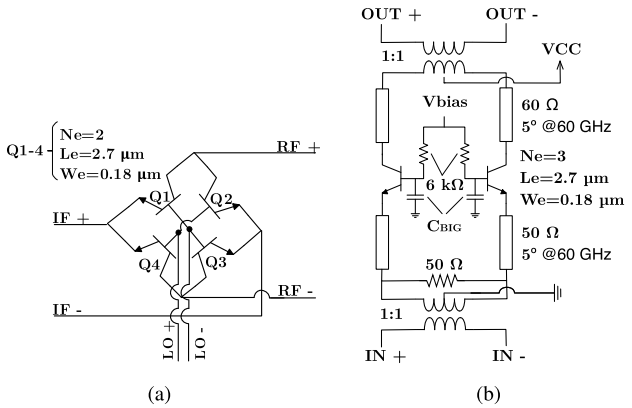
so that the linearity of the transmitter is not limited by the preceding stages.

The following sections will deal with the mm-wave blocks of the transmitter: the mixer and the PA. They are integrated together, as a single IC, in a 55-nm BiCMOS technology provided by STMicroelectronics [20]. The process provides eight copper layers as well as a top aluminum cap, with the simplified stack shown in Fig. 4. The eighth metal layer is ultrathick (~ 3 μm), sixth and seventh are thick, and first to fifth are thin.

IV. Upconverter Mixer Design

The mixer upconverts the IF band of 16–21 GHz to 71–76 GHz and 81–86 GHz using LO signals of 55 and 65 GHz, respectively. With the PA having a gain of 25–28 dB, there is sufficient system gain to allow for the use of a semi-passive mixer with a conversion loss of approximately 5 dB, without the need for a gain stage. Using the specifications derived in Section II, the target OP_{1dB} of the upconverter is at least -5 dBm, which includes a margin of a few dB.

The upconverter block has the architecture shown in Fig. 5 and consists of a double-balanced mixing core, a buffer for the LO signal and the required matching networks and interconnections. The double-balanced topology is selected because of its superior linearity performance and port-to-port isolation. The IF and LO signals are converted from single-ended to differential using integrated transformer baluns. A second set of center-tapped transformers is used to provide dc bias to the



(a) (b)

Fig. 6. (a) Schematic of the bipolar ring mixer core. (b) Schematic of the CB LO buffer.

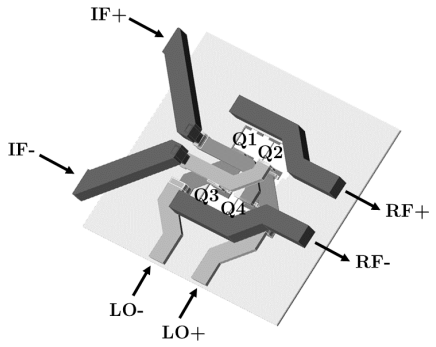


Fig. 7. 3-D view of the mixer core connections.

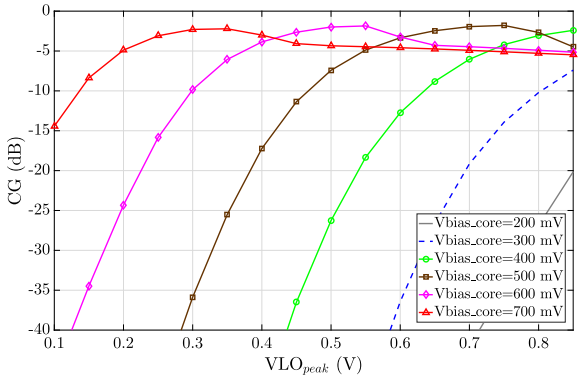


Fig. 8. CG versus LO voltage at different base bias voltages.

mixer core and to dc decouple it from the LO buffer and the output.

A 50-fF capacitor and a 230-Ω resistor are placed in shunt with the IF transformer's secondary winding to resonate out its inductance and simultaneously provide a broadband match to 50 Ω over the 16–21-GHz range. At the RF output port of the mixer, a 20 fF capacitor is used to resonate out the inductance of the RF transformer's primary winding at 78.5 GHz (center of the *E*-band) and to provide the required 71–86-GHz output bandwidth when the secondary is loaded with 50 Ω (a 50-Ω interface is chosen between the mixer and the PA). The transmission lines are implemented as side-shielded microstrip lines and the capacitors have a metal-oxide-metal (MOM) structure. The transformers, capacitors and interconnects are simulated using the Momentum electromagnetic (EM) solver.

The schematic of the double-balanced mixing core is shown in Fig. 6(a). This topology is chosen for its low power consumption, good linearity and compact layout, at the expense of higher loss than the standard Gilbert Cell [21]. Basic ring mixers, whether diode- or transistor-based, typically exhibit a conversion loss in the range of 9–12 dB and they require large LO signal power levels. In this paper, HBTs are used in the ring because they offer a better input impedance match at the LO port. The used HBTs have two emitter fingers of dimension $W_e = 0.18$ μm and $L_e = 2.7$ μm. The transistor cells have been RCc extracted for the simulations. In order to optimize the transistor arrangement and their connections, the transistor cells are removed from the layout, ports are added at the connection points and the resulting structure is EM simulated, following a procedure similar to the one outlined in [7]. Fig. 7 shows the 3-D view of the mixer core layout. As observed, the connections are made symmetrical with the objective of minimizing the imbalance between the differential branches and thus reduce the LO feedthrough.

To meet the conversion loss target of 5 dB for the mixer core and to simultaneously keep the LO power requirements at moderately low levels, a dc bias voltage, Vbias_core, is applied to the base terminals (the LO port) of the transistors. The dc voltage is in the vicinity of the transistors' base-emitter turn-on voltage, so as to place the devices in the most nonlinear region of their I–V curve, thus leading to stronger mixing tones and lower conversion loss—a technique that has been applied before to MOSFET ring mixers [22].

Fig. 8 shows the simulation of the conversion gain (CG) of the HBT ring mixer as a function of the LO signal amplitude for different values of Vbias_core. Consider, hypothetically, that the available LO signal amplitude was only 0.2 V which corresponds to −4 dBm in a 50-Ω environment. For this case, the conversion loss of the mixer without any dc bias applied to the base terminals would fall well below the −40-dB cutoff of the vertical axis in Fig. 8. Yet, the graph shows that if Vbias_core is set to 700-mV dc, then the mixer's conversion loss can be reduced to −5 dB.

The LO path includes a single-stage common-base (CB) buffer amplifier like the one shown in Fig. 6(b) to boost the LO signal prior to entering the passive mixing core and which is based on [23]. The base terminals are biased from an 850-mV supply through 6-kΩ resistors and large MOM capacitors are used as RF shorts to ground at the bases. The CB stage draws a current of 8 mA from a collector supply voltage of 1.2 V and exhibits a simulated voltage gain of 12 dB at 55 GHz and 14 dB at 65 GHz, with a maximum output voltage swing of 900 mVp.

The simulation results of the mm-wave mixer block when loaded with 50 Ω are shown in Fig. 9, with all the extracted and EM simulated parasitics taken into account. The CG is between −5 and −3 dB for both the lower and upper subbands and the OP_{1dB} is better than −3 dBm. The simulated LO-output isolation is 20 dB.

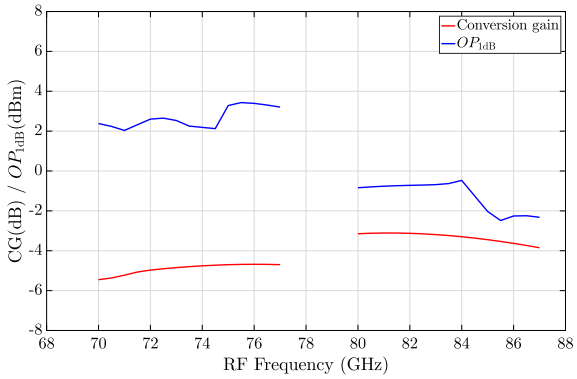


Fig. 9. Postlayout simulated CG and $OP_{1\ dB}$ of the mixer when loaded with 50 Ω.

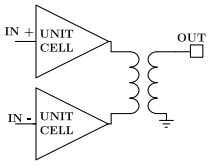


Fig. 10. Block diagram of the power combined PA cells.

V. Power Amplifier Design

A. General Description of the PA Architecture

In order to meet the system requirements given in Sections II and III, the PA must provide a gain bigger than 25 dB and an OP_{1dB} bigger than 14 dBm, maintaining its performance along the complete *E*-band (71–86 GHz).

The low breakdown voltages of high speed SiGe HBTs, with typical BV_{CE0} values of 1.5–1.8 V, limit the maximum voltage swing and thus the achievable output power at mm-wave frequencies. The most accepted strategy is to combine the output power of various PA cells [8], [24], [25], where the optimum number of cells to be combined depends on a tradeoff between output power, combining efficiency and routing complexity. The PA presented in this paper consists of two identical single-ended unit cells which are combined at the output as shown in Fig 10. This way around 2 dB higher power than with a single cell can be obtained (assuming a combiner insertion loss (IL) of around 1 dB) and at the same time a balanced input is presented to the mixer. Additionally, with this structure it is easy to make a symmetrical layout and also keep the transistors of both cells in close proximity to increase the matching and minimize the imbalance.

To achieve the required gain, each cell is implemented using a driver in cascode configuration followed by five common-emitter (CE) stages, with the schematic shown in Fig. 11. The transistor sizes are up-scaled toward the output to increase the power handling capabilities of the last stages and maintain a low power consumption at the input stages. The dc bias of the driver stage provides a tuning knob for self-healing purposes, as the gain can be varied to compensate for temperature, process and aging variations, as well as to implement automatic gain control systems. Fig. 12 shows the measured gain variation versus driver bias voltage for a standalone

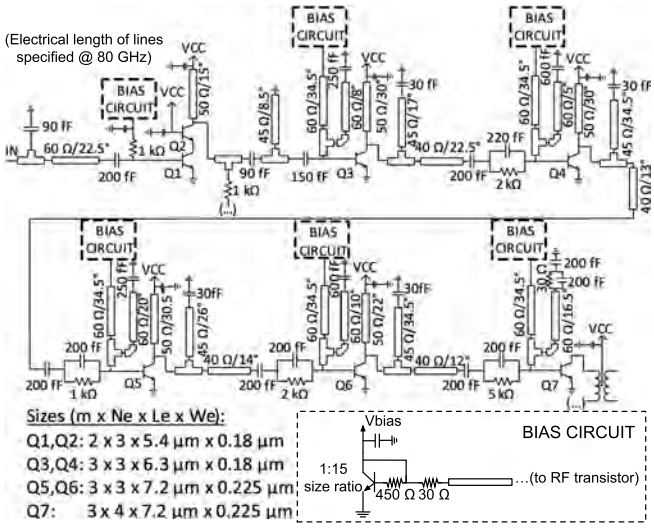


Fig. 11. Schematic of the designed single-ended unit cell.

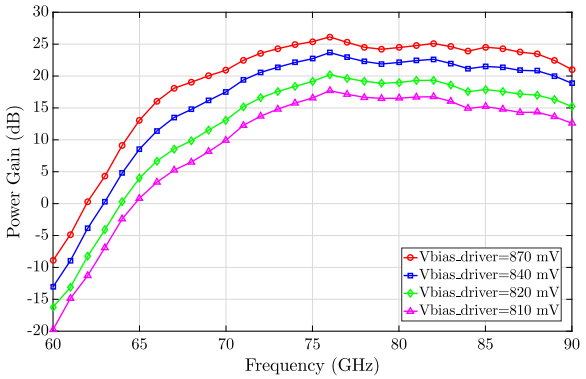


Fig. 12. Measured variation of PA gain versus driver dc bias.

version of the PA. As observed, a variation bigger than 8 dB can be obtained by changing the driver bias voltage from 810 to 870 mV.

B. Output Balun

An integrated transformer balun is used to combine the outputs of the two single-ended PA cells, since transformers provide low IL, high coupling coefficient, and compact layout simultaneously at mm-wave frequencies [26]–[28]. The balun is designed to minimize the IL at *E*-band frequencies and maximize its power combining efficiency. It is implemented on-chip using an octogonal stacked transformer structure like the one shown in Fig. 13. The primary is made using one turn of the ultrathick metal (M8), whereas the secondary is implemented using Alucap and M7 turns connected in parallel at the output. This way a high coupling coefficient (0.8–0.9) can be achieved and the lower M7 turn acts a shield for the primary. A P+ ring is placed around the structure to avoid induced currents spreading through the substrate and coupling to other parts of the circuit. The surrounding ground plane is implemented stacking the first two metals to minimize the resistance and maximize the quality factor. The coupling factor

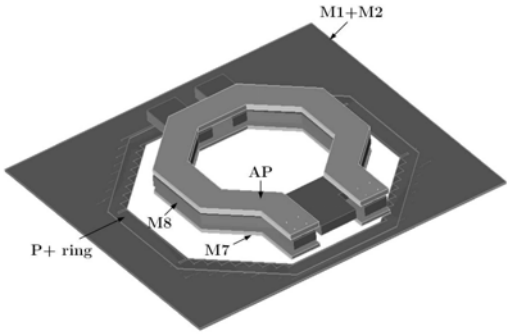


Fig. 13. 3-D view of the output balun transformer.

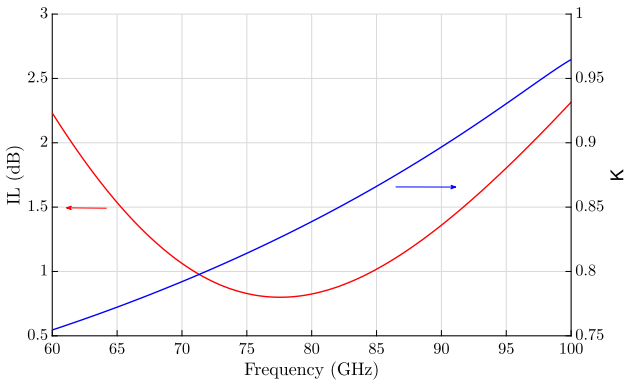


Fig. 14. Simulated IL and K of the output balun.

K is calculated as

$$\mathrm{K} = \sqrt{\frac{\mathrm{Im}(Z12)^2}{\mathrm{Im}(Z11)\cdot\mathrm{Im}(Z22)}} \tag{5}$$

and its simulated value is plotted together with the IL in Fig. 14. As shown, the IL is below 1 dB from 71 to 86 GHz, whereas the coupling coefficient is between 0.8 and 0.9.

Once the balun is designed, the connection to the output stage transistor cells is optimized, taking the parasitic inductance due to the length of the connections and the output pad capacitance (47 fF) into account. The arrangement is made as symmetrical as possible so as not to unbalance the output and to load the cells with equal impedances. In order to provide the required output power, each cell is loaded with ∼8 Ω.

C. Power Transistors

The high speed SiGe HBT transistors available in the technology provide f_T/f_{MAX} of 320/370 GHz, but their $\mathrm{BV_{CE0}}$ of 1.5 V limits the maximum collector–emitter voltage swing. Nevertheless, if the excess holes generated in the base–collector junction can flow out of the base, then they do not contribute to the avalanche multiplication effect and the breakdown limit can be reliably extended [29], [30]. Fig. 15 shows the simulated I_C versus V_{CE} curves of an HBT transistor when it is biased by a fixed I_B current or by a V_{BE} dc voltage connected through a resistor (RB). When the base current is fixed, the excess holes cannot flow out of the base and breakdown occurs at a voltage around 1.5 V. On the other hand, if there is a 0-Ω return path from the

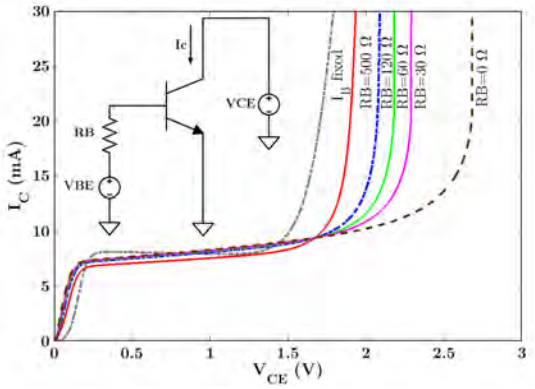


Fig. 15. IC versus VCE with RB as a parameter.

base to the emitter, then the breakdown limit is extended to around 2.5 V (more than x1.6 improvement). For moderate impedances the limit is above 2 V. Additionally, it is observed that the breakdown effect is also dependent on the current density (adjusted varying V_{BE}). An increase of the limit is observed at lower V_{BE} voltages, at the cost of having less current and consequently smaller gain.

Therefore the transistors are biased providing a V_{BE} voltage through proportional to absolute temperature mirrors and the bias circuits and matching networks are designed to provide a moderate impedance to the transistor bases (∼50 Ω at dc and ∼20 Ω at the *E*-band), which allow reliable operation at a Vcc voltage of 1.7 V. The CE stages are nominally biased at current densities of ∼1–3 mA/μm^2 that maximize the $\mathrm{BV_{CE0}}$ and thus the output power. In addition, biasing at low V_{BE} voltages makes the gain slightly increase when the PA is driven by large power signals, which helps increasing the 1-dB compression point by pushing it toward the saturation point. Special care is placed so that this gain expansion does not significantly degrade the IP3 of the amplifier, which is important when dealing with high-order modulations as 64-QAM. The driver stage is nominally biased at a current density of ∼5.5 mA/μm^2 to maximize the gain. The transistors are implemented with different cells in parallel, each with various fingers in Nx(CBEB)-C configuration to minimize the length to width ratio and consequently minimize the parasitic inductance and voltage drop along the fingers. The placement and spacing of the cells is done by carefully taking power management and reliability rules into account. Each cell is RCc extracted and the connections between and to the cells have been EM simulated to optimize the arrangement and to include all the effects introduced by the layout: parasitic capacitances, inductive/resistive degeneration, and so on.

D. Stability

Stability is an important issue when designing mm-wave PAs, especially when they have multiple stages. RC networks are placed at the inputs of the CE stages to increase the losses at lower frequencies and reduce the oscillation risk observed at frequencies around 20–30 GHz. The stability of the cascode stage is enhanced by placing a shunt 1-kΩ resistor at its output.

The simulated K and Δ stability factors of the complete PA up to 110 GHz are shown in Fig. 16.

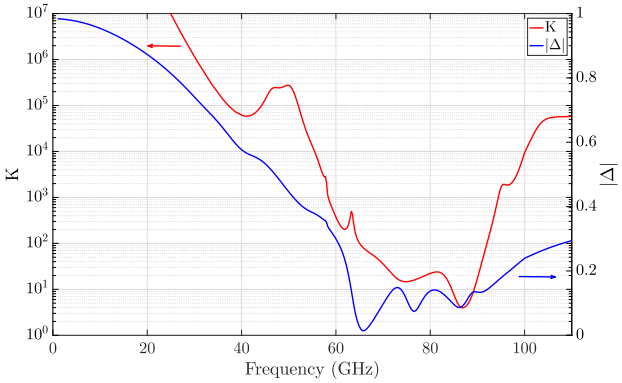


Fig. 16. K and |Δ| stability parameters of the PA.

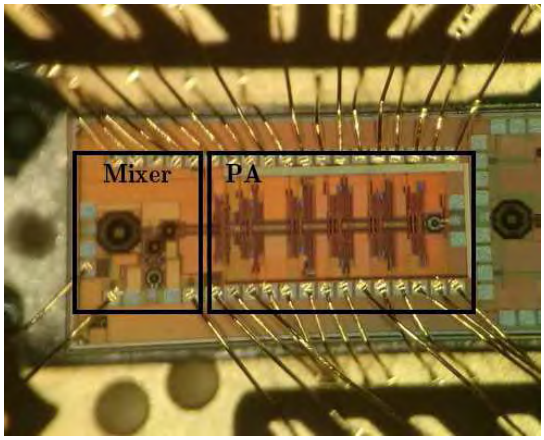


Fig. 17. Photograph of the fabricated chip.

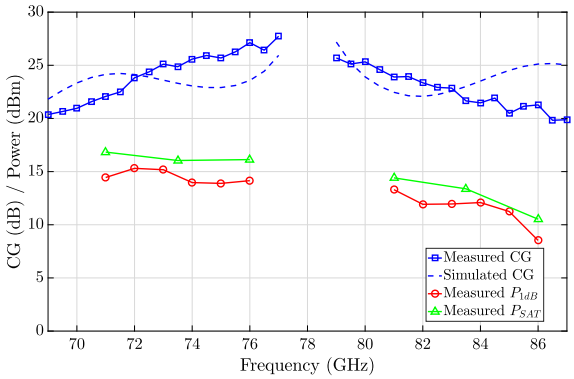


Fig. 18. Measured CG, P1dB, and Psat versus output frequency.

E. Matching Networks

The matching networks are designed to provide a broad bandwidth in both the gain and linearity of the amplifier. This is achieved by presenting a moderate impedance to the previous stages (∼30–40 Ω) which balances the gain and linearity, as well as by tuning the stages at slightly different frequencies to increase the overall bandwidth. The PA input is matched to 50 Ω to facilitate the integration with the mixer. The matching networks are implemented using transmission lines and MOM capacitors.

The transmission lines are constructed as side-shielded microstrip lines. The first two metals (M1 and M2) are stacked to provide a low-resistivity ground plane and increase the quality factor, with a loss of ∼0.6 dB/mm at E-band frequencies. The MOM capacitors are custom made using multiple fingers of the top ultrathick and thick metals, which have less resistive losses and lower parasitic capacitance to ground due to their bigger distance to the substrate. In addition, a ground shield with the M1 and M2 layers is placed underneath to further reduce the losses. This way it is possible to achieve high quality factors ($Q \sim 20$) at the band of interest.

Capacitors are placed at the end of the shunt transmission lines to prevent dc shorts. By carefully designing these LC networks, it is possible to provide the required reactance at E-band frequencies and simultaneously introduce a transmission zero at 50–60 GHz, which mitigates the effect of the LO feedthrough from the mixer.

The coupling effects between the different passive components are taken into account by EM simulations.

VI. Experimental Results

A. On-Wafer Measurement Results

The manufactured die occupies an area of 1.63 mm^2 and its photograph is shown in Fig. 17. It is attached and wire-bonded to a printed circuit board (PCB) to provide the dc bias to the circuit, whereas on-wafer ground-signal-ground probes are used for the RF signals. The measured and simulated CG of the E-band transmitter is shown in Fig. 18. For the measurement, the IF signal is swept between 14 and 22 GHz whereas the LO is set at 55 and 65 GHz with a power of 0 dBm. As shown, an average CG of 23 and 25 dB is measured at the lower band 71.125–73.125- and 73.625–75.625-GHz channels respectively, with a gain flatness of ±1.4 and ±0.8 dB across the channel bandwidth. As for the higher subband, the average measured CG is 23 and 21.5 dB at the 81.125–83.125- and 83.625–85.625-GHz channels, respectively, with a flatness of ±1.5 and ±0.7 dB.

Fig. 18 also shows the measured 1-dB compression point and output saturation power (P_{SAT}) versus output frequency. As observed, the $OP_{1\mathrm{dB}}$ is higher than 14 dBm in the lower subband, with a maximum of 15.3 dBm at 72 GHz, and higher than 11.2 dBm in the 81–85-GHz band. With regard to the saturation power, it has a maximum of 16.8 dBm at 71 GHz and it is higher than 12.3 dBm up to 85 GHz. A sharp decrease in the output power is observed at 86 GHz, which is thought to be caused by a mismatch in the impedance presented by the output balun to the last stage at this frequency.

Fig. 19 shows the simulated influence of temperature on the transmitter CG. If the base bias voltages are kept at their nominal values, a significant degradation can be observed, especially at −35 °C (the CG at this temperature falls below the area of the graph because it is around −40 dB). This is caused by the strong dependence of the HBT I–V curve on temperature. However, if an offset of around −1 mV/ °C is applied to the base bias voltages, then the performance can be brought back to the expected range, as shown in the figure (dashed lines). Thus, a linear temperature dependent bias circuit could easily be implemented to compensate for

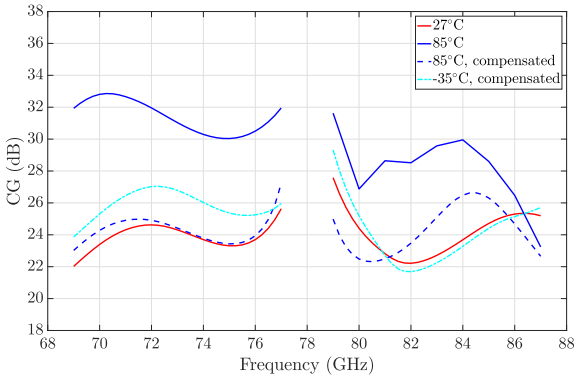


Fig. 19. Simulated CG versus output frequency as a function of temperature.

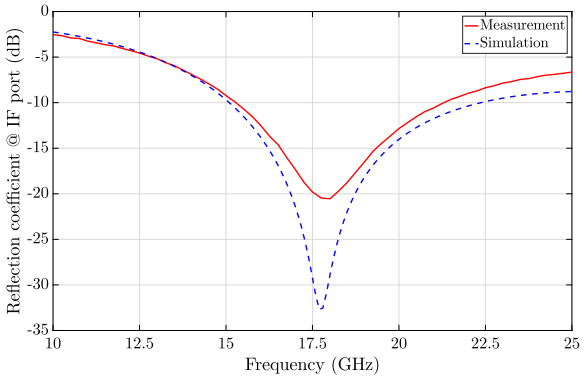


Fig. 21. Measured small signal reflection coefficient at the IF input.

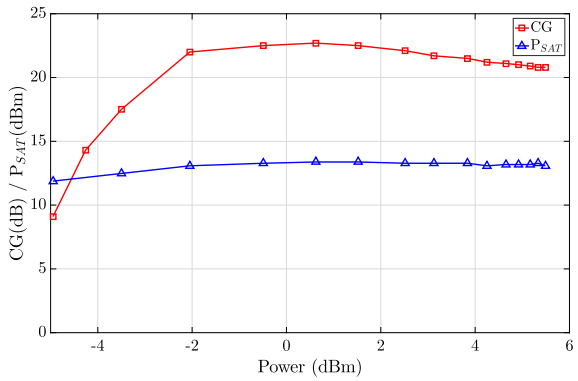


Fig. 20. Measured CG and saturation power versus LO power at 83.5 GHz.

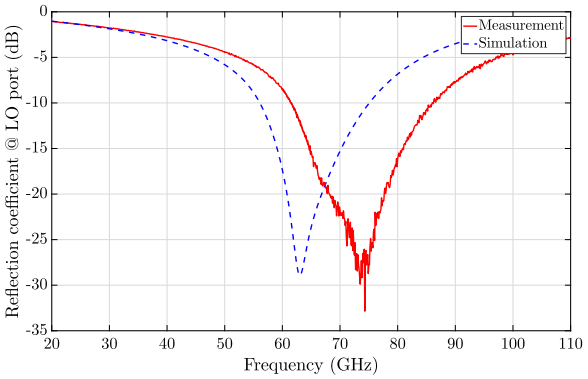


Fig. 22. Measured small signal reflection coefficient at the LO input.

the effect of temperature differences. Similarly, process corner simulations suggest that the effect of process deviations can also be minimized by applying an offset to the bias voltages.

Fig. 20 shows the measured CG and P_{SAT} as a function of the LO power at 83.5 GHz. The optimum performance in terms of gain and linearity is achieved for an LO power above -2 dBm. As shown, very little variation in P_{SAT} is obtained because the output power of the transmitter is mainly determined by the PA.

The measured LO feedthrough from the LO input of the mixer to the output of the PA is better than -50 dB at 55 GHz and better than -15 dB at 65 GHz. This feedthrough is thought to be caused by mismatches in the mixer structure as well as by coupling through the substrate and/or the measurement probes. Nevertheless, the obtained value is enough for the intended application because *E*-band diplexers (like the ones supplied by K&L Microwave or MtronPTI, for instance) typically attenuate more than 60 dB the spurs that fall out of the band. The small-signal reflection coefficient at the IF input port has also been measured, obtaining the results depicted in Fig. 21. It is well matched to 50 Ω at the IF frequency range, with a value lower than -10 dB from 15.2 to 21.3 GHz. As for the matching at the LO port, shown in Fig. 22, it is -6 dB at 55 GHz and -15 dB at 65 GHz. As observed, there is an up-shift in frequency with respect to simulations, which can be compensated by applying a bigger LO power at 55 GHz.

A Vcc value of 1.7 V is used for the PA and mixer, and of 1.2 V for the LO buffer. The base bias voltages are 650 mV for the mixer, 850 mV for the LO buffer and between 800–900 mV for the PA cells. The overall dc consumption of the *E*-band transmitter, under small-signal conditions, is 575 mW. According to what it is presented in Section II, this transmitter can be used to transmit a 64-QAM modulated signal with 2-GHz bandwidth over 1 km distance for rain rates below 45 and 35 mm/h at the lower and upper parts of the *E*-band respectively.

The main performance metrics of the presented transmitter are summarized and compared to other state of the art CMOS and BiCMOS *E*-band transmitters in Table III.

B. Multigigabit Signal Transmission Measurements

The performance of the implemented *E*-band transmitter with modulated multigigabit signals has also been evaluated, by means of the loop-back test setup shown in Fig. 23. This setup is intended to emulate the system proposed in Section III. The BB signal to be transmitted is generated using an FPGA (Xilinx VC707), and it consists of two digital subbands with 1 GHz bandwidth centered at -500 and 500 MHz, respectively, as described in Section III. The information in each digital subband is transmitted at a symbol rate of 869.6 Mbaud/s and it is organized in frames, with a short preamble for synchronization and equalization purposes.

The in-phase (I) and quadrature (Q) components of the modulated signal are converted to analog using a 14-bit 2.5-Gs/s DAC board (4DSP FMC230), attenuated (so as to operate the rest of the components in their linear region) and

TABLE III
COMPARISON OF STATE-OF-THE-ART CMOS AND BICMOS E-BAND TRANSMITTERS

Reference	Technology	Output Freq.(GHz)	Input Freq.(GHz)	Avg. Gain(dB)	P_{1dB}(dBm)	P_{SAT}(dBm)	P_{dc}
[9]	0.13 μm SiGe	71-76(chip1) 81-86(chip2)	Baseband Baseband	37.5 37.5	16-17.5 15.8-16.5	18.8-20 18-18.8	1.75 W (*) 1.8 W (*)
[10]	40 nm CMOS	71-86	Baseband	10	7-8.8	10-12.5	102 mW
[11]	0.35 μm SiGe	71-76(chip1) 81-86(chip2)	Baseband Baseband	25 25	N/A N/A	15(max) 15(max)	1.6 W (**) 1.6 W (**)
This work	55 nm SiGe	71-86	16-21	23	14-15.2(71-76 GHz) 8.5-13.3(81-86 GHz)	16-16.8(71-76 GHz) 10.5-14.4(81-86 GHz)	575 mW

(*)Including PLL, I/Q modulator and VGAs. (**)Including VCO.

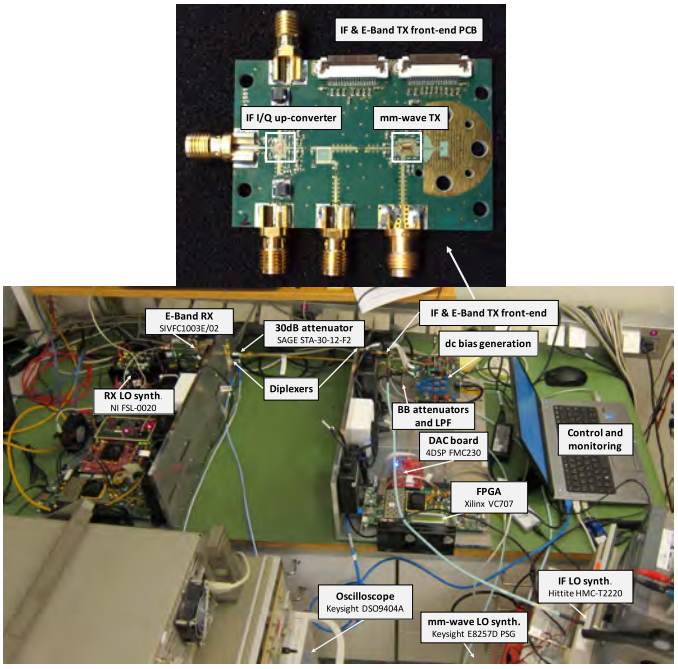


Fig. 23. Setup used for the loop-back test with a modulated signal.

then low-pass filtered. A custom IC I/Q upconverter is used to convert the signal from 0–1-GHz to 17.125/19.625-GHz IF. As for the introduced frequency selective phase and amplitude I/Q imbalance, it is compensated using digital predistortion following the procedure described in [31]. The implemented SiGe transmitter die is mounted on a PCB together with the I/Q upconverter. A standard FR-4 substrate with two copper layers is used for the dc traces, while a low-loss Rogers RO4350B substrate is attached on top of it for the RF and mm-wave transmission lines. SMA connectors are placed for the BB and IF LO signals. A 1.85-mm connector is used for the 55/65 GHz LO signal, whereas the E-band output is fed into a WR-12 waveguide. The FR-4 is removed at the WR-12 opening to minimize the loss.

E-band diplexers are placed at the TX output and RX input, connected through a WR-12 waveguide and a 30 dB attenuator (Sage STA-30-12-F2). A commercial E-band transceiver (Sivers IMA FC1003E/02) is used to down-convert the signal to a low-IF centered at 1.25 GHz. The received signal is captured using a 4-GHz oscilloscope (Keysight DSO9404A) and then analyzed using a demodulator implemented in MATLAB. This demodulator performs signal acquisition, synchronization, and equalization.

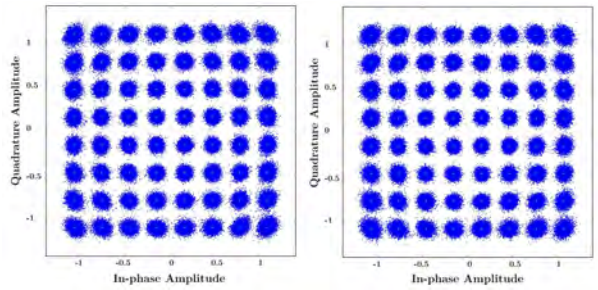


Fig. 24. Obtained constellations (left: lower subband, right: upper subband) when transmitting a 10 Gb/s 64-QAM modulated signal over the 72.125-GHz channel.

TABLE IV
SUMMARY OF LOOP-BACK TEST RESULTS

Freq. (GHz)	Bandwidth (MHz)	Modulation	Bitrate (Gb/s)[1]	EVM (%)[2]	P_{OUT} (dBm) [3]
72.125	2000	16-QAM 32-QAM 64-QAM	6.74 8.43 10.12	4.5/4.6 4.4/4.4 3.5/3.2	4
74.625	2000	16-QAM 32-QAM 64-QAM	6.74 8.43 10.12	3.6/5.5 3.7/5.2 3.2/4.5	4
82.125	2000	16-QAM 32-QAM 64-QAM	6.74 8.43 10.12	4.0/6.2 4.4/6.0 3.7/5.3	2
84.625	2000	16-QAM 32-QAM 64-QAM	6.74 8.43 10.12	6.1/7.1 6.5/7.9 5.3/6.4	1

[1]Raw data-rate of the payload.
[2]EVM of (Lower/Upper) sub-bands. [3] At the PA output.

Fig. 24 shows the received constellations when a 10-Gb/s signal is transmitted at the 72.125 GHz channel using 64-QAM modulation. The measured error vector magnitude is 3.5% and 3.2% at the lower and upper digital subbands, respectively. Table IV summarizes the measured performance for the tested channels and modulation schemes. As shown, a maximum bitrate of 10.12 Gb/s is obtained over a 2-GHz bandwidth using 64-QAM modulation, which corresponds to a spectral efficiency of 5.06 b/s/Hz. The output power has a back-off of around 10 dB below the OP_{1dB}. Fig. 25 shows the down-converted spectrum (at IF of 1.25 GHz) when the signal is transmitted through the 72.125-GHz channel. The ETSI spectral masks for class 5L (64-QAM) are also shown, extrapolated for a channel separation (CS) of 2000 and 2500 MHz (the CS considered in Section II of this paper). The masks have been extrapolated because class

TABLE V
COMPARISON OF STATE-OF-THE-ART MULTIGIGABIT *E*-BAND TRANSMITTERS

Reference	Technology	Modulation	Bitrate (Gb/ps)	Spectral eff. (bit/s/Hz)
[8]	CMOS	64-QAM QPSK	3 8	<6 <2
[9]	SiGe	64-QAM 128-QAM	0.6 0.7	<6 <7
[11]	SiGe	32-QAM	20	<5
[12]	SiGe	QPSK	18	<2
[13]	GaAs	8-PSK	6	2.4
[32]	SiGe	256-QAM	0.04	<8
[33]	CMOS	1024-QAM	0.5	<10
[34]	mHEMT	QPSK	10	<2
[35]	GaAs	16-QAM	5	3.2
[36]	GaAs	16-QAM	10	2
ELVA-1 PPC-10G	-	256-QAM	10	5
This work	SiGe	64-QAM	10.12	5.06

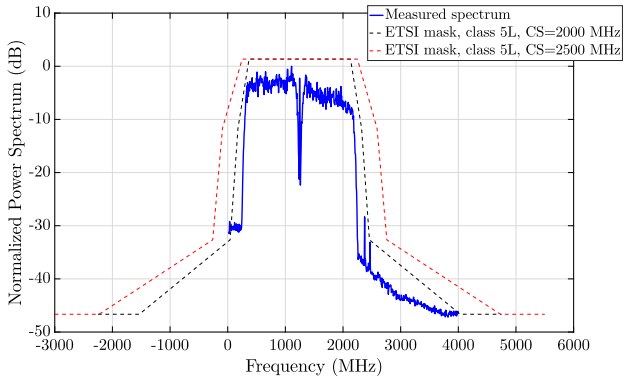


Fig. 25. Down-converted spectrum together with extrapolated masks for class 5L and CS = 2000 MHz and CS = 2500 MHz.

5L is not completely specified for CS bigger than 750 MHz yet [5]. Some spurs due to clock signal leakage in the FPGA and DAC can be observed, but they do not prevent from fulfilling the mask.

Table V compares the achieved performance with other reported state-of-the-art transmitters. It should be noted that, except the LO signal generators, the rest of the blocks used to generate, upconvert and down-convert the signal are made of custom implemented prototypes and commercial components rather than lab equipment as used in other reported testbenches.

VII. CONCLUSION

An integrated mm-wave transmitter has been presented, which can be used for the transmission of multigigabit signals in a proposed *E*-band point-to-point link for backhaul/fronthaul networks. The transmitter consists of a double-balanced bipolar ring upconverter mixer and a PA with 2-way output power combining. The performance of the implemented device is tested both standalone and together with other custom prototypes and commercial components in a loop-back setup in order to test the transmission of a multigigabit signal. A maximum datarate of 10.12 Gb/s is obtained with a spectral efficiency of 5.06 b/s/Hz. The presented *E*-band transmitter, integrated in a low cost technology, achieves a very good combination of broad bandwidth and high output power together with the capability of transmitting a spectrally efficient multigigabit signal.

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