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A 0.4–3.3 GHz low-noise variable gain amplifier with 35 dB tuning range, 4.9 dB NF, and 40 dBm IIP2

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Abstract This work presents a low-noise variable gain amplifier (LNVGA) in which the IIP2 is very high, and the gain control is applied to improve the system dynamic range, even with the limitations of the CMOS technology. Two stages compose the LNVGA, a low-noise amplifier, that keeps the noise figure (NF) at low values, and a variable voltage attenuator (VVA), that provides the gain variation. We have applied on the VVA the phase cancellation technique, in which the addition of two out-of-phase signals controls the gain. This technique provides a large gain tuning range only if the paths of the two signalsto be added are well balanced; hence, a precise 180 degrees phase difference is required. In this desing we propose an active balun with small imbalance, which creates those signals. The LNVGA was implemented in 130 nm CMOS with a 1.2 V supply. The measurement results show a 35 dB gain tuning range, varying from 10 to − 25 dB, a 4.9 dB minimum NF, a − 10 dBm IIP3, and an IIP2 as high as + 40 dBm.

Keywords Variable gain amplifier · Low-noise amplifier · Noise cancellation · Active balun · Moderate inversion

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1 Introduction

RF applications which target spectrum sharing within a wideband demand circuits that are not only highly linear but also low noise. The trade-off between these features, however, imposes limitations on their improvement [1, 6, 14]. A common way to overcome this limitation is to employ variable gain amplifier (VGA). However, this solution is mostly applied at low frequencies due to the limitation imposed by CMOS capacitances to the operation at gigahertz frequencies.

There are three possible methodologies to control the gain on the VGA: by tuning resistive elements, by tuning the bias voltage of one transistor, or by adding two signals with a 180 degrees phase shift (phase cancellation).

The resistive elements of the first methodology are usually replaced by transistors, that are biased in the triode mode of operation. And, the gain is controlled by changing the voltage at the gate of those transistors. This approach is applied in [11], and it achieves a significant gain control range (up to 60 dB gain variation). However, the transistors in triode are extremely noisy; thus, the noise figure of the circuit becomes prohibitively high. Moreover, the huge gain control range is achieved due to the utilization of multiple stages, that takes its toll on linearity. The second methodology, on the other hand, can achieve a low noise figure, as shown in [4, 15], yet these circuits are unable to get a large gain control range. The third methodology has been proposed in [9]. In addition to the large gain tuning range, this technique achieves an IIP3 above 0 dBm. However, in spite of these good features, the phase cancellation technique, as presented in [9], is unable to amplify the signal, so it suffers from a high noise figure which is undesirable in a receiver.

The above-mentioned VGAs achieve either a low-noise figure or a large gain tuning range. On the contrary, our low noise variable gain amplifier (LNVGA) achieves both of them. The LNVGA is composed of two-stages. The first one uses noise cancellation, achieving a low noise figure within a wide bandwidth. And the second one uses phase cancellation by which a large gain tuning range is achieved in a single stage. Moreover, the proposed balun achieves a small imbalance, which is crucial to the performance of the second stage.

This paper is organized as follows. Section 2 describes the main characteristics of the proposed and designed circuit. Section 3 shows the measurements of the fabricated circuit. Finally, Sect. 4 summarizes the contribution of this paper.

2 Circuit design

2.1 General concept

The LNVGA circuit has two stages: a low noise amplifier (LNA) and a variable voltage attenuator (VVA) as shown in Fig. 1(a). This combination provides a low noise figure, which increases sensitivity, when receiving weak signals. And, when receiving strong signals, it avoids their compression.

Since the first-stage has to provide a 50 Ω input match, in addition to a low NF, across a wide bandwidth, the LNA was designed using the noise-canceling technique [3, 8]. Moreover, the gain needs to be high enough to mitigate the second-stage noise contribution.

Figure 1(b) presents the block diagram of the VVA. The active baluns, A and B, split the input signal into two out-of-phase signals, then those are added at the output terminal so that they cancel each other [2, 9]. By fully turning on both baluns, the output signals completely cancel each other, achieving the minimum gain. On the other hand, by turning on only one of the baluns while the other one remains off, the gain is maximized.

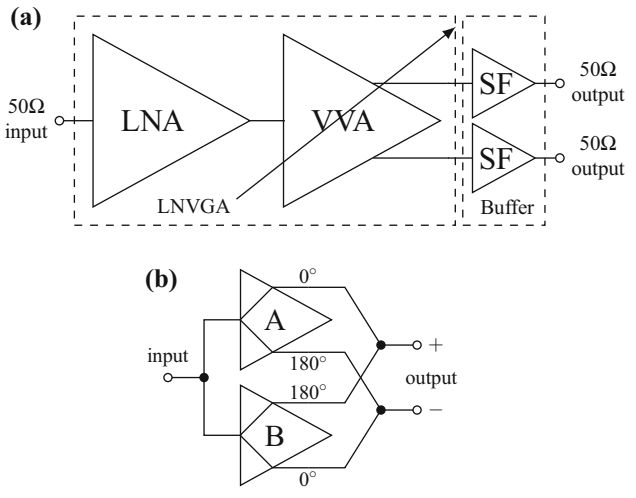

Fig. 1 Block diagram of the LNVGA with the measurement buffer (**a**). The VVA composed of two baluns (**b**)

Additionally, the signals at the output of the balun must have the same magnitude and a 180 degrees phase shift, i.e. a balanced output; otherwise, there will be only partial cancellation. Thus, the minimization of the imbalance is crucial to the VVA functioning.

The high power consumption is a disadvantage for the approach mentioned above, especially while working at minimum gain. Thus, our design targets g_m/I_D above 14 so that the transistors are in moderate inversion (MI) or weak inversion (WI), reducing the power consumption.

2.2 Low-noise amplifier

The LNA, which is presented in Fig. 2, uses noise cancellation, not only to provide a low NF over a wide band but also to break the trade-off between NF and input matching [3].

The noise factor of M1, M3, and R_{D3}, whose noise is to be canceled, are

$$F_{M1} = \frac{(\gamma/\alpha) g_{m1} R_s R_{D1}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{1}$$

$$F_{M3} = \frac{(\gamma/\alpha) g_{m3} R_s g_{m1}^2 R_{D1}^2 R_{D3}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{2}$$

$$F_{R_{D3}} = \frac{R_S R_{D3} g_{m1}^2 R_{D1}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{3}$$

where γ and α are noise parameters. These equations also show that only if the condition

$$\frac{g_{m2A}}{g_{m2B}} = \frac{R_{D1}}{R_S} \tag{4}$$

is fulfilled, the noise is fully cancelled.

Therefore, the noise factor of the LNA is reduced to

$$F_{LNA} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{g_{m2A} R_S} + \frac{g_{m2B}}{g_{m2A}^2 R_S}\right) + \left(\frac{g_{m2B}}{g_{m2A}}\right)^2 \frac{R_{D1}}{R_S} + \frac{1}{g_{m2A}^2 R_S R_{D2}}. \tag{5}$$

Furthermore, g_{m2A} is limited by the size of M2A because C_{gs2A} will become too large, damaging the input matching at high frequencies. Nevertheless, g_{m2A} has to be

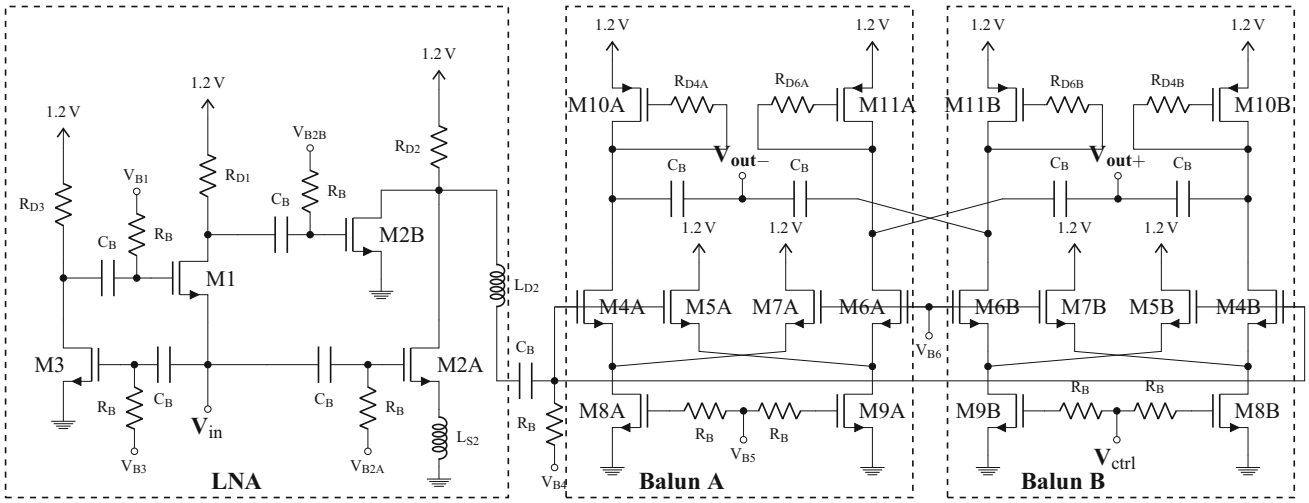

Fig. 2 The LNVGA schematic

maximised, for the main noise source is M2A, and the only way to reduce its noise is by increasing g_{m2A}. As a result, an inductor is connected to the source of M2A, that reduces the damage caused to the input matching by C_{gs2A}.

In addition, g_{m2B} is limited not only by the size of M2B since C_{gs2B} can make the pole at M2B gate, $1/R_{D1}C_{gs2B}$, shift to low frequencies, but also by the ratio g_{m2A}/g_{m2B}, which is proportional to R_{D1} and shifts the same pole. In this design the ratio g_{m2A}/g_{m2B} is kept below 20, which limits R_{D1} to 1 kΩ, and M2B is designed as small as possible.

Sizing down M2B, as long as the g_m/I_D remains fixed, reduces g_{m2B}, yet it has a small effect on the total noise since the signal was previously amplified by M1 and R_{D1}. On the other hand, the linearity is improved by reducing g_{m2B}.

The LNA uses g_m-boosting [4] to make the selection of the M1 transconductance (g_{m1}) flexible. The LNA input impedance needs to match the source impedance (R_S), that is 50 Ω. Consequently, without g_m-boosting, the g_{m1} must be equal to 20 mS. On the other hand, with g_m-boosting, the boosted g_{m1}, which is $G_{m1} = g_{m1}(1 + g_{m3}R_{D3})$, is the one to be equal to 20 mS. Therefore, g_{m1} can have any value.

However, it is important to mind the pole created by the local feedback, $1/(R_{d3}C_{gs1})$, at the gate of M1. It is necessary for best performance to place this pole at a frequency higher than the dominant pole so that it does not reduce the bandwidth.

Every transistor of the LNA is biased in MI, that reduces the power consumption, reduces the noise [5], and increases the linearity [10]. The designed transistor sizes and their g_m/I_D are presented in Table 1.

However, biasing the transistors in MI eventually requires the designer to enlarge them, which increases their parasitic capacitances, reducing the circuit bandwidth. Thus, a second inductor is connected to the output of the LNA, which extends its bandwidth.

Table 1 The transistors parameters of the LNVGA

	g_m/I_D	W (μm)	L (μm)	Region
M1	15.82	35	0.12	MI
M2A	18.52	400	0.12	MI
M2B	18.73	10	0.12	MI
M3	16.84	15	0.12	MI
M4, M5	16.34	84.98	0.12	MI
M6, M7	14.24	84.98	0.12	MI
M8, M9	4.2	30	0.18	SI
M10, M11	15.54	300	0.12	MI

2.3 Variable voltage attenuator

The VVA is composed of two identical baluns, which are presented in Fig. 2. Also, in order to change the gain, one balun needs to have a fixed gain while the other one needs to have variable gain. Hence, V_{B5} that controls the gain of Balun A has a fixed value of 0.7 V, and V_{ctrl} that controls the gain of Balun B is swept from 0 to 0.7 V. The gain, in fact, will be maximum when V_{ctrl} is 0 V, meaning that Balun B is turned off; on the other hand, the gain will be minimum when V_{ctrl} is 0.7 V.

By means of a differential pair where one of the inputs is ac-grounded, a simple balun can be created. However, both the g_{ds} of the tail and the C_{gd} of the differential pair degrade the signal balance. These issues are usually overcome by increasing the current of the differential pair and

the tail, yet this solution is insufficient because of the load, which reduces the drain voltage of the differential pair with the increasing current, driving the transistors into the triode region.

Therefore, a different technique has been proposed in this paper, adding an auxiliary crossed pair (M5A, M5B, M7A, M7B in Fig. 2) to the differential pair. This crossed pair largely reduces the imbalance caused by the tail, which is the dominant source of imbalance. Since the imbalance caused by C_{gd} is much smaller than the one caused by the tail, the former is neglected.

Furthermore, the positive and negative transfer functions are

$$\frac{v_{out-}}{v_{in}} = -\frac{g_{m4}(g_{m5}+g_s)\left(\frac{C_{gs}+C_s}{g_{m5}+g_s}s+1\right)}{Y_L(g_{m4}+g_{m5}+g_s)\left(\frac{2C_{gs}+C_s}{g_{m4}+g_{m5}+g_s}s+1\right)} \tag{6}$$

and

$$\frac{v_{out+}}{v_{in}} = \frac{g_{m4}g_{m6}\left(\frac{C_{gs}}{g_{m5}}s+1\right)}{Y_L(g_{m4}+g_{m5}+g_s)\left(\frac{2C_{gs}+C_s}{g_{m4}+g_{56}+g_s}s+1\right)}, \tag{7}$$

where g_s and C_s are, the conductance and the capacitance, respectively at the drain of M8 and M9. Additionally, Y_L is the load admittance and C_{gs} is the gate-to-source capacitance of M4, M5, M6, and M7.

The transistors M4, M5, M6, and M7 are equal but for their g_m/I_D, those are different if the transistors are either at the differential pair or the crossed pair. In addition to the different g_m/I_D, both M5 and M7 are directly connected to VDD, which allows them for a larger current; hence, their g_m is also high.

Furthermore, we can notice from (6) and (7) that, increasing g_{m5}, reduces the effect of g_s, which increases the simmetry of those equations. Their simmetry can be further improved by minimizing C_s, which is done by biasing both M8 and M9 on SI.

The balun bandwidth is enhanced by using, as the load, an active inductor [12, 13] that generates both a zero, $1/R_{D4}C_{gs10}$, and a pole, g_{m10}/C_{gs10}. The new pole will become the dominant pole, while the new zero will cancel the old dominant pole. However, not only the active inductor reduces the LNVGA gain, but it also increases its noise. Thus, the LNA must be designed to compensate for those issues.

2.4 Measurement buffer

The LNVGA has been designed to drive a capacitive load, which emulates the input of an active mixer, whereas every measurement equipment has a 50 Ω impedance. Thus, a highly linear source-follower buffer has been added to the LNVGA to provide the impedance matching with the measurement setup.

Since the buffer needs to have minimum effect on the circuit performance, thick-oxide 3.3 V transistors were used so that it achieves a high linearity. The linearity of the LNVGA, therefore, is unaffected by the buffer.

However, the buffer still reduces the gain and increases the noise of the overall circuit integrated on the chip, of which the LNVGA circuit is part of. These issues are circumvented by de-embedding their effects from the measurement results obtained from the fabricated integrated circuit which has the LNVGA and integrated buffers.

Figure 3 shows the buffer, that uses complementary transistors. In addition to reducing the power consumption, this buffer has superior linearity.

Due to the buffer capacitive input, it is impossible to test a standalone version. Hence, simulation results from the buffer are used for the de-embedding. As the de-embedding methodology was extensively discussed by [7], it will not be further discussed here.

In order to compensate for the losses on the buffer and the single-to-differential conversion, 9 dB are added to the measured value of S21, which gives the voltage gain of the LNVGA. The compensation for the noise figure, on the other hand, is not constant since the LNVGA has a variable gain, and the contribution of the buffer to the noise figure is inversely proportional to the LNVGA gain. The buffer will increase the total noise figure by 2 dB when the gain of the LNVGA is maximum. Moreover, the same buffer will increase the total noise figure by 5 dB when the gain of LNVGA is close to 0 dB.

2.5 Corner and Monte Carlo results

The Monte Carlo results are presented in Fig. 4 for 200 samples at 1 GHz. The mean S11 is − 15.2 dB with a standard deviation of 0.4 dB as shown in Fig. 4(a). Thus, the input of the LNVGA remains matched to 50 Ω regardless of process variation. The effect of process variation on both gain and NF is also reduced. Figure 4(b) shows that the mean voltage gain is 14.5 dB with standard deviation of 0.52 dB. Meanwhile, Fig. 4(c) shows

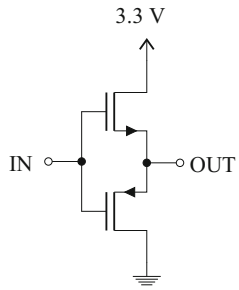

Fig. 3 Highly-linear measurement buffer

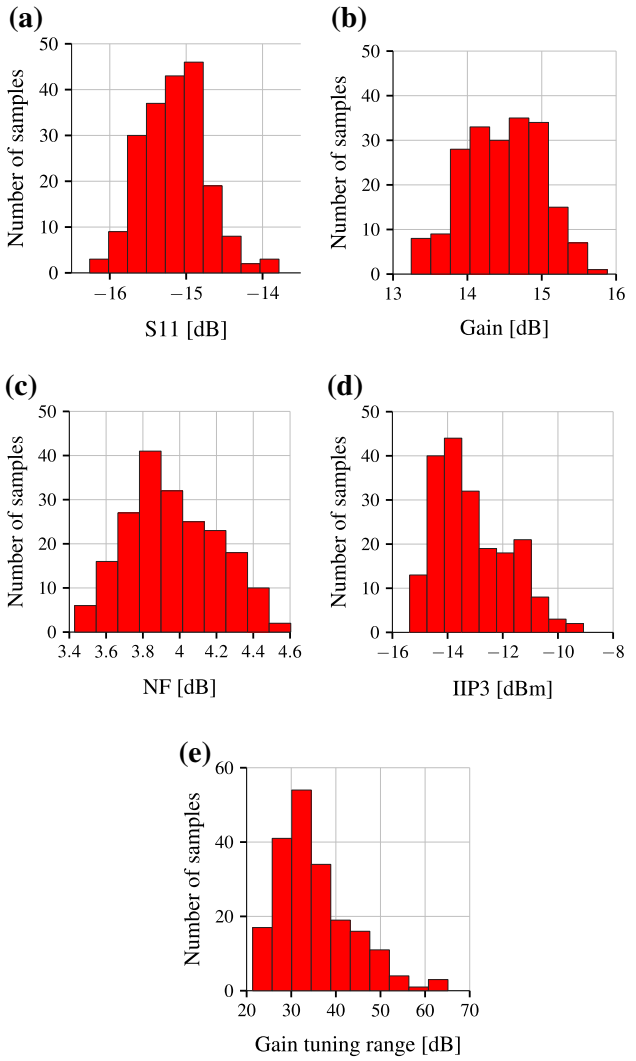

Fig. 4 The LNVGA Monte Carlo results of 200 samples. Input reflection coefficient (**a**), voltage Gain (**b**), NF (**c**), IIP3 (**d**), and gain tuning range (**e**)

a mean NF of 3.96 dB with a standard deviation of 0.24 dB. The deviation from the mean presented by the IIP3 is slightly larger than that presented by NF or gain. As shown in Fig. 4(d), the mean IIP3 is − 13 dBm and the standard deviation is 1.3 dBm.

The process corner simulation shows a small variation from the worst to the best case. The corner slow–fast (SF) which is the worst case shows a voltage gain and NF of 13.5 and 4.4 dB respectively, whereas the corner fast-slow (FS) which is the best case shows a voltage gain and NF of 15.5 and 3.4 dB respectively. The worst S11 is − 14.4 dB at the slow–slow (SS) corner.

The result most sensitive to process variation and corners is the gain tuning range because the minimum gain strongly relies on the matching between the two active baluns. Although the layout of the active baluns have been done so that the effect of process variation is mitigated on the gain tuning range, the gain tuning range of the LNVGA still presents a deviation from the mean of 8.4 dB. The mean gain tuning range is 35 dB, as shown in Fig. 4(e). The worst case corner is the fast–fast (FF) in which the gain tuning range is 22 dB.

3 Measurement results

The LNVGA, which is presented in Fig. 5, was fabricated in the process 130 nm CMOS with a 1.2 V supply.

Even though the entire area of the chip is 1 mm^2, the active area of the LNVGA is much smaller, only 0.15 mm^2, in which more than 50% of the area is occupied by inductors. Moreover, the LNVGA draws 23 mW when the gain is minimum, and it draws 15.6 mW when the gain is maximum. Since both Balun A and Balun B are turned on when the gain is minimum, the power drain on this condition is higher than the power drain at maximum gain. The power consumed by the LNVGA can be further reduced if the transistors are biased in WI, but then more inductors are needed.

The gain has been measured between 400 MHz and 4 GHz as shown in Fig. 6. By sweeping the V_{ctrl}, we observe a maximum gain of 10 dB and a minimum gain of − 25 dB, hence a gain control range of 35 dB. As shown in Table 2, the gain control range of the LNVGA is the second largest reported. Although we can further increase the range of the LNVGA gain control by increasing the gain of the VVA, this option has been discarded since it increases the power consumption. Figure 6 also shows the 3 dB cutoff frequency of the LNVGA which is measured as 3.3 GHz.

Measurements of the input reflection coefficient (S11), shown in Fig. 7, demonstrate that, regardless of the gain, the LNVGA input remains matched to 50 Ω, and also that the S11 is below − 10 dB inside the entire band.

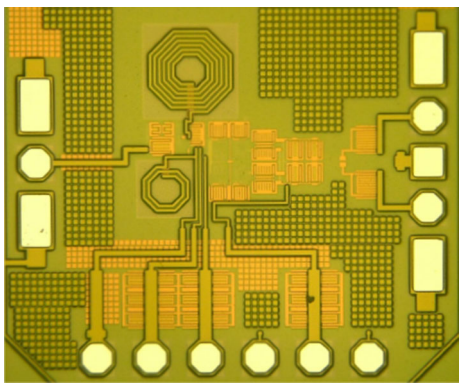

Fig. 5 The photograph of the LNVGA chip

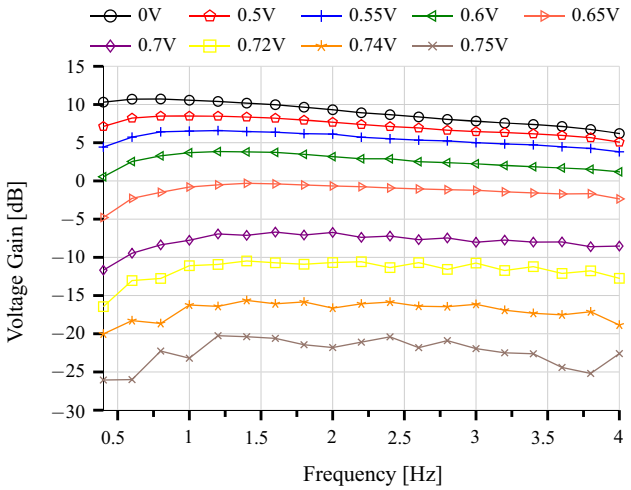

Fig. 6 Measured voltage gain and gain control range

The noise figure (NF), on the other hand, changes a lot with the gain. As long as the LNVGA gain is higher than 0 dB, the LNA holds the NF below 7 dB. When the LNVGA gain is lower than 0 dB, the NF sharply rises, reaching values as high as 20 dB. Moreover, the minimum NF is 4.9 dB at 500 MHz.

Figure 8 shows the measured NF over the entire band, at the maximum gain, after and before de-embedding from the measured NF data.

Figure 9 shows the IIP3 and P1dB, which remains almost constant regardless of the gain. The IIP3 is around − 10 dBm, while the P1dB varies in between − 18.56 and − 17.1 dBm. The linearity of the circuit is limited by the 2-stage topology although the gain of the second stage is low. Eventually, the linearity can be improved by modifying the circuit to a fully differential topology, that increases the linearity of the LNA.

In addition to enhancing the LNVGA bandwidth, the active inductor can partially cancel the second-order intermodulation (IM2) component, provided that the IM2 created by the active inductor cancels the IM2 created by the differential pair. As a result, when V_{ctrl} is 0.7 V, the LNVGA achieves an IIP2 as high as 40 dBm.

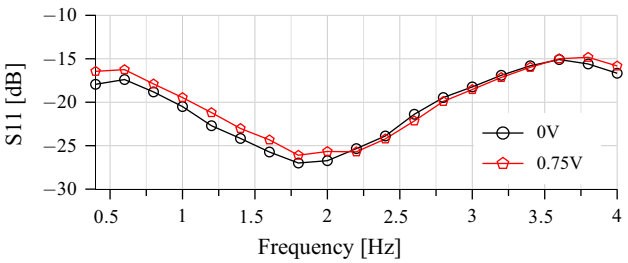

Fig. 7 Measured S11 at maximum and minimum gain

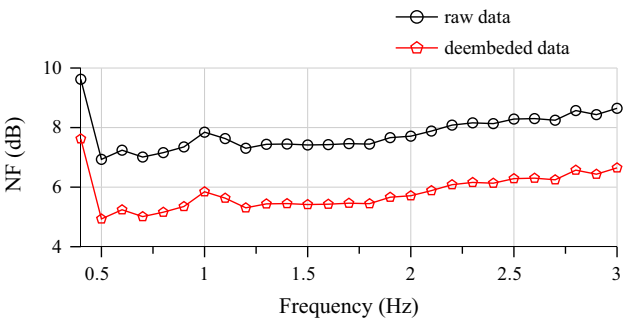

Fig. 8 Measured NF at maximum gain

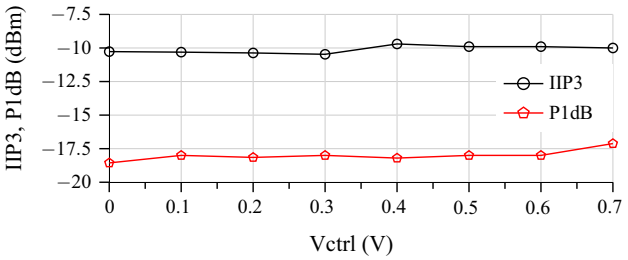

Fig. 9 Measured variation of IIP3 and P1dB within the gain control range

The best IIP2 is shown in Fig. 10(a), while the worst IIP2, which is 10 dBm, is shown in Fig. 10(b).

In comparison with similar works, which are presented in Table 2, the gain control range of the LNVGA is only smaller than the result presented in [11]. However, despite the larger gain control range presented in [11], its results of

Table 2 LNVGA results in comparison with similar works

REF.	Gain (dB)	Min. NF (dB)	IIP3 (dBm)	BW (GHz)	Power (mW)	Area (mm^2)	CMOS process (nm)
[15]	− 10 to 8	4.2	1.8	0.03–7	9	1.16	180
[9]	− 30 to − 2.6	N/A	3	1–3.5	18	0.05	180
[11]	− 10 to 50	17	− 45.4 to − 3.4[a]	0.01–2.2	2.5	0.01	90
[4]	− 5 to 11	3.2	− 4.5 to 0	1–5	19	0.067	180
This work	− 25 to 10	4.9	− 10	0.4–3.3	15.6	0.15	130

[a]Calculated from P1dB

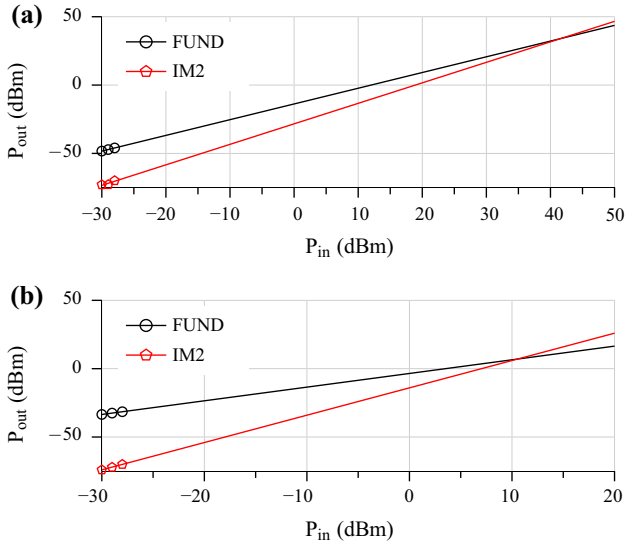

Fig. 10 Best case IIP2 at V_{ctrl} = 0.7 V (**a**) and worst case IIP2 at V_{ctrl} = 0 V (**b**)

NF, IIP3, and bandwidth are much worse than the results of our proposed LNVGA design. In fact, Wang et al. [11] reports a minimum NF of 17 dB, much higher than that achieved in the LNVGA herein designed and measured.

Furthermore, the NF of the LNVGA is slightly higher than the NF presented by either [15] or [4], but with a much larger gain tuning range. The LNVGA gain tuning range is 17 dB larger than the results shown in [15] and is 19 dB larger than the results shown in [4]. Moreover, the power consumed in [4] is even higher than the LNVGA, and the area reported in [15] is almost 10 times larger than the LNVGA.

In a nutshell, the LNVGA is the only one that provides both a large gain tuning range and a low noise figure.

4 Conclusion

A LNVGA has been presented. It was designed, fabricated, and measured in 130 nm CMOS process. The LNVGA provides not only a low noise figure but also a large gain tuning range within a wide band, from 400 MHz to 3.3 GHz. In fact, previously reported circuits have failed to improve both features simultaneously. Moreover, it has been proposed in this design a low imbalance active balun, which allows for the large gain tuning range. The active balun employs an active inductor which enhances both the bandwidth and the IIP2. The LNVGA at the maximum gain draws 15.6 mW from a 1.2 V supply. Also, it has achieved a rather large gain control range, 35 dB, a very high IIP2, + 40 dBm, and low noise figure, 4.9 dBm.

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