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Low-power low data rate FM-UWB receiver front end

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Abstract: This study introduces a frequency modulated ultra-wideband (FM-UWB) receiver optimised for low power and fast start-up. The receiver consists of a front end amplifier converting a frequency modulated signal to an amplitude modulated signal which is applied to an envelope detector. The receiver front end is for 500 MHz channels centred at 3450 and 3950 MHz. The amplifier uses passive gain and four cascaded gain stages to achieve high radio-frequency gain without the need for super-regeneration. By simplifying the architecture this way, the front end has a 5 µs wake-up time to enable efficient duty-cycling. The measured front end receives a signal at −68 dBm while consuming 600 µW of power (excluding a test buffer) from a 1 V supply. Fabrication was done using the IBM 130-nm CMOS technology on a 1 mm × 1 mm loose die.

1 Introduction

Frequency modulated ultra-wideband (FM-UWB) receiver optimised for low-power consumption and fast start-up is described. As demand for radio-frequency (RF) bandwidth increases, popular spectrum become more crowded [1]. This creates motivation to operate outside the popular narrow-band channels such as 940 and 2400 MHz [2]. Work to specifically improve low power wireless body area networks (WBANs) is also motivated by a rapidly increasing proportion of the global population that suffers from chronic diseases [3–5]. With the internet of things becoming increasingly popular, new technologies to meet demand in high traffic *ad-hoc* networks are also required [6, 7].

Of the proposed ultra-wideband (UWB) communication standards, two are outlined in the IEEE802.15.6 standard for WBANs. Impulse radio UWB is suitable for high data rate applications, while FM-UWB is suitable for low complexity, low data rate receivers in crowded environments [8]. FM-UWB also allows multiple sub-channels to be used within the same main channel, increasing spectrum efficiency.

FM-UWB has the output power limited to −41 dbm/MHz, meaning large channel bandwidth must be used to increase the range of communications [2, 9, 10]. Using 500 MHz channels allows −14 dBm of total output power to be transmitted. As shown in Fig. 1*a*, the data is encoded into the frequency of a sub-carrier, which modulates the frequency of the carrier signal. By sweeping the carrier frequency across the entire 500 MHz channel, the output power is kept within the Federal Communications Commission (FCC) mask [11] while allowing maximum total transmitted power. By encoding data in the sub-carrier, multiple channels can use the same RF band without interference [2, 12–14]. The modulation is shown in Fig. 2.

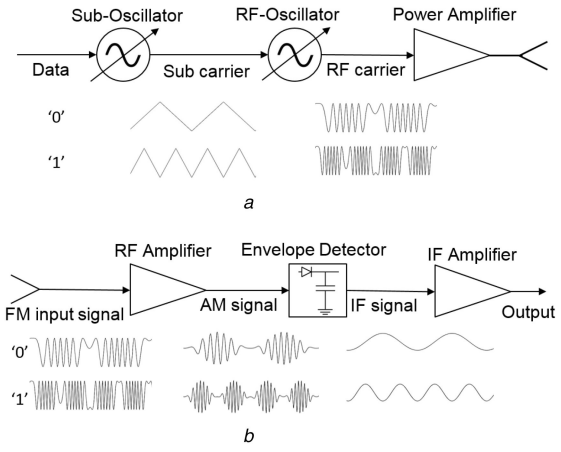

Fig. 1 *Block diagram for FM-UWB transceiver*
(a) An FM-UWB transmitter block diagram, ***(b)*** Block diagram for FM-UWB receiver front end. The constant amplitude input signal is converted to an amplitude modulated signal and the resultant AM signal is passed through an envelope detector [15]

The receiver portion for FM-UWB is based on an RF amplifier or filter that introduces a slope in the frequency response. The amplifier or filter converts the FM wireless signal to an amplitude modulated (AM) signal from which the sub-carrier is recovered using an envelope detector. The process is illustrated in Fig. 1*b*.

The early work in this variety of FM-UWB communicating was done by Long and co-workers [2, 16]. Some improvements in digital calibration were made in [17], eventually bringing the receiver power down below 1 mW [13]. The work by Kopta *et al.* in [14] cites even lower power consumption by using a super-heterodyne architecture to amplify the incoming signal below the carrier frequency at the cost of increased circuit complexity.

A further benefit of FM-UWB is the receiver does not require a phase locked loop (PLL) to function [2, 18].

The design presented here has a higher power consumption and lower data rate than [14], but uses a less expensive technology and is optimised for a fast start-up and duty cycling. What makes this

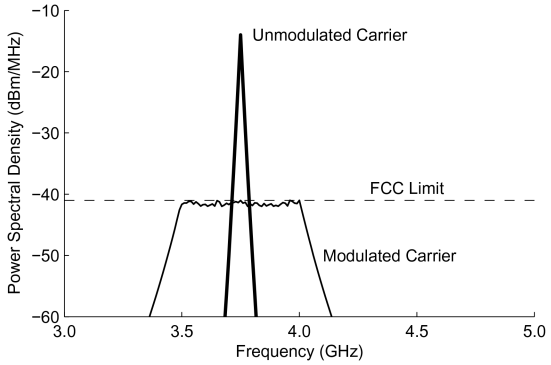

Fig. 2 *FM-UWB transmitter implemented using a sub-carrier oscillator to modulate an RF oscillator and produce a constant envelope output signal [15]*

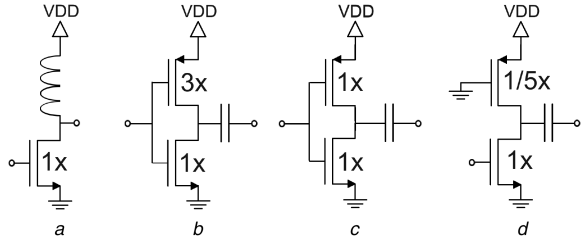

Fig. 3 *Various choices for the design of individual amplifier stages to be used in cascade are*

(a) Inductive loading, ***(b)*** Symmetric push–pull inverter, ***(c)*** Asymmetric push–pull inverter, ***(d)*** Pfet resistive loading

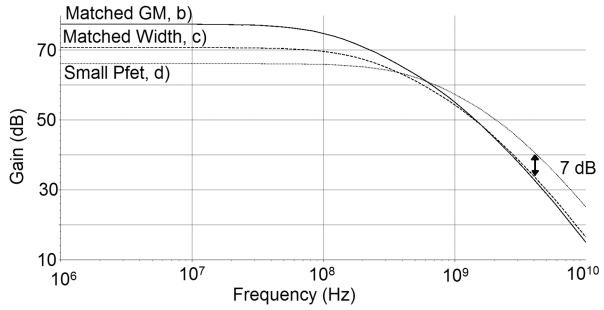

Fig. 4 *Simulation results for three cascaded stages of the amplifiers in Fig. 3b–d. All stages consume 100 μW of DC power*

circuit unique is the elimination of a super-regenerative amplifier at the input, which requires calibration at start-up as in [12, 13, 16]. The circuit implemented here uses only a multi-stage RF amplifier and allows for a 5 μs simulated wake up time. As the wake up time is smaller than any intended bit period, it can be thought of as a nearly instantaneous wake up, resulting in a negligible loss of transmission time.

Section 2 of the paper is the circuit design, which outlines the design of the RF amplifier, envelope detector, and intermediate-frequency (IF) amplifier. The circuit design is followed by the measurement results Section 3 which includes discussion and comparison to state-of-the-art. Section 4 is the conclusion, and then acknowledgements are made in Section 5.

2 Circuit design

The overall block diagram and example demodulations signals are shown in Fig. 1*b*. As previous designs used super-regeneration to achieve high gain, an attempt was made here to use a single gain path, reducing the need for tuning or calibration within the amplifier circuit.

Several options for low power amplifier stages are shown in Fig. 3. The inductive loading in Fig. 3*a* provides the best performance in terms of gain, noise figure, and power consumption, but at the cost of die area and circuit stability. The balanced push–pull inverter in Fig. 3*b* allows the current through the circuit to be reused twice, but the larger pfet transistor introduces more significant parasitics than an nfet transistor due to less electron mobility. By scaling the pfet device to be of equal size to the nfet device as shown in Fig. 3*c*, the parasitics are reduced by around 50% while the transconductance is reduced by just 33%. Using the pfet as only a load biased by the full supply voltage in Fig. 3*d*, the required size of the pfet is further reduced cutting parasitics from the symmetric case by around 70% while transconductance is reduced by 50%.

In a simple amplifier model considering only the parasitic capacitance and transconductance, cases (a), (b), and (c) compare as follows.

Each nfet has 1 arbitrary unit of transconductance, and one unit of capacitance. Each identically sized pfet has one-third the transconductance, but the same unit of capacitance. A pfet sized 3× larger has a single unit of transconductance, but three units of capacitance.

The transconductance-to-capacitance ratio is given by

$$\frac{gm}{C_\mathrm{p}} = \frac{gm_\mathrm{n} + gm_\mathrm{p}}{C_\mathrm{n} + C_\mathrm{p}} \tag{1}$$

For each describes amplifier stage the ratios are as follows:

$$\frac{gm_\mathrm{n} + gm_\mathrm{p}}{C_\mathrm{n} + C_\mathrm{p}} = \frac{1+1}{1+3} = 1/2 \tag{2}$$

$$\frac{gm_\mathrm{n} + gm_\mathrm{p}}{C_\mathrm{n} + C_\mathrm{p}} = \frac{1+1/3}{1+1} = 4/6 \tag{3}$$

$$\frac{gm_\mathrm{n} + gm_\mathrm{p}}{C_\mathrm{n} + C_\mathrm{p}} = \frac{1+0}{1+1/5} = 5/6 \tag{4}$$

Amplifiers are set up using three cascaded stages of the amplifiers in Figs. 3*b–d* and the simulated gain is shown in Fig. 4. The mismatched *gm* in designs (c) and (d) reduce the DC gain of the circuit, but at high frequency the small pfet design in Fig. 3*d* shows higher gain by 7 dB at 4.0 GHz.

2.1 RF front-end amplifier

The circuit for the front-end RF amplifier is shown in Fig. 5. The signal is first amplified passively by the resonance of inductor L_r and parasitic capacitances at the gate of M2. The passive gain, similar to that shown in [19], is given by

$$\frac{V_\mathrm{g}}{V_\mathrm{i}n} = \frac{(1/\mathrm{j}\omega C_\mathrm{eq})}{\mathrm{j}\omega L_\mathrm{r} + R_\mathrm{p} + (1/\mathrm{j}\omega C_\mathrm{eq})} \tag{5}$$

where L_r is the series inductance to the gate of M2 and C_eq is the equivalent capacitance at node V_g. Inductor L_r is tuned for resonance with C_eq, cancelling the reactive components in the denominator to give

$$\frac{V_\mathrm{g}}{V_\mathrm{in}} = \frac{(1/\mathrm{j}\omega C_\mathrm{eq})}{R_p} = -\frac{\mathrm{j}\omega L_\mathrm{r}}{R_p} = -\mathrm{j}Q_\mathrm{L} \tag{6}$$

where Q_L is the quality factor of inductor L_r.

The passive gain is affected by the Miller effect at the first stage, so a cascode structure with inductive loading is used. The inductor is tuned for self-resonance at the same frequency as the passive gain to provide a narrowband peak in the overall amplifier gain. M2 is sized at only 10 μm while M1 is 25 μm. This way, M2 acts as a cascode buffer while M1 provides amplification at the resonant frequency of inductor L_dd. The cascode structure also provides reverse isolation to improve the stability at the first stage. The following three stages are identical and are optimised for the highest possible gain. Resistors in the IBM 130-nm technology are larger than Pfet transistors to achieve the same resistance, so loading is implemented with pfet transistors biased in the triode region. The VSG bias voltage is the full 1.0 V difference from VDD to ground. By using a maximum bias voltage, the transistors can be as small as possible and have the lowest possible parasitic capacitance at the drain. The first stage is externally biased with VG1 through transistor M9. A 10 pF on chip capacitor (not shown) is included to filter the bias pad. Each of the three subsequent stages is biased at VG2 with a separate pad and is individually decoupled. All component values for the circuit are summarised in Table 1. The method used by Saputra and Long [13, 16] is to include a super-regenerative RF amplifier, biased on the edge of instability. The four-stage RF amplifier presented here has 48 dB of gain and a slope of −140 dB/decade as shown in Fig. 6. This corresponds to −15 dB of roll off across a 500 MHz channel. The capacitors *Cb*1, *Cb*2, and *Cb*3 are identical and small enough to effect the rising slope of the frequency response, producing a sharp cut off in both directions around the gain peak. Transistors M9–M12 are included only for biasing purposes, as the pfet transistors provide a high impedance while introducing fewer parasitics than any resistor within the technology. The actual resistance value must be over 100 kΩ for the shunt conductance to be negligible. At start-

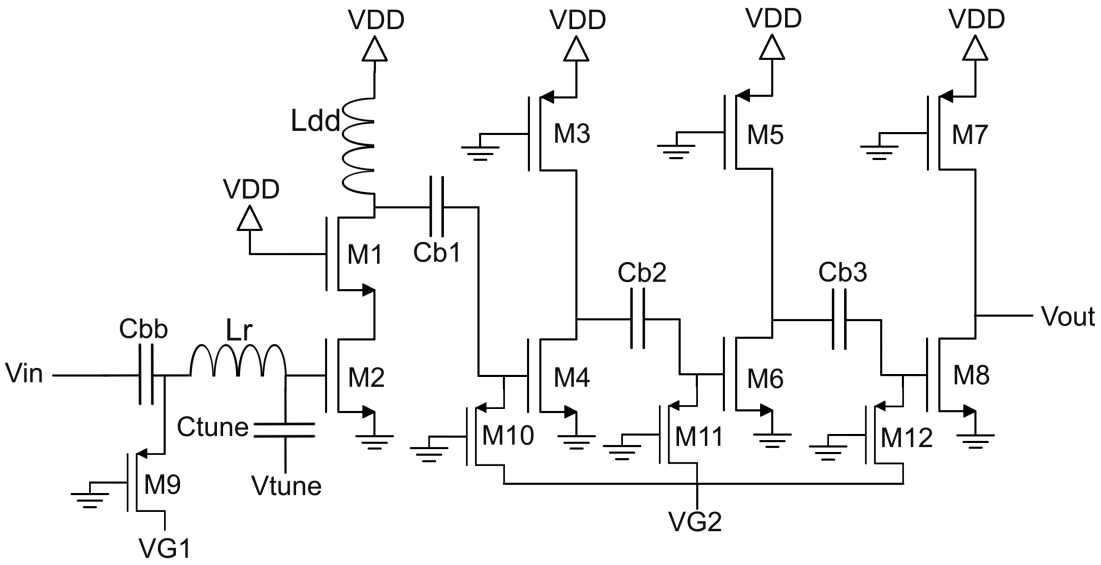

Fig. 5 *Circuit schematic for FM-UWB front-end amplifier*

Table 1 Component parameters for the front end amplifier

Transistor	M1	M2	M4,6,8	M3,5,7	M9–M12
width, μm	25	10	5	1	0.2

Component	C_{tune}	C_{bb}	L_r	L_{dd}	$C_{b1–3}$
value	42–117 fF	10 pF	11 nH	11 nH	200 fF

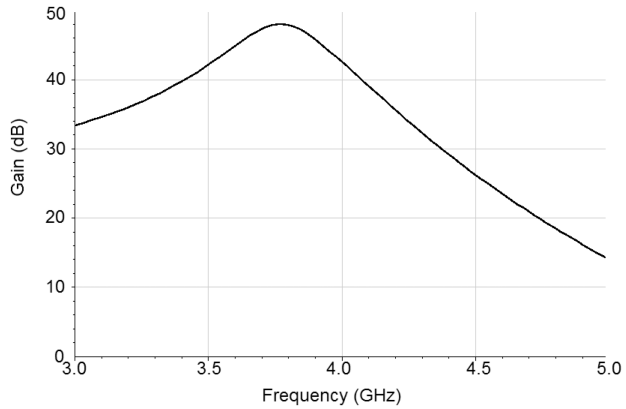

Fig. 6 *Voltage gain for front end RF amplifier for FM-UWB demodulation. The gain peaks at 48 dB after parasitics extraction and has a steep roll off of −140 dB/decade*

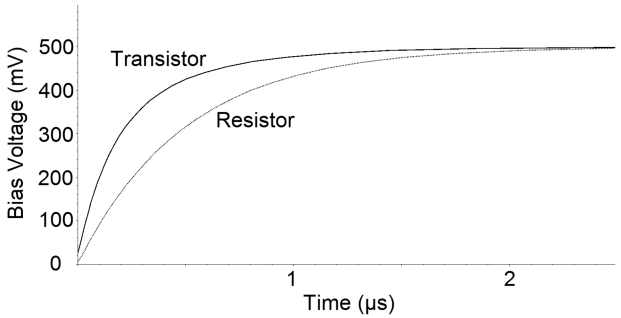

Fig. 7 *Simulation of a biasing resistor implemented using a transistor to enable faster start-up time*

up, the biasing transistors M9–M12 reverse drain/source orientation to enable faster charging than is available using resistors. As the gates of M4, M6, and M8 charge to the DC bias level, the biasing transistors transition to the triode region to provide the high required impedance. A test simulation is set up for a case where a 500 kΩ resistor is in series with a 1 pF capacitor being charged with a bias of 500 mV. At bias, the transistor models 500 kΩ of resistance, but charges two times faster than the resistor, as shown in Fig. 7. The work in [20] is designed to enable duty cycling with 2 dB better sensitivity but consumes ten times the DC power during operation.

2.2 Envelope detector

The front-end amplifier is followed by the envelope detector and IF amplifier in Fig. 8, with component values in Table 2. The output includes and on-chip buffer to connect to an external oscilloscope. The buffer power consumption is not included in the total. The envelope detector at M2 is biased externally at 0.3 V, while the IF amplifier stage includes feedback transistors for self biasing. The signal passes through DC blocking capacitor Cbb while transistor M4 acts as a biasing resistor. Implementing the resistance as a transistor results in the lower capacitive loading compared to available technology resistors, similar to the biasing of the front RF amplifier. Envelope detection is implemented at transistor M2 by applying the input to the gate of M2 and taking the rectified output at the drain, as in [19, 21, 22]. The envelope detector is biased with 10 μA of current while the IF amplifiers consume 5 μA each. At start-up, V_{DD} and V_{ed} can rise quickly, causing biasing transistor M4 to operate in the strong inversion region and quickly transfer charge to the gate of M2. As the gate of M2 charges, the drain–source voltage of M4 approaches zero and the transistor enters the triode region to provide the desired high-pass filter to the gate of M2. C_{bb} and the 10 kΩ resistance of M4 provide a cutoff of 500 MHz. The cutoff should be as high as possible without interfering without degrading the output of the amplifier, or around 2 GHz. However, 200 fF is close to the minimum capacitor available so it cannot be significantly reduced. To reduce the steady-state impedance of M4 would decrease the loading seen by the amplifier and degrade the output signal, so a trade-off is made. Similarly, the transistors M9–M12 in Fig. 5 transition from idle to strong inversion to the triode region for quick start-up. The gates of M5,

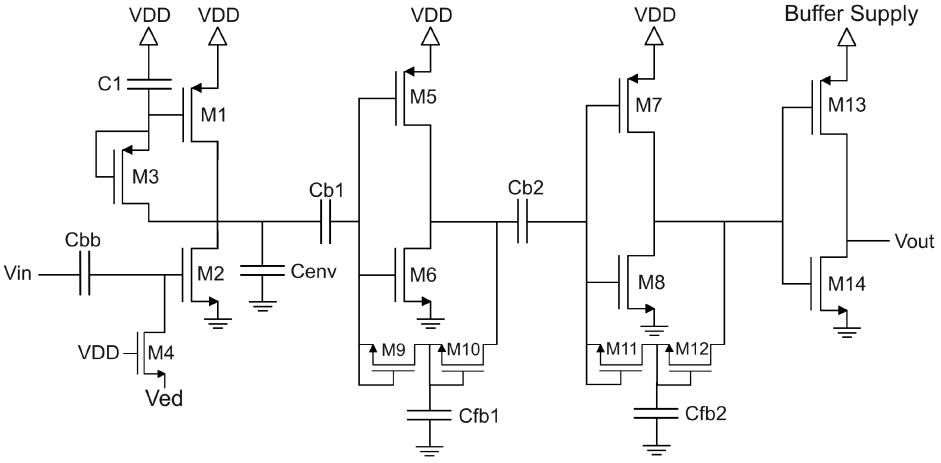

Fig. 8 *Circuit schematic for envelope detector and IF amplifier*

Table 2 Component parameters for the envelope detector and IF amplifier

Transistor	M1	M2	M3, M4	M5, M7
width, μm	1.0	4.0	0.3	3.0

Transistor	M6, M8	M9–M12	M13	M14
width, μm	0.8	0.3	6.0	2.0

Component	C_{bb}, C_1	C_{env}	C_{b1}, C_{b2}	C_{fb1}, C_{fb2}
value	200 fF	2.0 pF	0.5 pF	1.0 pF

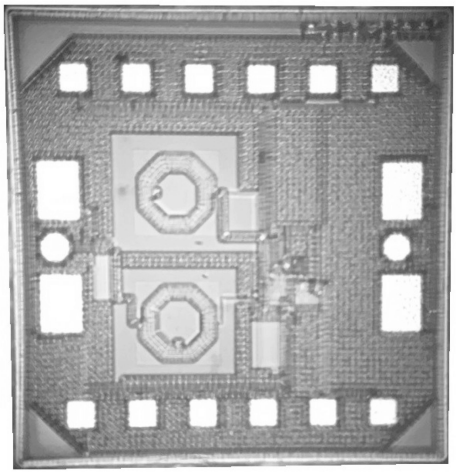

Fig. 9 *Micrograph of the 1 mm × 1 mm fabricated chip. Measurements were performed on the loose die using a microscope and probe station*

M6 are initially at zero, but as V_{DD} rises, the inversion causes the output of M5, M6 to also rise, and current flows through the feedback path M9, M10 to charge the gates. As the gate voltage of M5, M6 approaches the drain voltage, the stage becomes a standard inverter with self-biasing feedback. C_{fb1} and C_{fb2} further reduce the gain of the feedback path, reducing the total loop gain and improving stability during steady-state operation Table 2.

2.3 Sensitivity

In [23] it is found that the sensitivity signal-to-noise ratio (SNR) of an envelope detection circuit can be expressed as

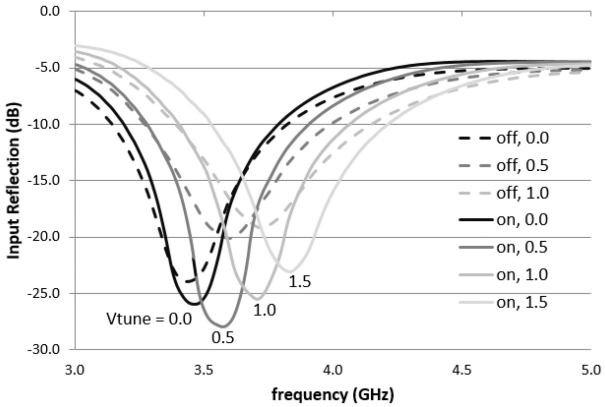

Fig. 10 *Measured tunable input match to the front end of the circuit*

$$\mathrm{SNR} = \frac{i_s^2}{i_n^2} = \frac{V_s^4 C_{env}}{10 k_B T V_T^2} \tag{7}$$

where i_n^2 and v_n^2 are the thermal noise power expressed by current or voltage, respectively, and referred to the receiver input. V_s is the amplitude of the input signal voltage, C_{env} is the enveloped detection capacitor, k_B is Boltzmann's constant, T is the temperature in Kelvin, and V_T is the thermal voltage. V_T is calculated by $V_T = nk_BT/q$, where $1 < n < 2$, and q is the elementary charge.

Rearranging (7) gives

$$V_s = \sqrt[4]{\frac{10 k_B T V_T^2 \mathrm{SNR}}{C_{env}}} \tag{8}$$

Substituting $n = 2$, $k_B = 1.38 \times 10^{-23}$, $q = 1.6 \times 10^{-19}$, $T = 300\,\mathrm{K}$, SNR = 12, and $C_{env} = 2\,\mathrm{pF}$ gives $V_s = 5.1\,\mathrm{mV}$, or −36 dBm across a 50 Ω load. Applying the 48 dB gain at the front end with a simulated 10 dB noise figure brings this to −71 dBm.

3 Measurement results

The circuit was fabricated in the IBM 130-nm CMOS technology and measured on the loose die as shown in Fig. 9. The chip also includes an envelope detector and IF amplifier at the output of the RF amplifier. The front end of the circuit is tunable, as shown in Fig. 10. The applied bias voltage to M2 effects the DC bias across varactor C_{tune}, giving different responses depending on where the receiver is on (solid lines) or off (dashed lines). An on chip buffer is included to couple with external measurement equipment. The power consumption of the on chip buffer is not included in the total.

The setup used to test the chip is shown in Fig. 11. For testing, the control voltages VG1 and VG2 are set to the nominal values of

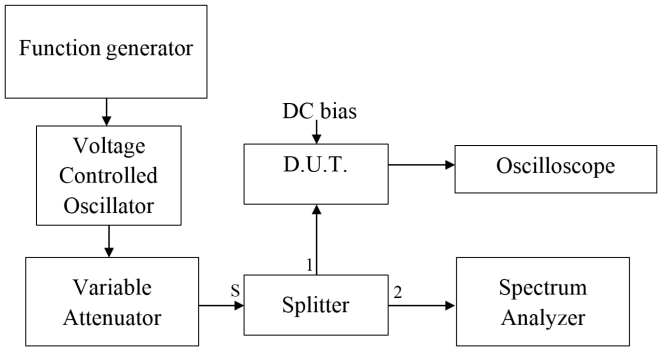

Fig. 11 *Test set up for FM-UWB receiver*

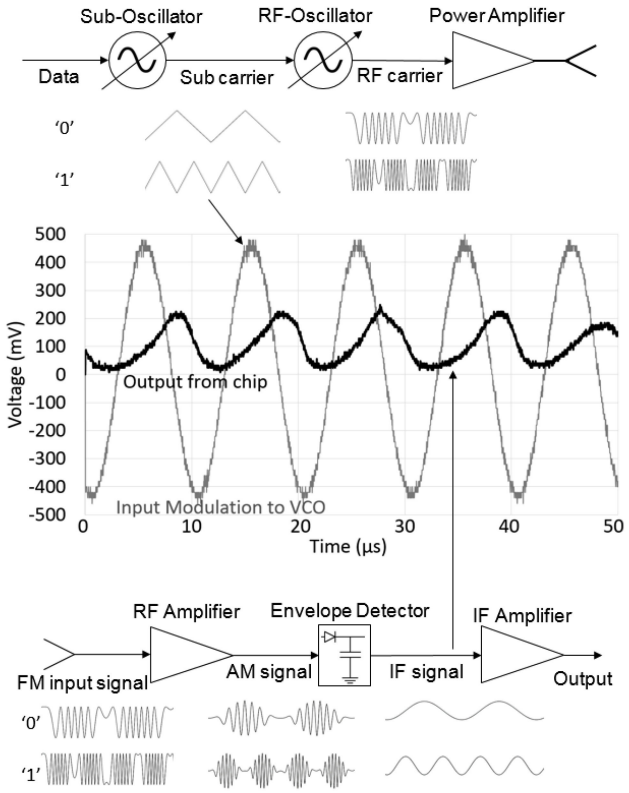

Fig. 12 *Sample of sub-carrier output of chip at 100 kHz with VCO modulation voltage as a reference. The transmitter and receiver block diagrams are included for clarity. The input power level is −68 dBm*

0.55 and 0.5 V, respectively. Modulation was achieved by applying a triangular wave to a 2.5–5.1 GHz Voltage Controlled Oscillator (Synergy DCYS250510). The input signal was split to enable constant monitoring of the signal being applied to the DUT. The triangular wave was tuned to produce a constant power spectral density between 3.2 and 3.7 GHz. When the 3.7–4.2 GHz channel is used, the sensitivity decreased to −66 dBm.

Sensitivity is measured using an oscilloscope. The sensitivity comes from an SNR of 12 W/W where the measured output voltage amplitude is at least 3.5 V/V times higher than the displayed noise fluctuations. The receiver performs for −68 dBm input RF power modulated at 100 kHz while consuming 0.6 mW of power. An example of the recovered analogue sub-carrier is shown in Fig. 12. The measured receiver is 3 dB worse than the simulated value for the output of the envelope detector. The difference is attributed to the $1/f$ noise added by the IF amplifier. If the modulation frequency is increased to 500 kHz, the sensitivity drops to −60 dBm.

The receiver performance is summarised with the state-of-the-art in Table 3. The cost–power product is calculated as

$$\text{cost} = 10\log\left(\frac{(\text{Technology})}{(\text{DCpower})(\text{ICarea})}\right)[\text{dB}] \quad (9)$$

where technology is in nm, DC power is in μW, and IC area is in mm^2.

4 Conclusion

The chip uses only standard analogue functionality without digital calibration to achieve a fast wake up time for duty cycled applications. It shows that high RF gain can be achieved with low power and without the use of positive feedback as in super-regeneration.

5 Acknowledgments

This work was funded, in part, by a grant from NSERC. Sean Whitehall was the recipient of one NSERC Canadian Graduate Scholarship and three Ontario Graduate scholarships. The circuit was simulated and fabricated using services provided by CMC Microsystems.

Table 3 Performance comparison of measured FM-UWB receivers to date

Ref.	This work	[8]	[24]	[12]	[25]	[20]	[16]
technology, nm	130	65	180	90	65	180	65
centre frequency, GHz	3.7	4.0	3.9	4.0	3.75	3.7	4.5
supply voltage, V	1.0	1.0	1.8	1.0	1.0	1.6	1.0
DC power, μW	600	432	13,500	580	3800	7200	2200
sensitivity, dBm	−68	−70	−70	−80	−78	−70	−87
bit rate, kbps	50	100	100	200	100	50	100
IC area, mm^2	0.4	3.0	1.0	0.4	1.5	2.2	0.6
cost–power product, dB	−2.7	−13.0	−18.7	−4.1	−9.4	−19.4	−13.1

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