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Compact 640 μW frequency-modulated ultra-wideband transmitter

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Abstract: This study reports a frequency-modulated ultra-wideband transmitter optimised for low-power consumption. The chip includes a sub-oscillator tunable from 0.1 to 4 MHz, a radio-frequency oscillator tunable from 3.0 to 4.5 GHz, and an output power amplifier with a matching network. Depending on the channel selected, the measured transmitter consumes between 440 and 640 μW of power to produce −14 dBm continuously to a 50 Ω load. Two power supplies are used to reduce the effect of wasted voltage headroom between circuit blocks. Fabrication is done using the International Business Machines Corporation 130 nm complementary metal–oxide–semiconductor technology on a 1 mm × 1 mm loose die, the circuit occupies 0.2 mm^2.

1 Introduction

A frequency-modulated ultra-wideband (FM-UWB) receiver optimised for low-power consumption and fast start-up is described. As demand for radio-frequency (RF) bandwidth increases, the popular spectrum becomes more crowded [1] and motivation to operate outside the 940 and 2400 MHz narrow-band channels is created [2]. Work to specifically improve low-power wireless body area networks (WBANs) is also motivated by a rapidly increasing proportion of the global population that suffers from chronic diseases [3, 4]. With the growing prevalence of the Internet of things, new technologies are also required to meet demand in high traffic *ad hoc* networks [5–8].

Of the proposed UWB communication standards, two are outlined in the IEEE 802.15.6 standard for WBANs. Impulse radio ultra-wideband is suitable for high data rate applications, while FM-UWB is suitable for low complexity, low data rate receivers in crowded environments [9]. FM-UWB also allows multiple sub-channels to be used within the same main channel, increasing spectrum efficiency.

FM-UWB has the output power limited to −41 dbm/MHz, meaning a large channel bandwidth must be used to increase the transmitted power, and therefore the range of communications [2, 10, 11]. Using 500 MHz channels allows −14 dBm of total output power to be transmitted. As shown in Fig. 1*a*, the data is encoded into the frequency of a sub-carrier, which modulates the frequency of the carrier signal. By sweeping the carrier frequency across the entire 500 MHz channel, the output power is kept within the Federal Communications Commission mask [12] while allowing maximum total transmitted power. By encoding data in the sub-carrier, multiple channels can use the same RF frequency band without interference [2, 9, 13, 14]. The modulation is shwon in Fig. 2. A further benefit of FM-UWB is the receiver does not require a phase-locked loop to function [2, 15].

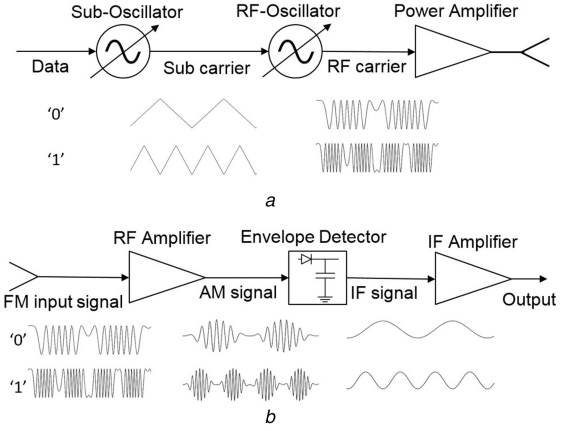

Fig. 1 *Data is encoded into the frequency of a sub-carrier*
(a) FM-UWB transmitter implemented using a sub-carrier oscillator to modulate an RF oscillator and produce a constant envelope output signal, ***(b)*** Block diagram for FM-UWB receiver front end

The receiver portion for FM-UWB is based on an RF amplifier or filter that introduces a slope in the frequency response. The amplifier or filter converts the FM wireless signal to an amplitude-modulated signal from which the sub-carrier is recovered using an envelope detector such as described and utilised in [16] or [17]. State-of-the-art receivers have power consumptions of 432 and 580 μW with sensitivities of −70 and −80 dBm in [9, 14], respectively. The simplified process is illustrated in Fig. 1*b*.

Transmitters have similarly become more efficient, with [14, 18] and this work all providing power consumption below 650 μW.

This work seeks to optimise the RF generation to output chain with the least possible complexity. The chip uses entirely analogue functionality implemented on-chip. Digital calibration could be applied to the bias voltages if desired. The RF oscillator and output power amplifier use separate voltage supplies to reduce the required power by 30%, but increase requirements on the power supply. The power amplifier uses active inductor loading to improve the output flatness when applied to the up-transformed output impedance.

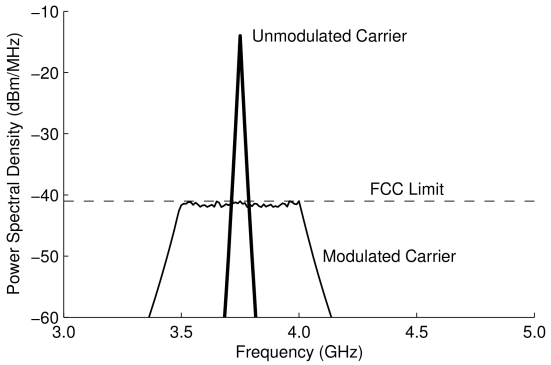

Fig. 2 *Unmodulated signal is swept across a wide bandwidth to produce a constant envelope output*

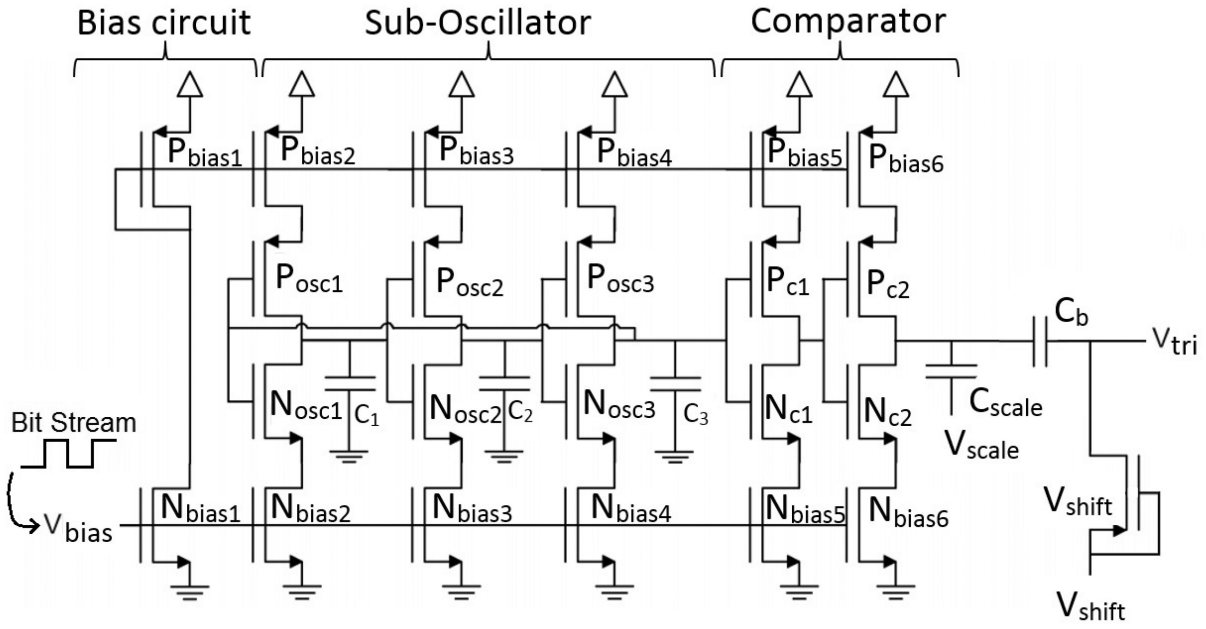

Fig. 3 *Sub-oscillator for FM-UWB transmitter is implemented using a VC CMOS ring oscillator*

Table 1 Component parameters for the sub-oscillator

Transistor	All PMOS transistors	All N-channel MOS transistors
width, μm	0.75	0.3

Component	$C_{1,\,2,\,3}$	C_{scale}	C_{b}
value, pF	0.1	0.3–1.6	1.0

Section 2 of this paper is the circuit design, which outlines in order of the design of the sub-oscillator, RF oscillator, and output power amplifier. The circuit design is followed by the measurement results in Section 3, which includes discussion and comparison with state of the art. Section 4 is the conclusion, then acknowledgements are made in Section 5.

2 Circuit design

2.1 Low-frequency sub-oscillator

The designed and simulated sub-oscillator is shown in Fig. 3 with component values summarised in Table 1. The design is a basic voltage-controlled (VC) three-stage ring oscillator followed by a comparator and integrating capacitor. The identical capacitors C_1, C_2, and C_3 dominate the transistor parasitics and reduce the oscillation frequency to a 0.1–4.0 MHz range. The output triangular wave is tunable across frequency, amplitude, and DC average voltage. V_{bias} adjusts the frequency of oscillation, while control voltage V_{tune} adjusts varactor C_{tune} to control the output amplitude of the triangular wave V_{tri}. The DC level of V_{tri} is decoupled with a DC blocking capacitor C_{b} before connection to the RF oscillator with an external bias voltage. The bit stream is applied directly to the port V_{bias}, which controls the output frequency of the sub-oscillator. Starting from the basic capacitor equation

$$i = C\frac{\mathrm{d}V}{\mathrm{d}t} \tag{1}$$

and rearranging to represent the output of Fig. 3 gives

$$\Delta V = \frac{1}{C_{\text{scale}}}\int_0^{T_{\text{sub}}/2} I_{\text{out}}\,\mathrm{d}t \tag{2}$$

where ΔV is the voltage swing of V_{tri} on effectively either side of C_{b}, T_{sub} is the period of oscillation for the sub-oscillator, and I_{out} is the output current into the capacitor C_{scale}. The integral is evaluated to

$$\Delta V = \frac{1}{C_{\text{scale}}}\frac{T}{2}I_{\text{out, avg}} = \frac{I_{\text{out, avg}}}{2C_{\text{scale}}f_{\text{sub}}} \tag{3}$$

where f_{sub} is the frequency of oscillation for the sub-oscillator and $I_{\text{out, avg}}$ is the time average current delivered into the capacitor. As the capacitors C_1, C_2, and C_3 are large enough to dominate the transistor parasitics, the oscillation frequency is approximated by

$$f_{\text{sub}} \propto \frac{I_{\text{branch, avg}}}{V_{\text{osc}}C_{1,\,2,\,3}} \tag{4}$$

where V_{osc} is the amplitude of oscillation, $C_{1,\,2,\,3}$ is any of the identical capacitors C_1, C_2, or C_3 and $I_{\text{branch, avg}}$ is the average current from any of the three branches flowing into the respective capacitors. Combining (3) and (4) gives

$$\Delta V \propto \frac{V_{\text{osc}}C_{1,\,2,\,3}}{C_{\text{scale}}}\frac{I_{\text{branch, avg}}}{I_{\text{out, avg}}}. \tag{5}$$

$I_{\text{branch, avg}}$ and $I_{\text{out, avg}}$ are controlled by identically sized and biased current source transistors, so they can be expected to change at same rate, leaving the output voltage swing independent of the frequency of oscillation. If the output voltage swing is not dependent on the frequency of oscillation and the capacitor C_{scale} does not need to be re-adjusted as the sub-oscillation frequency changes. The entire sub-oscillator circuit consumes 5–10 μW of power, which is only a few percentage points of the total power consumption and thus extra techniques to reduce the power are not required.

2.2 RF oscillator

Using an inductor–capacitor (LC)-tank oscillator is considered for the VC oscillator (VCO). Test VCO simulations consuming 200 μW are set up as an LC tank with variable capacitors (varactors), LC tank with switched capacitors, and a ring VCO with current sources. The results are summarised in Table 2.

For a multi-channel system at 4.0 GHz, 25% tuning range (TR) with continuous tuning is required. To sustain three channels between 3 and 4.5 GHz, (1.5/3.75) = 40% TR is required. The ring

Table 2 Comparison of implementation options for RF-VCO

Metric	LC tank with varactors	LC tank with switched capacitors	Ring VCO with current sources
tuning range, %	18	36	50
power, μW	200	200	200
continuous tuning	yes	no	yes

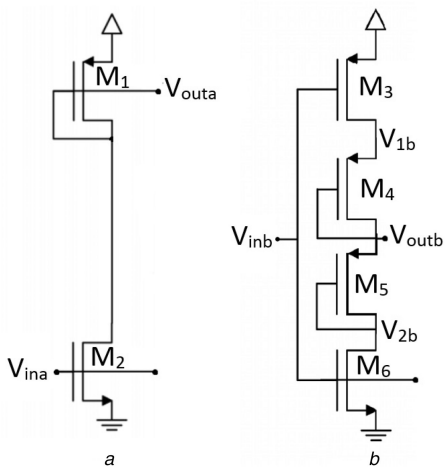

Fig. 4 *New bias circuit to reduce power consumption while improving functionality*
(a) Traditional circuit bias circuit, ***(b)*** Improved bias circuit for low power operation

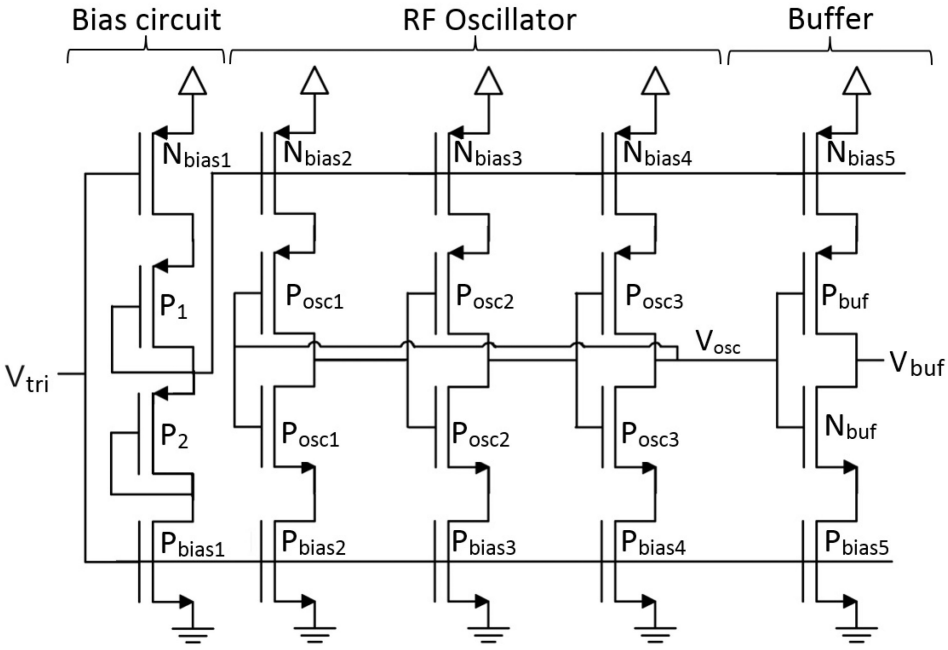

Fig. 5 *RF oscillator for FM-UWB transmitter. All bias transistors are sized twice as large as the oscillator transistors, to reduce the wasted voltage headroom*

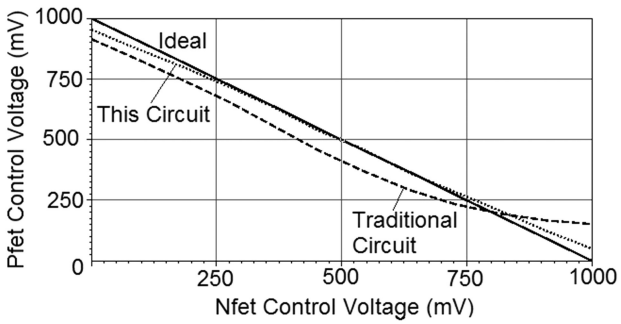

Fig. 6 *Transfer function for the modified biasing circuit to RF ring oscillator. A 1 V supply is used for demonstration*

VCO is the only architecture that meets these requirements. While the phase noise of the ring VCO is substantially worst, −70 versus −100 dBc/Hz at 1 MHz offset, FM-UWB systems can tolerate up to −60 dBc/Hz [2, 10, 14]. The ring VCO has the added advantage of requiring less than a tenth of the die area by eliminating the need for an inductor.

The RF oscillator is also a VC three-stage ring oscillator with some modifications. A different circuit is used to generate the bias voltage of the P-channel metal–oxide–semiconductor (PMOS) transistors as in Fig. 4. The full oscillator schematic is shown in Fig. 5 with component values in Table 3. The biasing transistors M_4 and M_5 are added to choke the current of the bias circuit to negligible levels while still providing bias functionality superior to a two transistor circuit, as shwon in Fig. 6. This reduces simulated oscillator power consumption by 25–40% depending on operating point.

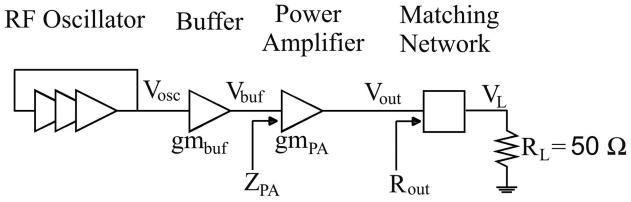

Fig. 7 *Block diagram to optimise the RF path of the transmitter*

To analyse the circuit in Fig. 4*b* in the sub-threshold regime, consider the case where the Nfet control voltage V_{inb} is a low value. In this case, M_3 can be considered 'ON' and the voltage V_{outb} is equal to V_{DD}. The current through each transistor M_4, M_5, and M_6 is approximated by the sub-threshold equation

$$I_{\text{DD}} \simeq I_{\text{d0}} e^{V_{\text{fb}}/V_{\text{T}}} \tag{6}$$

where $V_{\text{T}} = nkT/q$ with $1 < n < 2$, k is Boltzmann's constant, T is the temperature in Kelvin, q is the elementary charge, and V_{fb} is the forward-bias voltage ($V_{1\text{b}} - V_{\text{outb}}$) for M_4, ($V_{\text{outb}} - V_{2\text{b}}$) for M_5, and ($V_{\text{inb}} - 0$) for M_6. The transistors M_{4-6} are sized so the voltage drop across each is approximately the same

$$V_{1\text{b}} - V_{\text{outb}} = V_{\text{DD}} - V_{\text{outb}} = V_{\text{outb}} - V_{2\text{b}} = V_{\text{inb}}\,. \tag{7}$$

The important conclusion is $V_{\text{inb}} = V_{\text{DD}} - V_{\text{outb}}$, giving a linear negative relationship between the input and output. For the case when the Nfet control voltage V_{inb} is high, a similar analysis is used. The bottom transistor M_6 is 'ON' while

$$V_{\text{DD}} - V_{\text{inb}} = V_{1\text{b}} - V_{\text{outb}} = V_{\text{outb}} - V_{2\text{b}} = V_{\text{outb}}\,. \tag{8}$$

or simply $V_{\text{outb}} = V_{\text{DD}} - V_{\text{inb}}$ as before. The final case comes when the Nfet control voltage V_{in} is in a middle range, able to turn on both M_3 and M_6, whereas M_4 and M_5 remain in the sub-threshold region. For $V_{\text{in2}} = V_{\text{DD}}/2$, the top and bottom halves of the circuit are identical and result in $V_{\text{out2}} = V_{\text{in2}} = V_{\text{DD}}/2$. The Pfets M_4 and M_5 apply negative feedback to keep the response linear until V_{in} reaches either of the two previous conditions, yielding $V_{\text{out2}} = V_{\text{DD}} - V_{\text{in2}}$ for all ranges of V_{in}. For the circuit to function in the sub-threshold regime under higher voltages, M_4 and M_5 can be each replaced with two transistors without changing functionality.

The frequency of oscillation is increased using forward body bias (not shown in schematic) to reduce the threshold voltage of all transistors.

The entire RF chain of the transmitter is summarised in the block diagram of Fig. 7.

The output power is given by

$$P_{\text{out}} = \frac{V_{\text{out}}^2}{2R_{\text{out}}} \tag{9}$$

where V_{out} is the amplitude of the output voltage and R_{out} is the output resistance. Applying the gain of the output amplifier $V_{\text{out}}/V_{\text{rf}} = gm_{\text{PA}} \times R_{\text{out}}$

$$P_{\text{out}} = \frac{(V_{\text{buf}} gm_{\text{PA}} R_{\text{out}})^2}{2R_{\text{out}}} \tag{10}$$

where V_{buf} is the amplitude of V_{buf} in Fig. 5 and gm_{PA} is the transconductance of the output amplifier in Fig. 8*a*. Taking the signal from the oscillator using the gain of the buffer stage of $V_{\text{rf}}/V_{\text{osc}} = gm_{\text{buf}} \times Z_{\text{in}_{\text{PA}}}$

$$P_{\text{out}} = \frac{(V_{\text{osc}} gm_{\text{PA}} gm_{\text{buf}} Z_{\text{PA}})^2 R_{\text{out}}}{2} \tag{11}$$

Table 3 Component parameters for the RF oscillator

Transistor	$P_{\text{bias1–5}}$, P_1, P_2	$P_{\text{osc1–3}}$, P_{buf}
width, μm	2.0	1.0

Transistor	$N_{\text{bias1–5}}$	$N_{\text{osc1–3}}$, P_{buf}
width, μm	0.8	0.4

where V_{rf} is the amplitude of the oscillation signal produced by $P_{\text{osc1-3}}$ and $N_{\text{osc1-3}}$ and gm_{PA} is the transconductance of the buffer stage P_{buf} and N_{buf}. Considering the amplitude of oscillation V_{osc} is approximately $(1/2)V_{\text{DD}_{\text{osc}}}$ gives

$$P_{\text{out}} = \frac{(V_{\text{DD}} gm_{\text{PA}} gm_{\text{buf}} Z_{\text{PA}})^2 R_{\text{out}}}{8} \tag{12}$$

where V_{DD} is the DC supply voltage to the oscillator, which yields some useful observations. First is that the output power increases with the square of the oscillator supply voltage, while DC power increases linearly, so a higher supply voltage will yield higher efficiency while the transistors operate within a reasonable tolerance. The power increases with higher impedance to the output amplifier, so using only an Nfet load instead of a Pfet is beneficial to take advantage of the higher transconductance/load ratio. The amplifier requires a large current to drive the output load, however, so the signal is still attenuated by 10 dB after the buffer. While (12) suggests that the sizing of the power amplifier transistor could be reduced while keeping the $gm_{\text{PA}} \times Z_{\text{PA}}$ product constant, the Z_{PA} includes parasitics that do not scale with the reduced transistor size. That the output power increases directly with Rout shows the need for a matching network that transforms the 50 Ω load as high as possible. The power supply of the output amplifier does not contribute to a high output power beyond the effect on gm_{PA}, so separate power supplies of 1.4 and 0.7 V are used for the oscillators and amplifier, respectively, while an additional supply voltage is not.

The output efficiency can be expressed as

$$\eta_{\text{out}} = \frac{P_{\text{out}}}{V_{\text{DD}} I_{\text{osc}} + (1/2) V_{\text{DD}} I_{\text{PA}}} \tag{13}$$

where I_{osc} is the total current of the oscillator and buffer equal to roughly four times the average DC current of any branch, I_{PA} is the average DC current of the power amplifier, and $(1/2)V_{\text{DD}}$ is the supply voltage of the power amplifier. Combining (12) and (13) gives

$$\eta_{\text{out}} = V_{\text{DD}} \frac{(gm_{\text{PA}} gm_{\text{buf}} Z_{\text{PA}})^2}{I_{\text{osc}} + (1/2) I_{\text{PA}}} \frac{R_{\text{out}}}{8}\,. \tag{14}$$

At steady state, the oscillator will operate under the conditions

$$gm_{\text{osc}} Z_{\text{osc}} = gm_{\text{buf}} Z_{\text{osc}} = 1 \tag{15}$$

or

$$gm_{\text{buf}} = \frac{1}{Z_{\text{osc}}} \tag{16}$$

where gm_{osc} and Z_{osc} are the transconductance and impedance of and individual branch of the oscillator. Combining with (14) gives

$$\eta_{\text{out}} = V_{\text{DD}} \frac{(gm_{\text{PA}} (Z_{\text{PA}}/Z_{\text{osc}}))^2}{I_{\text{osc}} + (1/2) I_{\text{PA}}} \frac{R_{\text{out}}}{8}\,. \tag{17}$$

If gm_{PA} and Z_{PA} are linearly related, then any size of output amplifier would be sufficient. Unfortunately, Z_{PA} has a parasitic

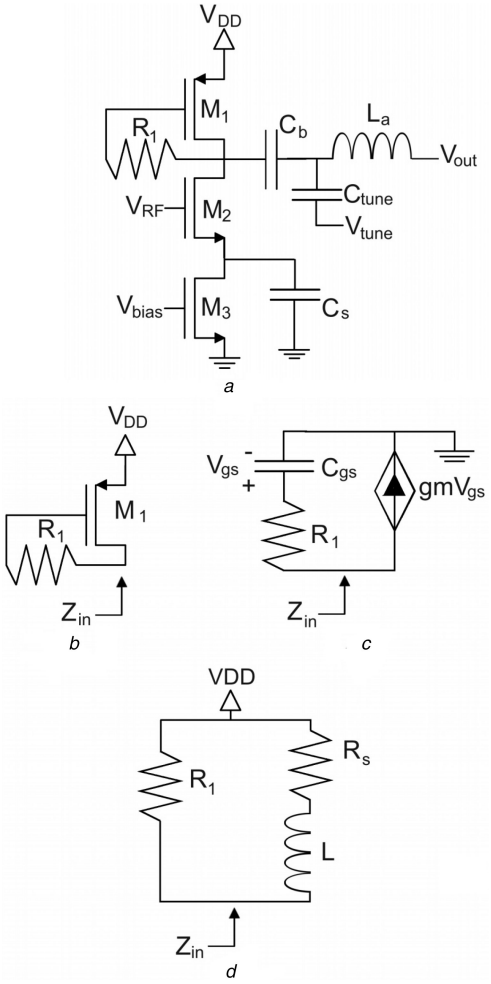

Fig. 8 *Transconductance of the output amplifier*
(a) Power amplifier for FM-UWB transmitter, ***(b)*** Transistor M_1 and resistor R_1 for an active inductor circuit, ***(c)*** Small signal equivalent circuit for active inductor, ***(d)*** Equivalent circuit for active inductor

Table 4 Component parameters for the power amplifier

Transistor	M_1	M_2	M_3
width, μm	10	4	8

Component	R_1	C_s and C_b	C_{tune}	L_a
value	10 kΩ	10 pF	60–250 fF	4 nH

component from the layout which increases the minimum sizing of the power amplifier. It can be shown that without layout parasitics considered, extra stages do not contribute to the gain because every linear increase in transconductance and capacitive loading with transistor width simply cancel each other out. With layout parasitics considered, any extra stages add to these parasitics and reduce the gain, motivating as few stages as possible in the RF chain.

The RF oscillator circuit is designed to consumer around 200 μA of power and the simulated phase noise is −70 dBc/Hz at 1 MHz offset when running at 4 GHz. This is well within the −60 dBc/Hz for proper operation recommended in [2, 10, 14, 19]. The total power budget includes 250 μA for the power amplifier and comes to <500 μA.

2.3 Power amplifier

The power amplifier for the circuit is shown in Fig. 8*a*. The power amplifier is meant to buffer the oscillator output to a 50 Ω load. To reduce loading on the buffer, the oscillator voltage V_{buf} is only connected to a transistor M_2 of the output power amplifier. Transistor M_3 is used for biasing, while M_1 and R_1 for active inductor loading, which is described in [20]. The small signal representation of the active inductor loading in Fig. 8*b* is shown in Fig. 8*c*. Several parasitics such as C_{ds}, g_O, and r_O are omitted from the representation. It is shown in [20] how the small signal model can be transformed to the single-ended inductor in Fig. 8*d* with the parameters

$$L = \frac{R_1 C_{gs}}{gm - (1/R_1)} \tag{18}$$

and

$$R_s = \frac{1}{gm - (1/R_1)}. \tag{19}$$

The active inductor loading had the advantage of low DC gain with the gain peaking at high frequencies, making the amplifier output insensitive to changes in DC bias while maintaining performance at high frequencies [20]. The low DC gain is important because the output amplifier is biased at M_2 directly from the buffer, which could have fluctuations in DC bias that are not entirely eliminated by the current source of M_3.

Capacitor C_s prevents the biasing transistor M_3 from affecting the gain of the amplifier. Inductor L_a and capacitor C_{tune} form a passive transformer that increases the 50 Ω load up to 500 Ω, increasing the amplitude of the output voltage. The Amp is designed to deliver the required −14 dBm of power to a 50 Ω load at V_{out}. The amplifier also provides −40 dm of simulated reverse isolation from the output to the RF-VCO. All component values are shown in Table 4.

3 Measurement results

The circuit is fabricated in the International Business Machines Corporation 130 nm complementary MOS (CMOS) technology and measured on the loose die as shown in Fig. 9. The 130 nm technology is chosen as a tradeoff of device frequency range and fabrication cost. The output of the circuit is tunable, as shown in Fig. 10. The simulated output match values provide the best match across the lower 3.1–3.6 GHz band, while the measured values are wider with superior performance at the top end of the bandwidth. The difference is attributed to increased losses within the inductor compared with the simulated model. The wider matched bandwidth at each tuning voltage suggests the quality factor of the output inductor is less than the simulation value.

An example measured output spectrum centred at 3.75 GHz is shown in Fig. 11. When transmitting at the 500 MHz channel centred at 3.25 GHz, the power consumption drops to 440 μW, but increases to 640 μW when using the channel centred at 4.25 GHz. The added power comes from the increased current consumption of the RF oscillator when producing higher frequencies, as shown in Fig. 12*a*.

The measured oscillation frequency and oscillator supply current are shown in Figs. 12 and *b*, respectively, with the 1.4 V supply voltage varied to 1.3 and 1.5 V. It should be noted that the increase in supply voltage of 1.3–1.5 (15%) leads to an increase in frequency of only 5%, but a supply current increase of 33%, and therefore a power increase of 50%. This shows the frequency of power efficiency does deteriorate for higher supply voltages above a certain threshold, limiting its usefulness if the oscillator and amplifier have the same supply voltage. However, the increased current has the added utility of reducing sensitivity to loading and also transfers directly to an increase in the transmitted output power.

The performance of the FM-UWB transmitter is compared with the state-of-the-art designs in Table 5. The power is reported as a range to cover the different transmission channels. As high frequencies require the oscillator to consume more power, the channels have increasing power consumption with frequency. While the cited works do not expand on the power required for

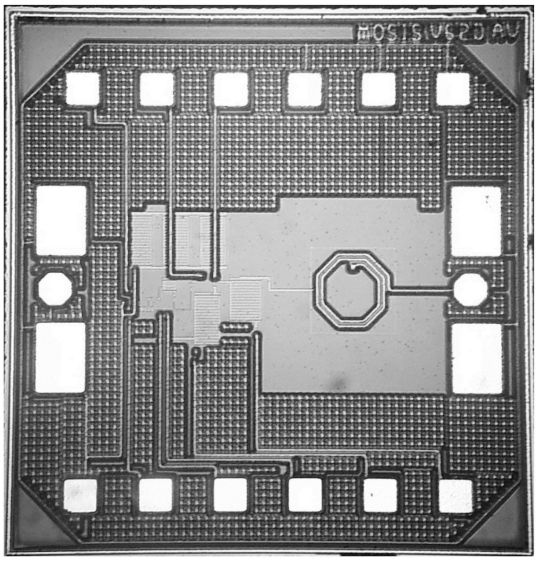

Fig. 9 *Micrograph of the 1 mm × 1 mm fabricated chip. Measurements are performed on the loose die using a microscope and probe station*

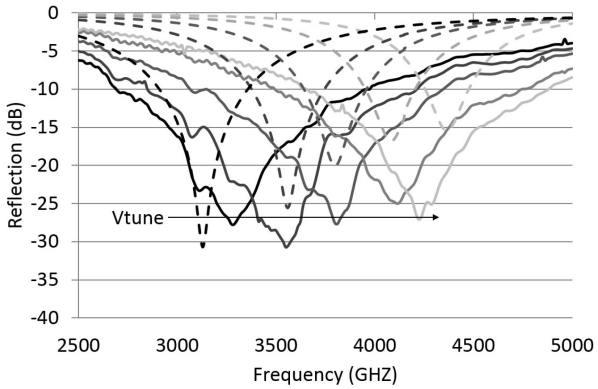

Fig. 10 *Tunable output match to the front end of the circuit. Dashed lines are simulation while measured results are in solid*

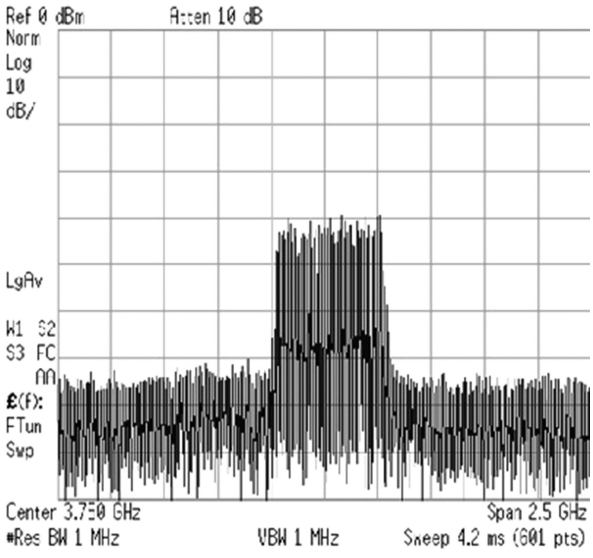

Fig. 11 *Measured output spectrum of the transmitter*

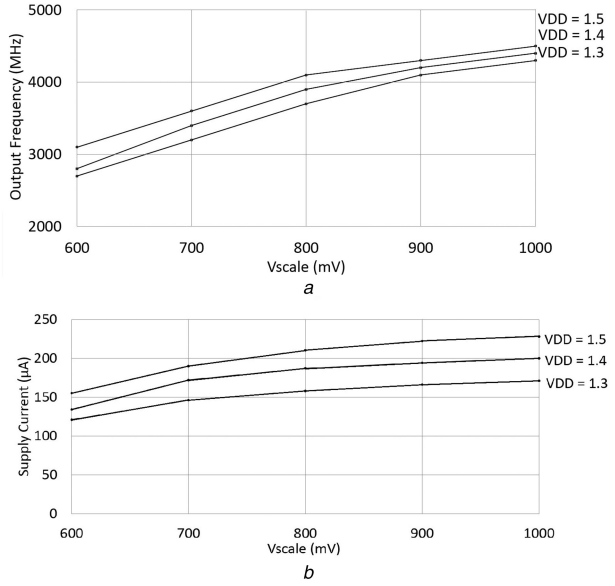

Fig. 12 *Added power comes from the increased current consumption of the RF oscillator*

(a) Oscillation frequency as a function of the tuning voltage V_{tune} across different supply voltages, ***(b)*** Oscillator current as a function of the tuning voltage V_{tune} across different supply voltages

different channels, Saputra and Long [14] do specify changing DC power with changes in measured output power. Specifically, 720 μW of DC power is required to produce −10.1 dBm of output RF power, with 630 μW of DC power producing −12.8 dBm [14]. The designs are compared using a figure of merit (FOM) calculated in decibels as

$$\text{FOM} = 10\log\left(\frac{(P_{\text{out}})(\text{BR})(\text{tech})(\text{TR})}{(P_{\text{DC}})(\text{IC}_{\text{area}})}\right) \tag{20}$$

Table 5 Performance comparison of measured FM-UWB transmitters to date

Reference	This work	[14]	[21]	[22]	[23]	[10]
technology, nm	130	90	65	180	180	65
frequency range, GHz	3–4.5	3–5	3.5–4	3.7	3.5–4.5	3–5
supply voltage, V	1.4, 0.7	1.0	1.0	1.6	1.5	1.0
DC power, μW	440–640	630	1140	8700	1000	900
output power, dBm	−14	−10.1	−14	−13.7	−14	−10.2
BR, kbps	200	200	750	50	2000	100
IC area, mm^2	0.2	0.6	0.2	2.2	1.44	0.4
FOM, dB	5.1	3.7	4.5	−26.0	4.1	−0.4

where BR is the bit rate in kbps, tech is the technology device length in nm, TR is the tuning range calculated by total frequency range divided by centre frequency, P_{DC} is the power consumption in μW, integrated circuit area is in mm^2, and P_{out} is the transmitted output power in mW.

4 Conclusion

An FM-UWB transmitter is fabricated in a common CMOS 130 nm process. The circuit analysis showed that the total power of the circuit is reduced by using separate power supplies to different sections of the circuit. By reducing the RF chain to the minimum required stages, parasitic capacitance, and power consumption are reduced.

5 Acknowledgments

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