

A Tunable 300-800MHz RF-Sampling Receiver Achieving 60dB Harmonic Rejection and 0.8dB Minimum NF in 65nm CMOS

Z. Ru, E. Klumperink, C. Saavedra*, B. Nauta

University of Twente, Netherlands

*Queen's University, Canada

Abstract — A 300-800MHz CMOS radio receiver aiming at software-defined radio is proposed. It exploits an LNA preceded by a tunable LC filter with one external coil to achieve voltage amplification for low NF and low-pass filtering to improve the 3rd and 5th harmonic rejection of an RF-sampling receiver to >60dB. The balun-LNA provides partial IM3 compensation, to drive a wideband sampling downconverter. The measured gain is 22-28dB while NF ranges from 0.8-4.3dB. The core consumes 6mW and clock takes 12mW.

Index Terms — CMOS, LC filter, tunable filter, LNA, downconverter, sampling, receiver, sampling receiver, matching, nonlinearity, distortion, harmonic rejection, software-defined radio, cognitive radio.

I. INTRODUCTION

In the last few years, radio receivers based on the RF-sampling instead of mixing found industrial applications [1] [2] [3]. Sampling early at RF allows more discrete-time and digital signal processing, which can have advantages with respect to the compatibility with digital CMOS technology [1] [2] and SoC integration [3]. However, most published RF-sampling receivers are narrowband, and compared to RF-mixing receivers, a number of extra challenges exist to apply RF-sampling to wideband software-defined radio (SDR) receivers [4].

For a wideband receiver, limiting the effect of sampling aliases of noise and interference is vital. RF SAW filters can help but compromise the flexibility of a SDR receiver and are also bulky and costly. Recently, a flexible and wideband harmonic rejection (HR) technique has been proposed for RF-sampling receivers, via a discrete-time (DT) mixing architecture [5]. However, the achieved 3rd and 5th HR ratio (average 40dB and $\sigma=5$ dB $\Rightarrow 3\sigma$ limits as low as 25dB) is significantly degraded by mismatch, and the poor NF (>12dB) asks for more pre-amplification.

This paper proposes a technique to improve the 3rd and 5th HR by more than 30dB and 40dB respectively, while also reducing the noise figure dramatically. It exploits an LC filter which provides voltage amplification and pre-filtering followed by a wideband low noise voltage amplifier and balun. We aim at a receiver covering 300MHz to 800MHz (DVB-H band and TV white-space bands for cognitive radio) in two sub-bands. This paper discusses the design of the receiver with an emphasis on the filter/LNA part while the sampling downconverter was described in [5].

II. RF-SAMPLING RECEIVER ARCHITECTURE

Fig. 1 shows the receiver architecture. Two input signal paths are used for two different sub-bands. These can be connected to different antennae, as shown, but also to a single antenna which can cover the full bandwidth. The antennae deliver signals to two inductors followed by a receiver chip consisting of two switchable capacitor banks, a single-input differential-output (balun) LNA with two selectable input stages in parallel, an RF-sampling downconverter (RFSD) with 3rd and 5th HR driven by a frequency-divider.

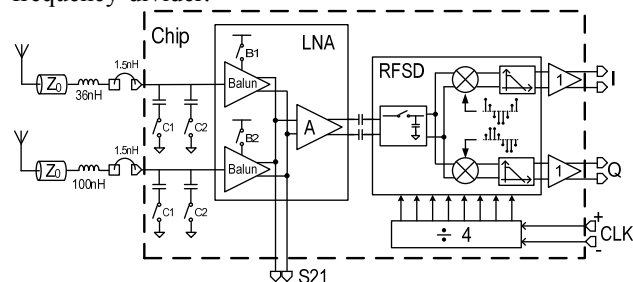


Fig. 1. The multi-band RF-sampling receiver

III. DIGITALLY-CONTROLLED LC Filter

As well known, a series inductor and a capacitor to ground define a 2nd order low-pass filter. Since inductors are not easily tunable and varactors introduce nonlinearity, we aim to exploit MOS-switches and linear capacitors for tuning, which can be digitally controlled, as shown in Fig. 2. Such an LC filter *does not* provide impedance matching, but *does give useful voltage pre-gain* around the resonance frequency. Moreover, the low-pass transfer function provides significant attenuation for RF signals at multiples of the LO-frequency, hence improving HR of RFSD. The voltage pre-gain can boost the wanted signal and the improved HR reduces noise and interference aliasing. *Both features improve the NF of a wideband sampling receiver.* For capacitor values in the order of a few pF, suitable inductor values for the 300-800MHz band are in the order of 10-100nH. Such values are not easily integrated and even if doable the Q is low. On-board inductors can be small, e.g. SMD, and with higher-Q, and also they are relatively low cost compared to, for instance, SAW filters, while still allowing for flexibility via changing the on-chip C. If the receiver has a single-

ended RF input, only one external inductor is needed for every sub-band.

Fig.2 shows the schematic of the 2nd order tunable LC filter. At the resonance frequency $\omega_0=1/\sqrt{LC}$, the voltage magnitude on the capacitor can be written as

$$|V_{out}| = \frac{|V_{src}|}{R_{src}} \cdot \frac{1}{\omega_0 C} = \frac{\sqrt{L/C}}{R_{src}} \cdot |V_{src}| = Q \cdot |V_{src}| = 2Q \cdot |V_{match}| \quad (1)$$

where the actual source voltage $|V_{src}|$ is twice as large as the voltage $|V_{match}|$ in case of impedance matching (see further below). For a sufficiently high L/C ratio, $Q=\sqrt{L/C}/R$ can be >0.5 and thus this filter can realize “passive” voltage gain around the resonance peak f_0 . This improves the receiver sensitivity, without adding noise and power consumption. This property is favorable compared to SAW filters, which introduce significant loss. The gain is well-defined if the antenna impedance (R_{src}) is well-defined. If not, additional measures may be needed to adaptively control the Q and resonance frequency of the filter. Switching the capacitor to tune the filter to another frequency also changes its gain, but this gain variation can be acceptable (within $\pm 3\text{dB}$) if we keep the frequency tuning range $<50\%$, i.e. $0.75f_0$ to $1.25f_0$.

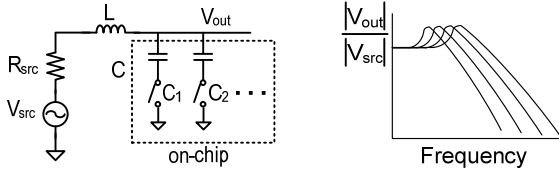


Fig. 2. A 2nd-order tunable LC filter with transfer function

At resonance, its input impedance is 0 (short) instead of R_{src} . This is not necessarily to be a problem if no RF filter designed for matching with R_{src} is used. Note that for input matching there is maximum power transfer, but it degrades the voltage by half, i.e. $V_{match}=V_{src}/2$ as shown in (1). For voltage sensing devices such as a MOSFET at $f \ll f_T$, the maximum voltage transfer is more of interest, and an unmatched input may have advantages, e.g. lower noise, lower power consumption, and higher-Q (no extra R from the matching device). Receivers without input matching have been proposed before, e.g. in [6] [7].

Since inductors conduct DC, the attenuation on the low-frequency side is limited. But to suppress LO harmonics it is enough to have the roll-off on the high-frequency side. A simple 2nd-order LC filter does not show a characteristic as sharp as most SAW filters, so the suppression of out-of-band interference is less. Whether this is acceptable depends on the application, the antenna characteristic and the linearity of the front-end.

Fig. 3 shows the schematic of the implemented LC filter together with the LNA. Two inductors, 36nH for high-band and 100nH for low-band, with two capacitors ($C_1=0.5\text{pF}$, $C_2=1.2\text{pF}$) for each inductor, are included to demonstrate the multi-band function. Which signal path in

use is selected by enabling one of the LNAs (B_1 , B_2). In practice, the parasitic capacitance, e.g. from LNA, ESD, pad, and PCB, will limit the maximum achievable Q.

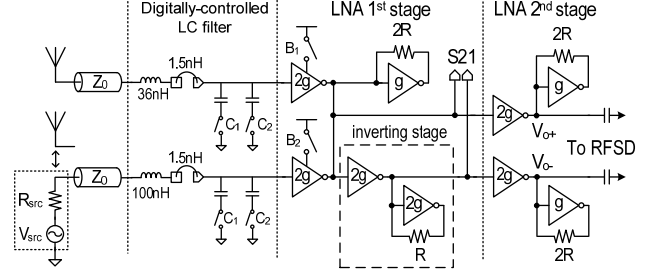


Fig. 3. Implemented LC filter and LNA

IV. BALUN-LNA BASED ON INVERTERS

As shown in Fig. 3, the balun-LNA is built using inverters as transconductors with good g_m/I_d (current reuse) while tolerating large voltage swings. To understand its basic functionality, consider all feedback resistors as shorts, realizing an impedance $1/g$ or $1/(2g)$ where g is the unit transconductance in use. Driven by a transconductor of $2g$, an inverting gain is realized. The gain is -2 in all cases except for the “inverting stage” (gain= -1). Thus the 1st stage is a balun with 6dB gain from the input to each of the differential outputs (single-to-differential gain= 4), and the 2nd stage is a pseudo differential amplifier with another 6dB gain. Due to the additional stage used for inverting (marked in box) in the V_{o-} path, extra delay exists and the balun performance can degrade with higher frequency. Simulations show 0.05dB amplitude error and 2.8° phase error at 300MHz, while 0.02dB and 7.5° at 800MHz. But this could be compensated by adding a capacitor with appropriate value at the V_{o+} node to balance two paths. Please note all inverters are self-biased in practice.

The passive LC pre-gain improves receiver NF, but will also degrade linearity. The aim of the feedback resistors is to mitigate this effect by partially compensating the 3rd-order distortion. To understand the principle, consider the simple case with two equal inverters for gain= -1 (Fig. 4), and only include the linear term and the 3rd-order term. Modeling the transconductor as a nonlinear V-I converter with no v_{ds} dependence, i.e. only g_{m1} and g_{m3} terms, the nonlinearity in the V-I conversion and the I-V conversion cancel each other (inverse functions) whatever the value of the feedback resistor (can be a short). However, in modern CMOS technology the output impedance and the $v_{gs}v_{ds}$ cross term cannot be neglected anymore [8]. If we model these effects via equation (2) it still appears possible to achieve 3rd-order cancellation.

The exact nonlinear math is somewhat involved, but we will try to make this plausible as follows. Assume a negligible input current of the transconductor, then in Fig.4 i_o is equal to i_a , based on Kirchhoff Current Law.

For a linear amplifier, we want $v_o = -v_{in}$, without any 3rd order terms. Putting this condition in (2), and equating the equations shows that $v_a \approx -v_o$ renders a solution. This can be realized by choosing $R=1/g$, so that $g \cdot R=1$. Please note that, for $v_a \approx -v_o$, the feedback resistor for g should be $2R$ and for $2g$ that should be R , as shown in Fig. 3. Therefore, although the output current i_o contains 3rd-order distortion, the output voltage v_o can be linear.

$$\begin{cases} i_o = g_{m1}v_{in} + g_{ds1}v_o + g_{m3}v_{in}^3 + x_{21}v_{in}^2v_o + x_{12}v_{in}v_o^2 + g_{ds3}v_o^3 \\ -i_a = g_{m1}v_o + g_{ds1}v_a + g_{m3}v_o^3 + x_{21}v_o^2v_a + x_{12}v_o v_a^2 + g_{ds3}v_a^3 \end{cases} \quad (2)$$

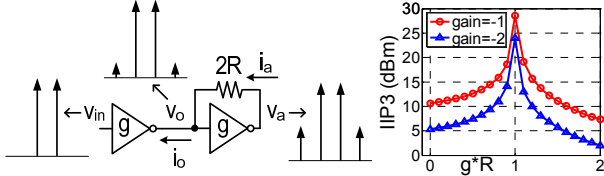


Fig. 4. IM3 compensation mechanism and simulation

The above analysis is only valid to the 1st order. Since v_o is linear and i_a is nonlinear, $v_a = v_o + i_a \cdot 2R$ cannot be linear. Therefore v_a is only equal to $-v_o$ to the 1st order, and then to satisfy $i_o = i_a$, v_o must also be polluted by some distortion, but to a much less degree than v_a . This is why in Fig. 3 all the nodes corresponding to v_a are not used.

Unfortunately this principle can only help the odd-order distortion but not the even-order distortion. By using an inverter, the even-order distortion of the NMOS and PMOS can compensate each other nominally [9], although spread leads to residual distortion. The technique also works for non equal inverters but the improvement can be less. We used it for a gain of -2. The simulation in Fig. 4 shows that a peak IIP3 exists for $R \approx 1/g$ for both gain=-1 and -2 cases. A 25% change of $g \cdot R$ from 1 can still give about 5dB better IIP3 compared to $g \cdot R=0$ ($R=0$, i.e. feedback is short).

V. RF-SAMPLING DOWNCONVERTER

As shown in Fig. 1, the RFSD [5] consists of S/H, I/Q DT mixers with 3rd and 5th HR, a divide-by-4 generating an 8-phase 1/8-duty-cycle LO, and IIR low-pass filters. The RFA in [5] is equivalent to the LNA 2nd stage in this paper, but its topology was not shown. The quadrature outputs are buffered via source followers, only for testing. The RFSD is based on a DT mixing architecture which can achieve wideband quadrature demodulation and wideband HR without channel bandwidth limitation, therefore more suitable for SDR receivers compared to traditional sampling mixers. The LC filter reduces the noise and interference folding from the antenna source, while the HR in RFSD not just can suppress interference further but also reduces the noise folding from LNA which cannot be helped by the LC filter.

VI. EXPERIMENTAL RESULTS

The proof-of-concept receiver is implemented in 65nm CMOS (Fig. 5), taking an active area=0.5mm². The chip is measured on PCB and the input port has $R_{src}=50\Omega$ for all tests. With a 1.2V supply, the current consumption is 5mA for the core (LNA+RFSD), 10mA for the clock at 800MHz LO, and 2.4mA for the output buffer.

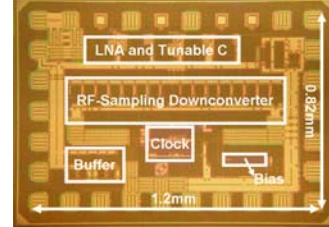


Fig. 5. Chip microphotograph in 65nm CMOS

To verify the tunability of the digitally-controlled LC filter, we measured S_{21} of the LC filter together with the LNA 1st stage (Fig. 3 & Fig. 1). The input of the LC filter is connected to Vector Network Analyzer (VNA) via PCB traces and co-axial cables. At the output of the LNA 1st stage, an active probe (up to 3GHz) is used to perform the differential to single-ended conversion (1x voltage gain) as well as the impedance transformation to 50 Ω to match VNA. Fig. 6 shows the measured S_{21} for low-band (LB) and high-band (HB) respectively, which can continuously cover 300-500MHz and 500-800MHz with less than 3dB gain variation in each band. Due to different inductor values (36nH and 100nH) used, the Q and therefore the peak gain and bandwidth are different for LB and HB. Considering the designed 12dB gain from the LNA 1st stage, the “passive” LC pre-gain is about 14dB for LB and 8dB for HB.

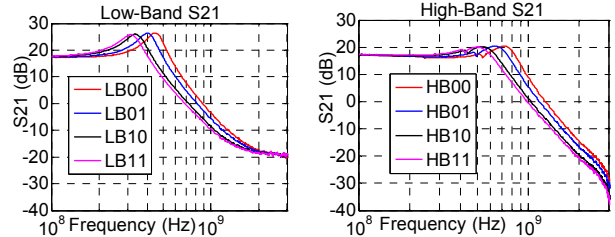


Fig. 6. Measured S_{21} of low-band (LB) and high-band (HB), each band tuned by two digits (00, 01, 10, 11) representing two switchable capacitors (C_2C_1)

Both bands show an effective suppression of LO harmonics, with a minimum of 33dB and 42dB for 3rd and 5th harmonics respectively. The measured 3rd and 5th HR of the complete receiver (4 chips) is shown in Fig. 7, where the HR ratios for the whole band are above 60dB.

Theoretically, balanced LO or 50% duty cycle can reject all even-order harmonics. However, experiments show 2nd-order HR may become the bottleneck, since the LC filter suppresses 3rd and higher order harmonics more. This requires balanced LO being more accurate.

The measured transfer function (Fig. 6) shows a lowered peak frequency and gain from simulation (with on-chip parasitic C modeled, from LNA, ESD and pad), which is most likely due to the excess capacitance from PCB. Via an extra 250fF to emulate the PCB capacitor, about the same transfer function can be achieved.

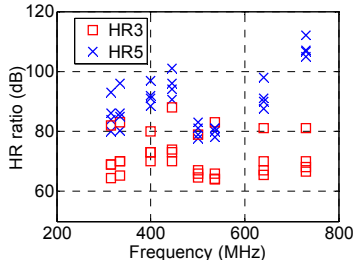


Fig. 7. Measured 3rd and 5th HR ratio (4 chips)

Fig. 8 plots the measured voltage gain and NF of the complete receiver, at the peak frequencies of both bands. The gain difference from LB to HB matches the measured S21 in Fig. 6. The NF is measured via the Y-factor method to read the noise voltage at the output. Fig. 8 shows a clear link between gain and NF, i.e. the high “passive” gain at LB also gives a better NF. The measured minimum NF is 0.8dB for the whole receiver, which shows a very low NF can be achieved with low power consumption (6mW core), even for the sampling receiver suffering from severe noise folding. Such a low NF is achieved via a combination of *sufficient* “passive” pre-gain, 2nd-order LC filter, and HR downconverter.

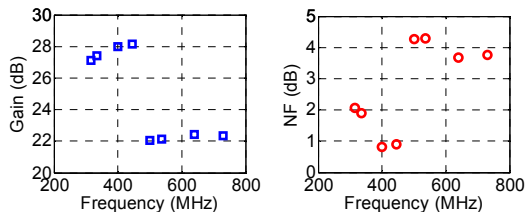


Fig. 8. Measured voltage gain and NF over RF

The measured in-band IIP3 and IIP2 via two-tone test are shown in Fig. 9. From the IIP3 plot, we also see the direct effect of the “passive” pre-gain, sharing almost the same trend as NF. Considering the LC pre-gain, the LNA+RFSD combination should present an IIP3 around 0dBm. Simulation shows the LNA dominates IIP3, which means the 2-stage LNA has an IIP3 around 0dBm. Referred to the input of the LNA 2nd stage (S21 node in Fig. 3), the IIP3 should be about +6dBm. This IIP3 is almost the worst case in Fig. 4, for the gain=-2 curve. On the other hand, the measured DC linearity via three-point method is at least 6dB better than the two-tone test result, leaving some discrepancy we cannot fully explain yet. Since LNA is AC coupled (Fig. 1), the IIP2 is dominated by RFSD and degrades with higher frequency, rather independent of the gain. Most likely it is due to the

degraded balun performance at high band, since IIP2 directly relates to the matching of differential signal.

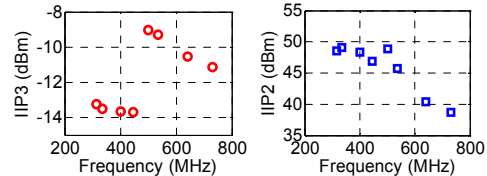


Fig. 9 Measured in-band IIP3 and IIP2 over RF

VII. CONCLUSIONS

A multi-band RF-sampling receiver with more than 60dB 3rd and 5th HR is presented. A low NF (0.8dB) at a low power consumption (6mW core) for sampling receiver can be achieved by a sufficient “passive” pre-gain, together with a simple 2nd-order LC filter and a HR downconverter to reduce noise folding. This LC tank provides the “passive” pre-gain and acts as a harmonic filter tunable via on-chip capacitor banks, significantly improving the sampling downconverter’s HR ratio. The balun-LNA is a cascade of inverter-type amplifiers, partially compensating IM3 products. This flexible sampling receiver has been demonstrated in 65nm CMOS.

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