Reconfigurable Broadband Mixer with Variable Conversion Gain

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***Abstract*—A 2−10 GHz Gilbert-type mixer is reported in which the gate widths of the transistors in the RF stage are reconfigurable. The change in the total gate-width of the RF devices ultimately results in a variable conversion gain for the mixer. Measurements show that the conversion gain can vary from a maximum of 24 dB to a minimum of 9 dB. The IP_{1dB} is −19 dBm at the highest conversion gain setting and −4 dBm at the lowest setting, while the OP_{1dB} remained fairly constant at +3 dBm for all conversion gain levels, as expected. The IIP3 was −12 dBm and +3.5 dBm at the high and low conversion gain settings, respectively. The OPI3 of the mixer remained constant at around +11 dBm. The mixer's dc power consumption was dependent on the conversion gain and it ranged from 2.4 mW up to 18 mW drawn from a single 1.2 V supply. The chip core measures 0.19 mm^2.**

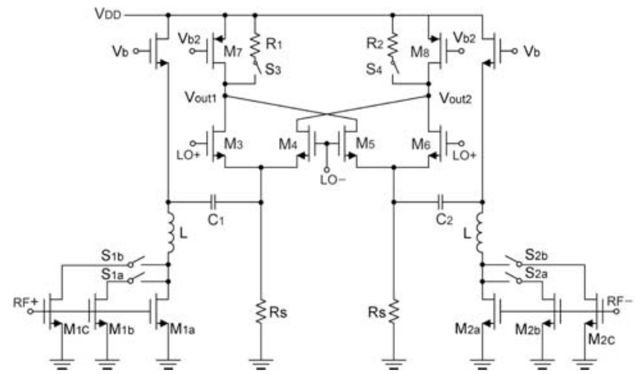

Fig. 1. The proposed reconfigurable broadband mixer circuit.

I. Introduction

It is common for communications transceivers to have a gain-control capability at the RF front-end to maintain the signal stregnth levels within a particular window in response to changes in atmospheric conditions (e.g. rain), temperature variations or other factors.

Usually, the gain control function is carried out using a variable gain amplifier or a variable attenuator. However, recent work on variable conversion gain mixers [1], [2], [3], [4] reveals that it is also possible to use a mixer for system gain control. A benefit of using a mixer in this manner is that the designer can accomplish two separate tasks simultaneously: gain control and frequency conversion, which can result in significant savings in chip area.

In this paper, a downconverter mixer based on the Gilbert-cell topology is presented whose conversion gain can be varied by changing the overall gate-width, W, of the RF transconductor devices. An arrangement of 6 transistors in parallel is used: three transistors on the right and three transistors on the left-hand side of the RF transconductance stage of the mixer. The overall gate-width of the RF stage is changed through two sets of switches that are used to activate or deactivate the parallel transistors. The mixer can achieve a conversion gain variation from 9 dB to 24 dB while consuming 2.4 mW of dc power in the low conversoin gain mode and 18 mW of power in the high-gain mode.

The mixer described in this paper has separate dc bias currents for the RF transconductance stage and the LO switching core, which enables the designer to optimize the conversion gain of the mixer and reduce the impact of $1/f$ noise on the overall noise performance of the mixer.

II. Circuit Description

The proposed mixer is shown in Fig. 1. The RF transconductor stage consists of a parallel arrangement of three NMOS transistors on the lower left ($M_{1a,b,c}$) and three transistors on the lower right-hand ($M_{2a,b,c}$) side of the mixer. When the four switches connected to transistors $M_{1b,c}$ and $M_{2b,c}$ are all ON, the total gate-width, W_{tot}, of the three parallel devices in both the right and left-hand sides is

$$W_{tot} = W_a + W_b + W_c \tag{1}$$

where W_a, W_b and W_c are corresponding gate-widths of transistors $M_{1a,b,c}$ and $M_{2a,b,c}$. Using the short-channel MOSFET device equations, the overall transconductance of the RF devices when they are in saturation is

$$g_m = v_{sat} C_{ox} W_{tot} \tag{2}$$

where v_{sat} is the saturation velocity of the charge carriers in the transistors and C_{ox} is the transistor gate capacitance.

The conversion gain of a Gilbert-cell mixer is related to the transconductance of the devices in the RF stage through the basic relation $CG = \frac{2}{\pi} g_m Z_L$, where Z_L is the IF load

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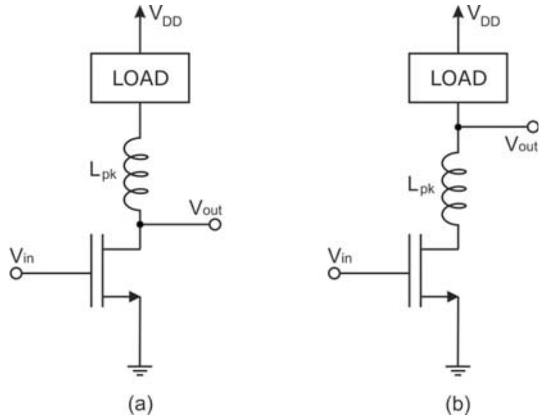

Fig. 2. Illustrative shunt peaking circuits: (a) the conventional topology and (b) the topology used in this paper

impedance of the mixer. Thus, for the mixer in Fig. 1 its conversion gain (CG) can be written as

$$CG = \frac{2}{\pi} v_{sat} C_{ox} Z_L (W_a + W_b + W_c) \tag{3}$$

As the switches in the RF stage, $S_{1a,b}$ and $S_{2a,b}$, are turned ON or OFF the transistors attached to those switches are either connected or disconnected from the rest of the mixer. Therefore, W_{tot} in Eqn. 1 will change in value and the conversion gain of the mixer will also change as a result of Eqn. 3.

To preserve the symmetry of the mixer circuit, switches S_{1a} and S_{2a} are tied to the same ON/OFF control signal and hence they toggle in unison. Similarly, switches S_{1b} and S_{2b} are also connected to a common control signal so that they also act as a pair.

When all four switches $S_{1a,2a}$ and $S_{1b,2b}$ are turned on, the mixer is in the highest conversion gain mode (mode 1) because the effective device area of the RF transconductor stage is at its largest. If switches $S_{1a,2a}$ are on while $S_{1b,2b}$ are off, then the mixer is in mode 2 where it has a moderate conversion gain. In mode 3, the mixer has the lowest conversion gain and it occurs when all four switches, $S_{1a,2a}$ and $S_{1b,2b}$, are turned off and the only devices employed in the RF stage are M_{1a} and M_{2a}. The mixer has an IF load network consisting of transistors $M_{7,8}$ and resistors $R_{1,2}$. When switches $S_{3,4}$ are toggled, the total load resistance can increase or decrease and the result is that within each of the three mixer operating modes, the conversion gain can be fine tuned over an additional range of about 3.5 dB.

Often, it is desirable to bias the LO switching transistors, M_3–M_6, with a low dc current to obtain high switching speeds and to reduce the $1/f$ noise [5] [6] [7]. On the other hand, a somewhat larger dc bias current is preferred in the RF transconductor stage in order to achieve a high conversion gain. If the LO and RF stages of the mixer can be biased independently then there will be more degrees of freedom in the design. Thus, in the mixer shown in Fig. 1, capacitors C_1 and C_2 are used as dc blocks in order to feed different bias currents to the RF and LO stages.

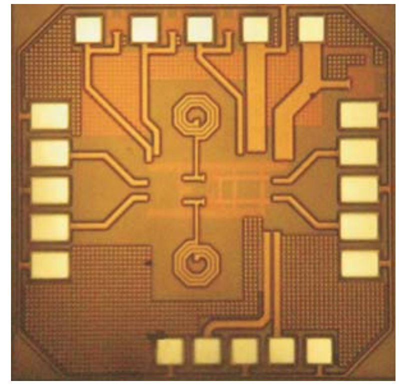

Fig. 3. Microphotograph of the fabricated chip.

Inductive peaking was used to obtain a broadband frequency response for the mixer. In contrast to the more conventional shunt peaking technique in which the output signal is taken between the gain device and the peaking inductor as shown in the illustrative circuit of Fig. 2(a), in this paper the output signal was taken between the inductor and the load as shown in Fig. 2(b). This simple re-arrangement of the output node has an impact on the amount of bandwidth extension that is obtained for this mixer circuit with inductive peaking. Defining the bandwidth extension of the circuit as the ratio of the 3-dB bandwidth with inductive peaking to the 3-dB bandwidth without inductive peaking [8], the bandwidth extension for this circuit can be shown to be [9]

$$\frac{\omega}{\omega_0} = \sqrt{\left(m - \frac{m^2}{2}\right) + \sqrt{\left(m - \frac{m^2}{2}\right)^2 + m^2}} \tag{4}$$

where $m = \frac{R_s C}{L/R_s}$. Calculations using Eq. 4 as well as circuit simulations show that with inductive peaking the 3-dB bandwidth of the proposed mixer can be increased by over 40% compared to an identical mixer without inductive peaking.

III. Experimental Results

The downconverter mixer was fabricated using a standard 130 nm CMOS process and the chip occupies an area of 0.19 mm^2 without bonding pads. A microphotograph of the chip is shown in Fig. 3.

Figure 4 shows the measured conversion gain of the mixer in the different modes. In the measurements, the LO frequency was swept in sync with the RF frequency in order to maintain a constant IF of 200 MHz. Over the span from 2−10 GHz, the mixer has an average conversion gain of 24 dB in mode 1, 17 dB in mode 2, and 9 dB in mode 3. If the gate-source bias voltages of the six RF transistors ($M_{1a,b,c}$ and $M_{2a,b,c}$) are kept constant in each operating mode, it follows that the highest dc power consumption occurs in mode 1 while the

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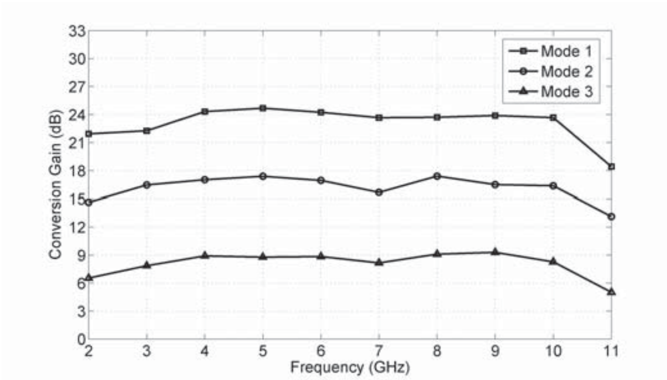

Fig. 4. Measured conversion gain of the mixer versus frequency.

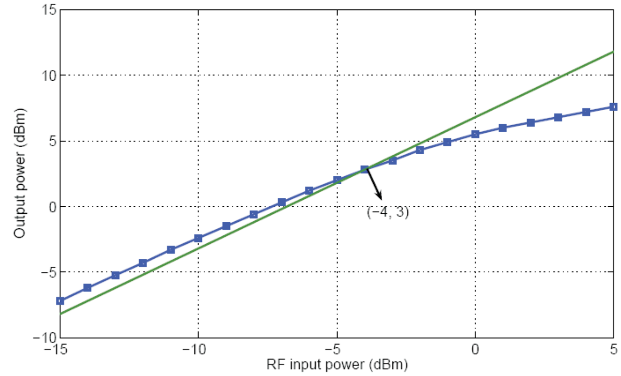

Fig. 6. RF power measurement in gain mode 3 taken at 7 GHz

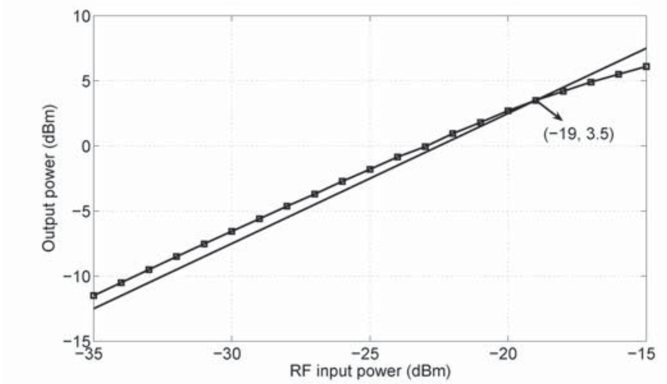

Fig. 5. RF power measurement in gain mode 1 taken at 7 GHz.

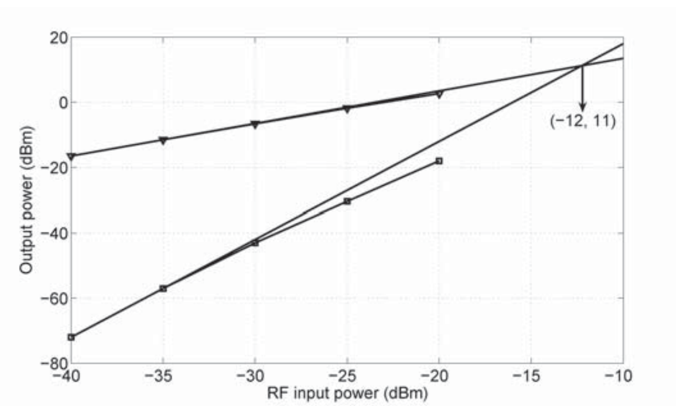

Fig. 7. Two-tone test results in gain mode 1.

lowest consumption is in mode 3 because the dc current draw of any transistor is dependent on its $W \times L$ gate dimensions. The dc power consumption of the mixer was 18 mW, 12 mW and 2.4 mW in modes 1, 2 and 3, respectively.

The 1-dB compression point (P_{1dB}) of the mixer was measured at 7 GHz for every operating mode. As expected, the IP_{1dB} is different in each gain mode because the conversion gain varies but the OP_{1dB} shows very little variation. The IP_{1dB} was -19 dBm in mode 1, -11.5 dBm in mode 2, and -4 dBm in mode 3, while the OP_{1dB} was between +3.0 dBm and +3.5 dBm for the three operating modes. Measurements of the RF output power versus input power performance of this mixer taken in gain mode 1 and at a frequency of 7 GHz are shown in Fig. 5. RF power measurements were also made in gain mode 3 and the results are in Fig. 6.

A two-tone test was also carried out to determine the third-order intercept point (IP3) of the mixer. The IIP3 of the mixer was -12 dBm in mode 1, -3.5 dBm in mode 2, and +3.5 dBm in mode 3 while the OIP3 of the mixer was between +11 dBm and +11.5 dBm for the three gain modes. Experimental results of a two-tone test done when the mixer was in gain mode 1 are shown in Fig. 7. The two-tone test results when the mixer was in gain mode 3 are depicted in Fig. 8. Both of these two-tone tests were carried out using one tone at 6999.5 MHz and another at 7000.5 MHz.

The mixer exhibits a high amount of isolation between the ports. The LO-to-RF isolation, for example, was greater than 62 dB over the entire $2-10$ GHz band. A plot of the measured port-to-port isolations are displayed in Fig. 9.

In most circuits with variable gain such as amplifiers and also in mixers, the designer has to make a tradeoff between conversion gain and noise figure because these two quantities exhibit an inverse relationship. For the mixer in this work, double sideband (DSB) noise figure measurements were taken at 7 GHz and the results show that it has a NF of 8 dB in

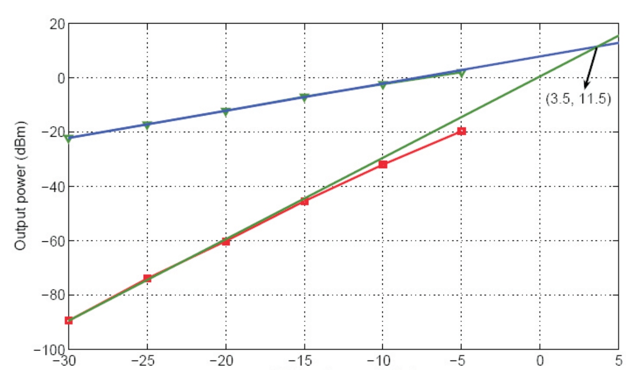

Fig. 8. Two-tone test results in gain mode 3.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

		Units	**This Work**	[1]	[2]	[3]	[4]
RF frequency range		GHz	2 to 10	1.6	2.4	5.25	28 to 37
Conversion gain	(max)	dB	24	8	24.2	6	−11.9
	(min)		9	−49.8	14.5	−28	−21.2
Input P_{1dB}	(max)	dBm	−4	−2	•	−16	•
	(min)		−19	•	−22	•	•
LO-to-RF isolation		dB	> 62	•	30	53	> 30
Supply voltage		V	1.2	1.8	0.8	1.8	N/A
DC power		mW	2.4 to 18	4.2	2	7.2	0 (passive)
Chip area		mm^2	0.19 (core)	0.025	0.931	•	2.89

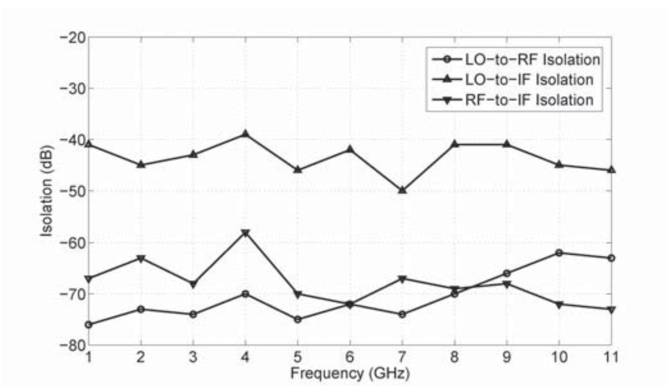

Fig. 9. Measured port-to-port isolations of the mixer in mode 1.

mode 1, 16 dB in mode 2 and 23 dB in mode 3. A summary of the measured results and a comparison with other works is shown in Table I.

IV. CONCLUSION

Variable conversion gain mixers are very attractive circuits for use in communications systems because they can carry out two distinct functions at once: frequency conversion and gain control. Instead of using dc bias variations to change the conversion gain of the mixer, the circuit presented here does so by reconfiguring the effective size of the devices in the RF transconductor stage using an arrangement of parallel transistors and switches.

V. ACKNOWLEDGMENTS

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