# A 24 GHz Quadrature Pulsed Oscillator for Short-Range UWB Vehicular Radar Applications

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***Abstract*—A new 24 GHz quadrature pulsed oscillator is presented using 0.13 $\mu$m CMOS for short-range ultra-wideband (UWB) vehicular radar. A quadrature inductor-capacitor (LC) oscillator is quickly switched on and off for a pulse repetition time (PRT) as short as 1.66 ns. The switching technique creates a large initial voltage for fast startup (0.5 ns) and locks the initial phase of the oscillations to the input clock for phase coherence. The measured output phase noise matches that of the clock signal, with a relatively low phase noise of -70 dBc/Hz and -100 dBc/Hz at 1 kHz and 1 MHz offset respectively. The integrated rms jitter from 100 Hz to 1 MHz is thus less than 720 fs. The circuit consumes a low average power of less than 1.6 mW and 13.3 mW at 50 MHz and 600 MHz pulse repetition frequencies (PRFs) respectively, or below 8 pJ of energy per pulse. It occupies an active area of less than 0.17 mm$^2$.**

## I. Introduction

Ultra-Wideband (UWB) short-range radar (SRR), which is regulated by the Federal Communications Commission (FCC) for commercial use in the 22 to 29 GHz frequency band, is a key element in comprehensive environment sensing for automobiles, complementing other technologies such as infrared (IR), ultrasonic, video and long-range Active Cruise Control (ACC) radars [1]. A network of 16 or more UWB radar sensors [2] can provide a variety of features, ranging from simple parking aids to more sophisticated blind-spot monitoring, pre-crash detection and stop-and-go [1].

In conventional pulsed vehicular radars, pulses are generated by time gating the output of a local oscillator (LO) phase-locked loop (PLL) using a switch [1], [3]–[7]. The LO PLL is continuously running since its turn-on and locking transient are usually not short enough for it to be switched off and on between pulses, resulting in high LO leakage and a low power efficiency. Furthermore the LO PLL can be rather complex, occupying a large chip area and/or consuming significant power. Although power consumption is not a primary concern in automobiles, the total power consumption can become significant as the number of sensors is increased for enhanced processing capability [2]. Pulsed oscillators have also been investigated [8]–[15]. However, most if not all of them are implemented using expensive technologies such as Gallium Arsenide (GaAs), and they do not provide quadrature outputs. Furthermore, pulse generators employing passive filters [16] or distributed structures of edge combiners [2] have been reported. They often occupy a large area or are limited to a specific pulse and frequency spectrum that highly depend on device parameters and matching.

In this paper, a new 24 GHz quadrature pulsed oscillator is proposed using 0.13 $\mu$m CMOS for short-range UWB vehicular radar applications. It is part of a quadrature pulse generator that includes a variable attenuator to shape the amplitude envelope and time duration [17]. The full quadrature pulse generator provides template pulses for quadrature pulse correlation [1], [3]–[5], or enables quadri-phase pulse coding for enhanced pulse compression and interference mitigation. A 24 GHz quadrature inductor-capacitor (LC) oscillator is quickly switched on and off with a pulse repetition time (PRT) as short as 1.66 ns or a pulse repetition frequency (PRF) as high as 600 MHz, allowing it to be readily shared between the transmitter and receiver for range gates as short as 0.25 m. As the oscillator is switched off between pulses, LO leakage, LO self-mixing, DC offsets and power consumption are reduced. The oscillations settle within about 0.5 ns from startup, and their initial phase is locked to the input clock for phase coherence.

## II. Circuit Design and Simulations

A circuit diagram of the 24 GHz quadrature pulsed oscillator is shown in Fig. 1. It consists of a quadrature LC oscillator, output buffers, and a current switching network. Current-starved inverter chains sharpen the rising/falling edge of the clock signal (CLK) and realize two trigger signals $CLK+$ and $CLK-$ with a short delay between them. These signals are used to drive the current switching network, which turns on and off the biasing current of the oscillators ($I_{I+}$, $I_{I-}$, $I_{Q+}$ and $I_{Q-}$) and buffers ($I_{BI+}$, $I_{BI-}$, $I_{BQ+}$ and $I_{BQ-}$) to generate differential quadrature 24 GHz pulsed oscillations ($LO_{I+}$, $LO_{I-}$, $LO_{Q+}$ and $LO_{Q-}$).

### A. Quadrature LC Oscillator

The quadrature LC oscillator circuit designed in this work is shown in Fig. 2. It consists of two differential LC oscillators that are quadrature-coupled using the body terminals (or back-gates) of the PMOS devices $M_{P1}$, $M_{P2}$, $M_{P3}$ and $M_{P4}$. The inductors ($L$) used in this circuit are symmetric spirals, and are 100 $\mu$m $\times$ 100 $\mu$m in size with one turn and 7.5 $\mu$m trace width. An electromagnetic (EM) simulation of the inductors predicts an inductance of 0.16 nH and a quality-factor (Q) of

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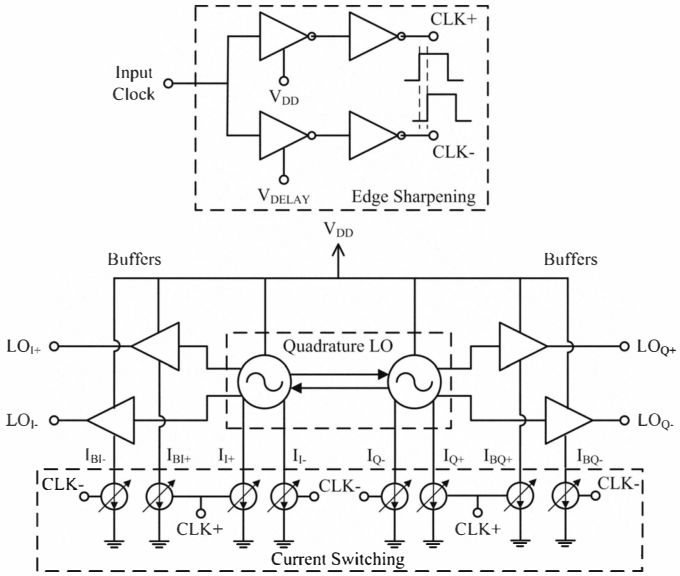


Fig. 1. Circuit diagram of quadrature pulsed oscillator.

approximately 26 at 24 GHz. The total capacitance $C$ seen at the output nodes including the parasitic capacitance of the cross-coupled transistors, common-source buffers and metal interconnects is about 0.27 pF for oscillation at 24 GHz.

The initial startup transient of the oscillations can be characterized by the well-known "van der Pol" non-linear differential equation which can be solved for the differential output voltage $v(t)$ as [18]:

$$v(t) = \frac{2v_0}{\sqrt{1 + \left(\left(\frac{2v_0}{v(0)}\right)^2 - 1\right) e^{-\epsilon\omega_0 t}}} \cos(\omega_0 t - \phi) \quad (1)$$

where $\epsilon = (g_m - 1/R_P)\sqrt{L/C}$ is a damping factor, $g_m$ is the transconductance of the differential pair, $R_P$ is the equivalent parallel resistance of the LC tank, $v(0)$ is the initial condition voltage and $2v_0$ is the steady-state oscillation amplitude. The settling time $t_s$ for the oscillation $v(t)$ to reach 90% of its steady state value $2v_0$ can be derived from (1) [18]:

$$t_s \approx \frac{Q_{res}}{\omega_0 (A_{OL} - 1)} \left[2 \ln\left(\frac{2v_0}{v(0)} - 1\right) + 1.45\right] \quad (2)$$

where $A_{OL} = g_m R_P$ is the open-loop gain and $Q_{res} = R_P\sqrt{C/L}$ is the quality-factor of the LC tank. It is clear that the settling time $t_s$ is shorter for larger initial conditions $v(0)$. In addition, the settling time can be reduced by decreasing $\frac{Q_{res}}{\omega_0(A_{OL}-1)}$, which can be approximated for $A_{OL} >> 1$ as:

$$\frac{Q_{res}}{\omega_0 (A_{OL} - 1)} \approx \frac{Q_{res}}{\omega_0 A_{OL}} = \frac{R_P\sqrt{C/L}}{g_m R_P/\sqrt{LC}} = \frac{C}{g_m} \quad (3)$$

From (3), the settling time $t_s$ can be reduced by decreasing the tank capacitance $C$ or increasing the transistor transconductance $g_m$. Thus the capacitance $C$ is minimized to include only the parasitic capacitance of the cross-coupled transistors ($M_{N1}$, $M_{N2}$, $M_{P1}$, $M_{P2}$) and the connecting common-source buffers ($M_{N5} - M_{P5}$ and $M_{N6} - M_{P6}$).

### B. Current Switching

The biasing currents of the two differential oscillators ($I_{I+} - I_{I-}$ and $I_{Q+} - I_{Q-}$) and that of the four output buffers ($I_{BI+} - I_{BI-}$ and $I_{BQ+} - I_{BQ-}$) are switched on and off using NMOS switches ($M_{SW1} - M_{SW8}$) as shown in Fig. 2. By switching on one side of each differential oscillator before the other (i.e. switching on $M_{SW1}$ before $M_{SW2}$, and $M_{SW3}$ before $M_{SW4}$), a current $I_{inj}$ initially flows through the LC tank as shown in Fig. 2. The current-starved inverters shown in Fig. 2 are used to introduce a very short delay between the clock signals $CLK+$ and $CLK-$ that trigger the pair of switches. Therefore the initial current $I_{inj}$ only flows for a short time. In effect, a current impulse with a short time duration is injected through the LC tank, which can have high harmonic components out to 24 GHz. This creates a large initial condition ($v(0)$) for a short settling time as indicated by (2) [18]. It also sets the initial phase of the oscillations, locking it to the input clock. Note that the delay between the clock signals $CLK+$ and $CLK-$ can be tuned using the control voltage $V_{DELAY}$ (Fig. 1) to vary the time duration of the current impulse $I_{inj}$.

The oscillator was simulated in the time-domain using a 500 MHz clock signal (50% duty-cycle square wave). The control voltage $V_{DELAY}$ is set to 0.98 V for a delay of about 18 ps between the clock signals $CLK-$ and $CLK+$. The resulting current impulse has an amplitude larger than 4 mA and a time duration of only 48 ps, yielding a large initial condition voltage $v(0)$ of about 45 mV. The differential buffered LO signals ($LO_I = LO_{I+} - LO_{I-}$ and $LO_Q = LO_{Q+} - LO_{Q-}$) are shown in Fig. 3, and can reach steady-state within 0.5 ns from the $CLK+$ rising edge. The peak-to-peak voltage is about 760 mV and the time duration is around 1.2 ns. The clock on period and the pulsed output time duration can be set as short as 0.8 and 1.0 ns respectively, yielding a –10 dB bandwidth of more than 2.0 GHz.

## III. Experimental and Measurement Results

The quadrature pulsed oscillator was fabricated in a standard 0.13 $\mu$m CMOS process and a photograph of the IC is shown in Fig. 4. It occupies a die area of 0.54 mm$^2$ including bonding pads, decoupling capacitors and the chip guard ring (plus chamfer regions), while the core circuit area is 0.17 mm$^2$. The circuit consumes less than 1.6 mW of average power at a PRF of 50 MHz. The power consumption increases with the PRF, reaching 13.3 mW at the maximum PRF of 600 MHz. This gives an energy consumption $E_p$ of less than 8.0 pJ and 5.5 pJ at 50 MHz and 600 MHz PRF respectively for each of the four differential quadrature pulses.

The quadrature pulsed oscillator IC was measured directly on-wafer using 40 GHz coplanar waveguide (CPW) probes and DC probes. Fig. 5 shows the measured output power spectrum, when the quadrature oscillator is in free running mode, i.e. the input clock is held at logic high ($V_{DD} = 1.4$V). The free-running output power level is about –5.0 dBm (single-ended) at a frequency of 23.9 GHz.

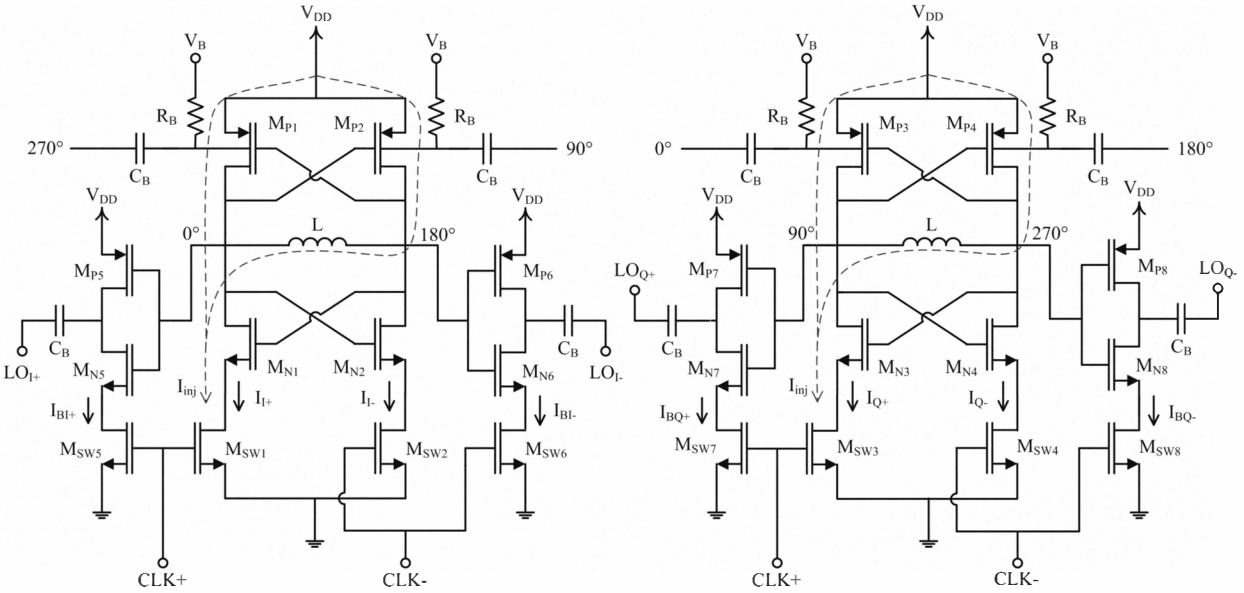


Fig. 2. Circuit schematic of quadrature LC oscillators and buffers.

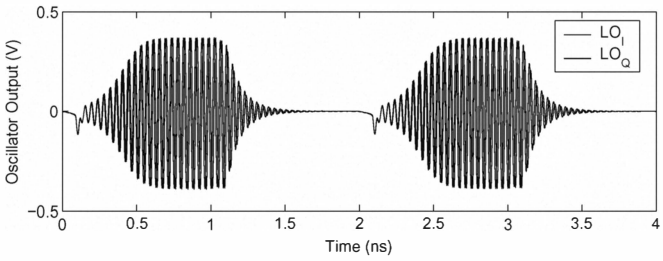


Fig. 3. Simulated pulsed oscillator waveforms.

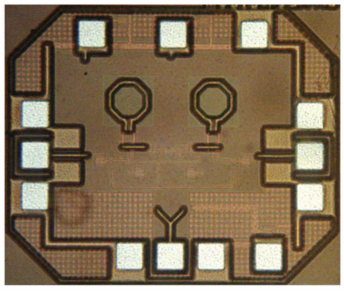

Fig. 4. Photograph of quadrature pulsed oscillator IC.

The pulsed output power spectrum was also measured over a span of 8 GHz and is plotted in Fig. 6 (left). The clock frequency was set to about 500 MHz (508 MHz), and the power spectrum exhibits peaks at multiples of the clock frequency since the output is periodic (unmodulated). The generated harmonic components are coherent and well-defined, and Fig. 6 (right) shows the generated peak at 23.92 GHz in more detail over a span of only 1 MHz, clearly showing stable and locked operation. The 24 GHz oscillation cycles were also clearly visible and stable in the pulsed output when viewed on a time sampling oscilloscope triggered with the input clock, indicating phase coherence.

Fig. 7 shows the measured phase noise of the generated pulsed output at 23.92 GHz. The measured phase noise of the clock reference and that of the free-running output (Fig. 5) are also included for comparison. The output phase noise matches that of the clock reference but is approximately 33 dB higher. This corresponds to the frequency ratio between the output and the clock reference since 20 log (23.92/0.508) = 33 dB. Fig. 7 verifies that the 24-GHz oscillator is phase locked to the 500 MHz clock reference, achieving a relatively low phase noise of –62 dBc/Hz at 100 Hz, –70 dBc/Hz at 1kHz and –65

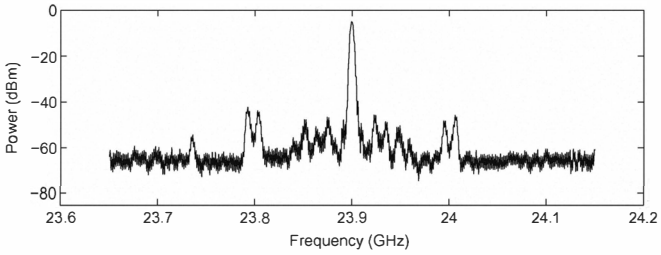


Fig. 5. Measured free-running output spectrum over a span of 500 MHz.

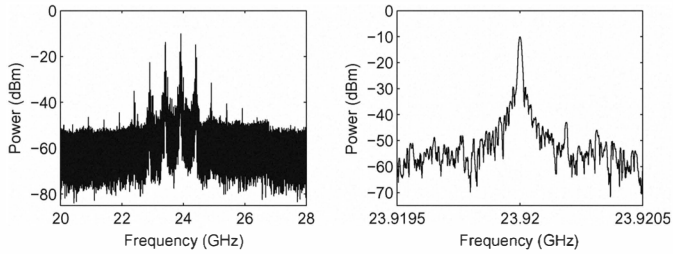


Fig. 6. Measured pulsed output spectrum over an 8 GHz span (left) and a 1 MHz span (right).

TABLE I
SUMMARY OF QUADRATURE UWB PULSED OSCILLATOR CHARACTERISTICS

| Characteristic | **This work** | [2] | [3] | [4] | [14] | [15] |
|---|---|---|---|---|---|---|
| Technology | **0.13 $\mu$m CMOS** | 90 nm CMOS | 0.18 $\mu$m CMOS | 0.13 $\mu$m SiGe | GaAs HBT | GaAs HBT |
| Circuit Area (mm$^2$) | **0.17** | 0.0014 [1] | – | – | 1.17 | 1.0 |
| Power (mW) | **13.3** | 1.4 | 42 | 14.5 | 55 | – |
| PRF (MHz) | **600** | 500 | – | 10 | 62.5 | 10 |
| Energy | **5.5 pJ/pulse** | 2.8 pJ/pulse | – | – | – | – |
| Peak-to-Peak Amplitude | **380 mV** | 71 mV | – | 630 mV | 1.4 V | 600 mV |
| Time Duration | **1.0 ns** | 552 ps | 250 ps | 1.0 ns | 1.0 ns | 900 ps |
| Carrier Frequency (GHz) | **23.9** | 25.5 | 26.5 | 24.125 | 24.31 | 26.5 |
| Phase Noise (dBc/Hz) | **-70 at 1 kHz**<br>**-100 at 1 MHz** | – | -57 at 10 kHz<br>-107 at 1 MHz | -56 at 1 kHz<br>-104.3 at 1 MHz | -102.5 at 100 kHz<br>-120.83 at 1 MHz | – |

[1] External bias-tee (choke inductor) used for edge and pulse combining.

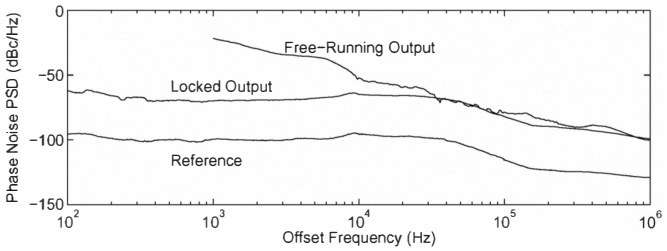


Fig. 7. Measured phase noise of pulsed output at 24 GHz.

dBc/Hz at 10 kHz. This amounts to a low integrated rms jitter of 720 fs from 100 Hz to 1 MHz.

Table I summarizes the circuit's characteristics in comparison with other work [2]–[4], [14], [15]. It has comparable phase noise and a higher energy efficiency (output voltage per energy consumed). The circuit area is also relatively small.

## IV. CONCLUSION

A new 24 GHz quadrature pulsed oscillator has been developed in 0.13 $\mu$m CMOS. By switching on one side of each differential oscillator in the quadrature-coupled pair just before the other, a current impulse is injected into the LC tank, creating a large initial condition for fast startup and locking the initial phase of the oscillations to the input clock. The measured output phase noise matches that of the clock signal, with a low value of -70 dBc/Hz at 1 kHz offset, and -100 dBc/Hz at 1 MHz offset. This reduces the integrated rms jitter from 100 Hz to 1 MHz to less than 720 fs. The circuit consumes below 8 pJ of energy per pulse and occupies an active area of less than 0.17 mm$^2$.

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