4.0−5.5 GHz Tunable Power Splitter RFIC using Active Inductors

You Zheng[1] and Carlos E. Saavedra[2]

[1]Formerly with Queen's University, now with SkyWave Mobile Communications, Ottawa, Ontario, Canada
[2]Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada

***Abstract*—A highly compact and tunable four-port power splitter was designed and fabricated in a 180 nm CMOS process. Instead of distributed transmission lines, an LC lumped-element equivalent was selected for on-chip realization of the power splitter. To further reduce the varied by changing the bias current of the gyrator circuit. Experimental tests reveal that the power split is 6 dB and the center frequency can be tuned from 4.0 GHz to 5.5 GHz. The chip was biased from a 3 V dc voltage supply and consumes a maximum of 69 mW of power.**

***Index terms*−active indcutors, active power splitters, power couplers, RFIC's, CMOS**

I. Introduction

In spite of the low cost of CMOS RF integrated circuits (RFIC's) compared to their III-V counterparts, there is a class of high-frequency circuits that remains prohibitively expensive to implement on-chip even in CMOS: passive microwave circuits. The basic problem is that the physical dimensions of distributed-element passive circuits such as power splitters, filters and baluns, for instance, are on the order of the signal wavelength. Thus, at the lower end of the microwave spectrum these circuits are too large for on-chip realization. As a result, passive microwave circuits are usually located off-chip, on a printed circuit board, which reduces the overall manufacturing throughput and yield for microwave systems.

One approach to bring low-frequency passive microwave components on-chip has been to reduce their size by converting the distributed-element circuits into lumped-element equivalents [1]–[4]. This lumped-element approach is attractive for circuits such as power splitters because, in many instances, inductors with moderate quality factors (Q's) can be used which are easier to implement in CMOS and other semicondor processes. Power splitters are ubiquitous circuits in high-frequency systems [5], [6] and their most common manifestation is the equal n-way splitter although unequal splitters [7]–[9] are also used.

This paper reports on the design and experimental verification of a lumped-element power splitter implemented in a standard 180 nm CMOS process. Through the use of active inductors [10]–[13] instead of passive spiral inductors the size of the coupler was further reduced. The proposed power coupler's center frequency can be tuned from 4.0 GHz to 5.5 GHz while the splitter described in [3], also implemented in 180 nm CMOS, has a tuning range of 3.6 GHz to 4.7 GHz.

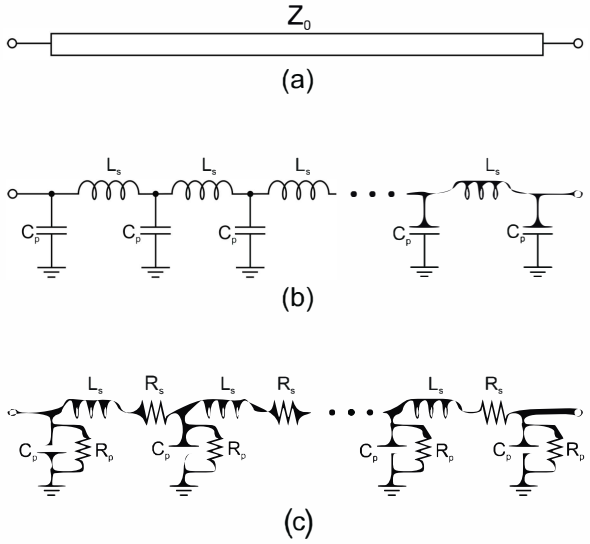

Fig. 1. (a) distributed transmission line and its (b) lossless and (c) lossy lumped-element equivalent circuit models.

II. Power Splitter Circuit

The distributed transmission line depicted in Fig. 1(a) can be modeled [14] with the lumped-element L-C ladder circuit in Fig. 1(b). If the dielectric material on which the transmission line rests is very pure and if a high-quality metal is used to implement the transmission line traces, then the lossless model in Fig. 1(b) can be used. For best accuracy, the lossy transmission line model in Fig. 1(c) is used because it accounts for the finite conductivity of the metal trace and the dielectric losses through resistances R_s and R_p, respectively. When the length of a transmission line is sufficiently short (i.e. less than one wavelength) then a truncated version of the lumped-

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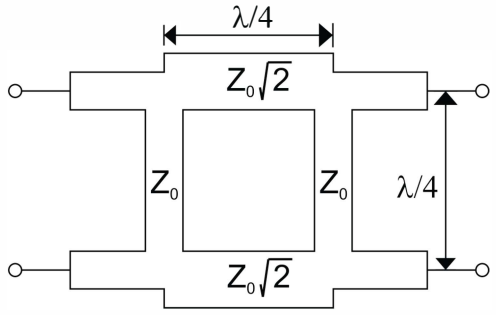

Fig. 2. Distributed-element microwave branchline power splitter.

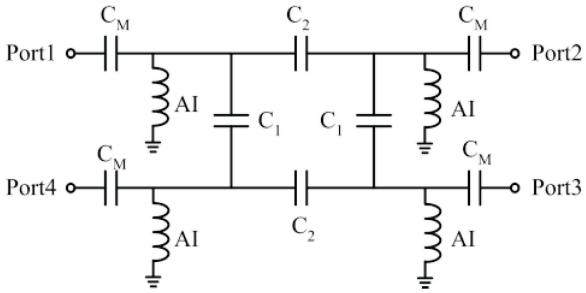

Fig. 3. Lumped-element realization of the branchline power splitter.

element networks can be used. The truncated model normally has three components and it is most accurate at the frequency at which the components are calculated.

A diagram of the microwave power splitter that was chosen for this work is shown in Fig. 2. Port 1 is the input port, Ports 2 and 3 are the signal transmission ports and Port 4 is isolated. Each $\lambda/4$ segment of transmission line was replaced with a three-component equivalent circuit and the result is the circuit in Fig. 3. For simplicity, and to reduce area, all parallel components sharing a single node were merged into a single component. Note that while the equivalent transmission models in Fig. 1 have series inductances and shunt capacitors, the circuit in Fig. 3 has shunt inductors and series capacitors. This reversal was carried out through a $Y \leftrightarrow \Delta$ circuit transformation.

The series capacitors (C_M) at the port terminals serve as dc blocks and also help with input impedance matching. The capacitances C_1 and C_2 were implemented using MOS varactors so that their values could be optimized for best phase and amplitude balance in the power splitter. For this design, the capacitor values were: C_M = 0.4 pF, C_1 = 0.2 pF, C_2 = 1.414 C_1 The lumped-element inductors were implemented using the transistor-based circuit shown in Fig. 4. The active inductor saves chip area compared to a spiral inductor and its inductance value can be changed by varying its bias current. At 4.75 GHz, the center frequency of the power splitter's tuning range, the active inductors had a value of 1.4 nH. The ability to simultaneously vary the capacitances C_1 and C_2 plus the inductances allows the center frequency of the power splitter to be tuned over a very broad frequency range of 1.5 GHz between 4.0 GHz and 5.5 GHz.

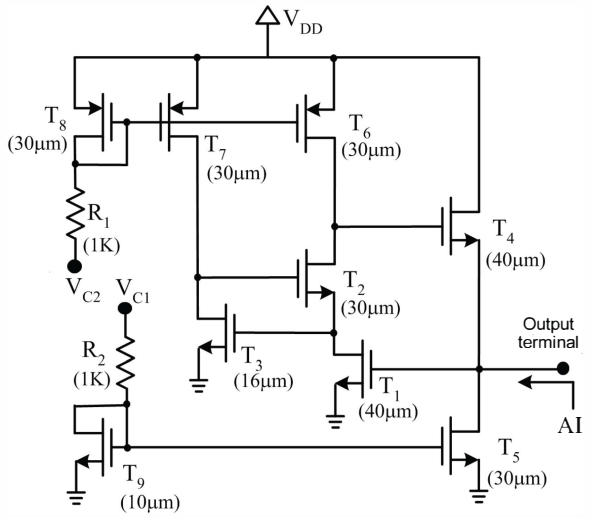

Fig. 4. Actrive inductor circuit topology realized in 180 nm CMOS.

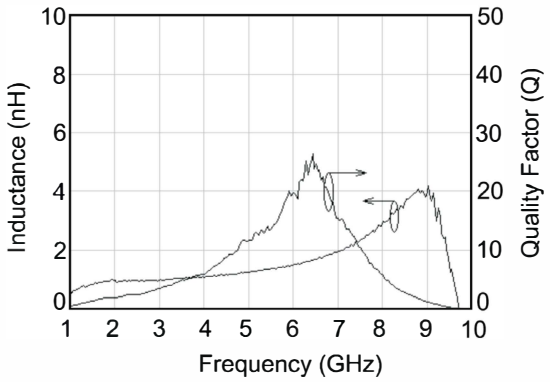

Fig. 5. The active inductor's measured inductance versus frequency.

The topology used for the active inductor in Fig. 4 has two feedback loops: transistors T_1/T_2/T_4 make up the first loop and transistors T_2/T_3 make up the second loop. The two loops are joined at transistor T_2. This dual loop arrangement improves the frequency response of the active inductor compared to configurations that rely on a single loop topology [10]. DC current is supplied to the active inductor through a pair of current mirrors. The mirror currents are controlled through the voltages V_{C1} and V_{C2}.

III. Experimental Results

A chip was fabricated to test the active inductor performance by itself and another chip was fabricated to test the performance of the power splitter. Both chips were fabricated using a standard 180 nm CMOS process.

The plot in Fig. 5 shows the measured inductance and quality factor of the active inductor as a function of frequency. This active inductor was designed to produce an inductance of 1 nH, which is maintained over a span of nearly 5 GHz. The maximum inductance is 4 nH at 9 GHz and its self-resonant

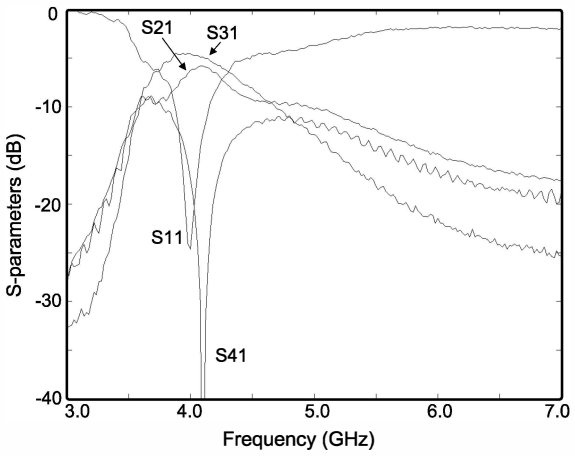

Fig. 6. Measured s-parameters at the lower-end of the band.

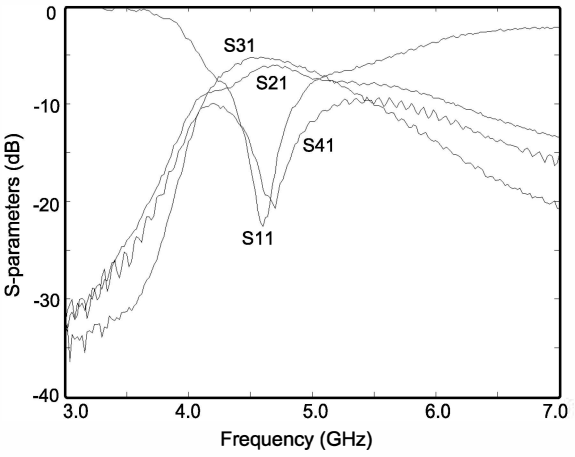

Fig. 7. Measured s-parameters at mid-band.

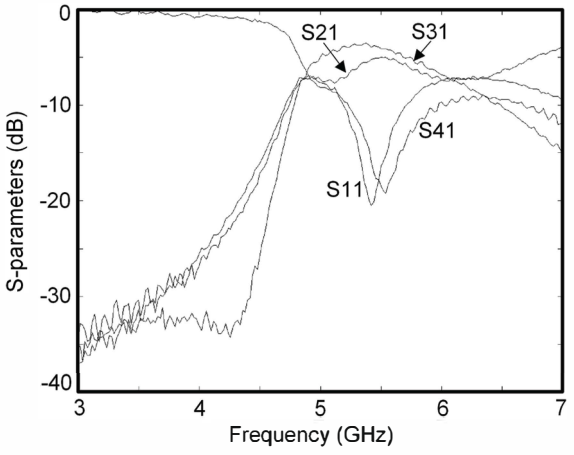

Fig. 8. Measured s-parameters at the upper-end of the band.

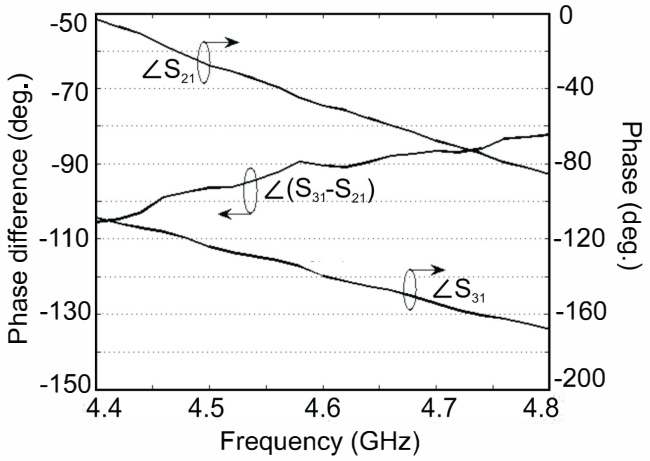

Fig. 9. Measured phase response at mid-band.

frequency is 9.8 GHz. The quality factor of this inductor peaks at around 20 at 6.4 GHz. Active inductors often have much better Q's than passive inductors because they can be designed to have a very small accompanying parasitic resistance. The parasitic resistance can even be negative in which case it can be used in conjunction with a capacitor to create an oscillator.

Figures 6, 7, and 8 show the measured s-parameters of the power splitter at 4 GHz, 4.75 GHz and 5.5 GHz, respectively. For all three cases, the forward transmission coefficients, S_{21} and S_{31}, are close to -6 dB. Ideally, the transmission coefficients should be -3 dB, but in this splitter the additional 3 dB drop comes from the MOS varactors and losses in the active inductors. Increasing the transistor dimensions in the active inductors can reduce their loss but the tradeoff would be a lower center frequency for the overall circuit. The power splitter's reflection coefficient at the input port, S_{11}, and the isolation between ports 1 and 4, S_{41}, are around -20 dB or lower. At the center frequency of 4.75 GHz, the active inductor's internal bias voltages in the power splitter, V_{C1} and V_{C2}, were set to 1.1 V and 0.44V, respectively.

The phase response of the power splitter was measured at different center frequencies. The plot in Fig. 9 shows $\angle S_{21}$, $\angle S_{31}$ and $\angle(S_{21}\text{-}S_{31})$ when the splitter was tuned to 4.75 GHz. As expected for a quadrature power splitter $\angle(S_{21}\text{-}S_{31})$ is in the neighborhood of 90°.

The plot in Fig. 10 shows the input power versus output power response of the splitter. The input 1-dB compression point (IP_{1dB}) of this splitter is -20 dBm when the output power is measured at port 2 and -18 dBm when the output is measured at port 3. In active power splitters the linearity is limited by the active inductors, a feature also observed in the circuit reported in [3].

A microphoto of the fabricated chip is shown in Fig. 11.

IV. Conclusion

Traditional high-frequency power splitters using distributed elements require a large area because their size is proportional to the signal's wavelength. To reduce the size of a power splitter so that it can be placed on-chip a lumped-element realization of a microwave power splitter was designed and

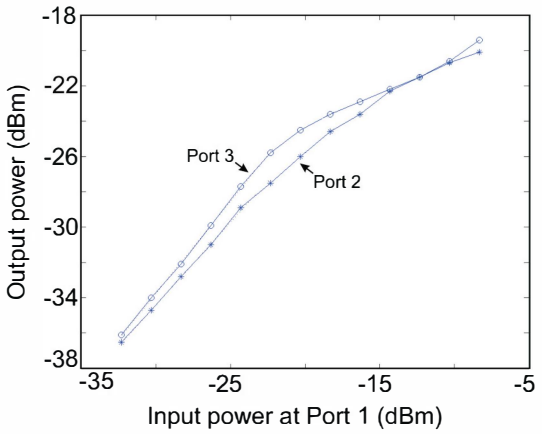

Fig. 10. Measured input power versus output power response of the splitter.

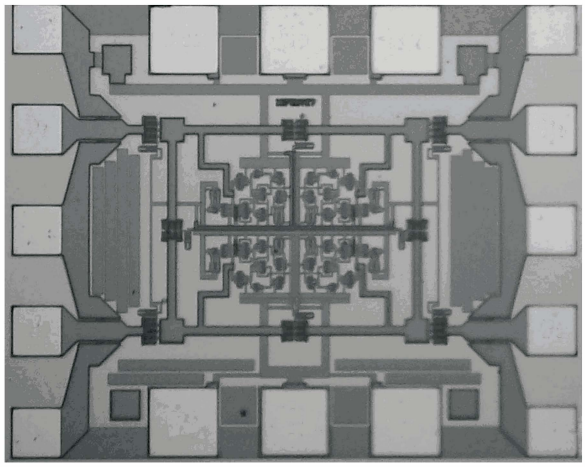

Fig. 11. Microphotgraph of the power coupler chip

fabricated using a 180 nm CMOS process. Instead of passive spiral inductors, active inductors were used to further reduce the area footprint of the power splitter. Using the active inductor also allows for frequency tunability which is not possible when using passive power splitters.

V. Acknowledgments

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