A Volterra Series Approach for the Design of Low-Voltage CG-CS Active Baluns

Shan He and Carlos E. Saavedra
Gigahertz Integrated Circuits Group
Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada K7L 3N6

***Abstract*—A low-voltage active balun and amplifier is presented. The circuit uses a common-gate common-source (CG-CS) noise-cancelling topology with a simple distortion cancellation method to improve the IIP_3 performance of the balun-amplifier. A Volterra series analysis is employed to provide insights into the nonlinear behavior of the circuit. A chip was fabricated and the experimental test results show an average voltage gain for the balun-amplifier of 16.2 dB and a maximum IIP_3 of -3.8 dBm over the span of 0.3−2.4 GHz. The circuit exhibits a noise figure below 4.0 dB over the measured band and reaches a minimum of 3.2 dB. The chip uses a single 0.9 V dc supply and consumes 15.8 mW of power. The RFIC was fabricated using a standard 130 nm CMOS process.**

***Index Terms*—active balun, balun-amplifier, CMOS, intermodulation distortion, IMD, Volterra series analysis**

I. Introduction

Spectral bands within the frequency range of a few hundred MHz to the low GHz are highly coveted by the broadcasting and communications industries. An important reason for the appeal of these bands is that the carrier waves have long wavelengths which allows them to propagate through forrests, buildings, or other large objects. In addition, those waves can travel over large distances due, in part, to low atmospheric attenuation.

The electronic circuitry used for the lower frequency bands is generally much less expensive than the circuits used at high microwave and millimeter wave frequencies. Yet, in the category of passive circuits the situation is reversed: it is often prohibitively expensive to implement components such as baluns and filters on-chip at low frequencies compared to high frequecies because the component dimensions are too large−even if implemented using lumped elements. As a result, low-frequency passive components are typically located off-chip which, in turn, increases the parts count and thereby the overall cost of the system.

While active baluns offer the benefit of compact size [1]–[6], such circuits must be used with care because their linearity performance often places a strong upper limit on the IIP_3 of an entire receiver chain. When an active balun's dc supply voltage is lowered its linearity is degraded unless steps are taken to alleviate the issue.

This paper reports a design approach for low-distortion active baluns-amplifiers using the common-gate common-source (CG-CS) topology based on a Volterra series analysis of the nonlinear response of that circuit. The CG-CS topology was selected because it has the interesting property of offering simultaneous noise and distortion cancellation [7], [8] which allows the designer to optimize the circuit for both metrics. To verify the design approach we fabricated and tested a chip using a standard 130 nm CMOS process. The circuit is biased from a single 0.9 V supply and it exhibits a maximum IIP_3 of -3.8 dBm and a noise figure below 4.0 dB over an ultrawide bandwidth of 0.3 to 2.4 GHz (8:1).

II. Linearity Analysis of the Active Balun

Fig. 1 illustrates the circuit schematic of the wideband low-voltage active balun-amplifier. The design, in its essence, is composed of two parts, the common gate (CG) transistor M_1 which provides the in-phase signal and the common source transistors M_2 and M_3 that yield the out-of-phase signal. The capacitances C_0, C_1 and C_2 model the parasitic capacitance of the RF probe pads on the fabricated chip.

The voltages seen at the source and the drain of transistor M_1 are defined by the following operations with respect to the input voltage V_s

$$V_0 = A_1(\omega) \circ V_s + A_2(\omega_1, \omega_2) \circ V_s^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \quad (1)$$

and

$$V_1 = B_1(\omega) \circ V_s + B_2(\omega_1, \omega_2) \circ V_s^2 + B_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \quad (2)$$

while the voltage at the drain of M_2 and M_3 is given by

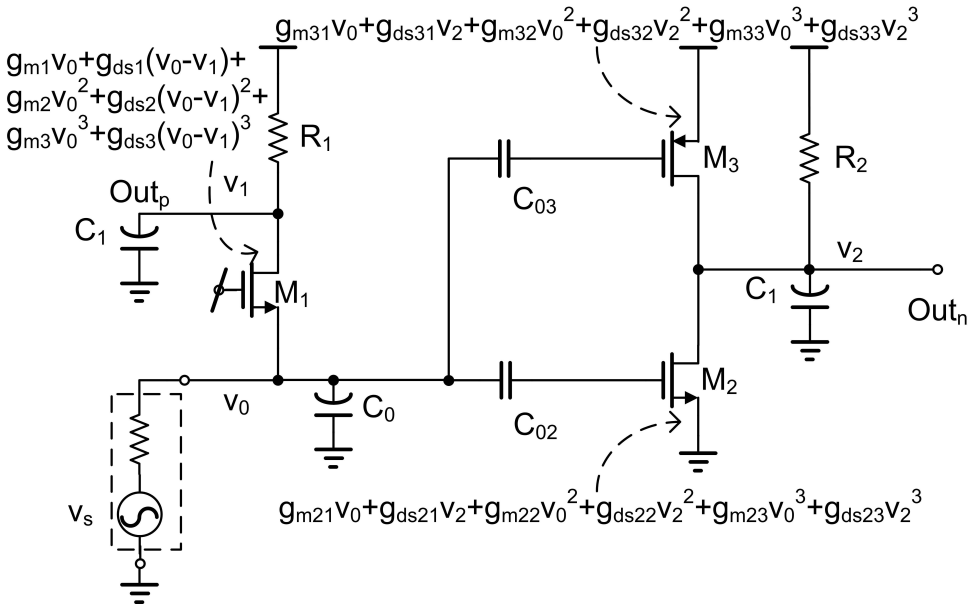


Fig. 1. Circuit schematic of the wideband, low-voltage, active balun and amplifier circuit.

$$\begin{aligned} V_2 =& K_1(\omega) \circ V_s + K_2(\omega_1, \omega_2) \circ V_s^2 + \\ & K_3(\omega_1, \omega_2, \omega_3) \circ V_s^3. \end{aligned} \tag{3}$$

where each $\circ$ denotes the Volterra operand, the ω's denote the dependent frequencies and A_1, A_2, and A_3 are the Volterra kernels that model the first, second, and the third order nonlinear response of M_1 at the source terminal due to the applied input V_s. Similarly the B_n's model the n^{th}-order nonlinear response at the drain of M_1 while the K_n's model the response at the drains of M_2 and M_3 due to the applied input voltage V_s.

Let $Y_s = 1/R_s$ be the admittance of the signal source, $Y_0 = sC_0$ be the parasitic admittance at node V_0 and $Y_1 = 1/R_1 + sC_1$ be parasitic admittance at node V_1. Defining the drain current of device M_1 as i_{m1} the following set of KCL equations are obtained at node V_0 and V_1

$$\begin{aligned} i_{m1} + Y_0(\omega)V_0 =& Y_s(V_s - V_0) \\ i_{m1} =& Y_1(\omega)V_1. \end{aligned} \tag{4}$$

An accurate analysis of the response of M_1 must take into account the nonlinear nature of its transconductance. The transonductance of the device is modeled through a set of g_{mk} coefficients which are given by

$$g_{mk} = \frac{1}{k!}\frac{\partial^k i_{m1}}{\partial V_0^k} \tag{5}$$

The output conductance of the transistor is also nonlinear and it is modeled using the g_{dsk} coefficients below

$$g_{dsk} = \frac{1}{k!}\frac{\partial^k i_{m1}}{\partial (V_1 - V_0)^k} \tag{6}$$

Lastly, there are 'crossover' terms that are used to describe the dependence of the transconductance on the output voltage. Those terms are defined as

$$x_{mn} = \frac{1}{m!n!}\frac{\partial^{m+n} i_{m1}}{\partial V_0^m (V_1 - V_0)^n}. \tag{7}$$

As we are most interested in the third-order intermodulation distortion performance of the circuit, the analysis that follows incorporates the above terms out to $k = 3$. When the Volterra kernels for V_0 and V_1 are solved recursively the third-order input intercept point IIP_3 of the CG circuit at voltage node V_0 and V_1 can be computed [9].

The differential output signal produced by the balun is

$$\begin{aligned} V_{out} =& V_1 - V_2 \\ =& D_1(\omega) \circ V_s + D_2(\omega_1, \omega_2) \circ V_s^2 + \\ & D_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \end{aligned} \tag{8}$$

where

$$\begin{aligned} D_1 =& [\frac{Z_L(\omega_1)(g_{m21} + g_{m31})}{1 + Z_L(\omega_1)(g_{ds31} + g_{ds21})} + \\ & \frac{g_{m1} + g_{ds1}}{g_{ds1} + Y_1(\omega_1)}]A_1(\omega_1) \end{aligned} \tag{9}$$

$$\begin{aligned} D_2 =& \frac{Z_L(\omega_1 + \omega_2)}{1 + Z_L(\omega_1 + \omega_2)(g_{ds31} + g_{ds21})} \times \\ & [(g_{m21} + g_{m31})A_2(\omega_1, \omega_2) + \\ & (g_{m22} + g_{m32})A_1(\omega_1)A_1(\omega_2) + \\ & (g_{ds32} + g_{ds22})K_1(\omega_1)K_1(\omega_2)] - \\ & A_2(\omega_1, \omega_2)\frac{Y_0(\omega_1 + \omega_2) + Y_s}{Y_1(\omega_1 + \omega_2)} \end{aligned} \tag{10}$$

$$
\begin{aligned}
D_3 = & \frac{Z_L(\omega_1+\omega_2+\omega_3)}{1+Z_L(\omega_1+\omega_2+\omega_3)(g_{ds31}+g_{ds21})}\times \\
& [(g_{m21}+g_{m31})A_3(\omega_1,\omega_2,\omega_3)+ \\
& 2(g_{m22}+g_{m32})\overline{A_1(\omega_1)A_2(\omega_2,\omega_3)}+ \\
& (g_{m23}+g_{m33})\prod_{i=1}^{3}A_1(\omega_i)+ \\
& 2(g_{ds32}+g_{ds22})\overline{K_1(\omega_1)K_2(\omega_2,\omega_3)}+ \\
& (g_{ds33}+g_{ds23})\prod_{i=1}^{3}K_1(\omega_i)]- \\
& A_3(\omega_1,\omega_2,\omega_3)\frac{Y_0(\omega_1+\omega_2+\omega_3)+Y_s}{Y_1(\omega_1+\omega_2+\omega_3)}.
\end{aligned}
\tag{11}
$$

The kernel D_3 has within itself the kernel A_3 plus other terms. Focusing on the factors that multiply A_3 in Eq. (11) we observe that

$$
\begin{aligned}
& \frac{(g_{m21}+g_{m31})Z_L(\omega_1+\omega_2+\omega_3)}{1+Z_L(\omega_1+\omega_2+\omega_3)(g_{ds31}+g_{ds21})}- \\
& \frac{Y_0(\omega_1+\omega_2+\omega_3)+Y_s}{Y_1(\omega_1+\omega_2+\omega_3)} \\
\approx & \frac{g_{m21}+g_{m31}}{R_2 \parallel \frac{1}{g_{ds21}} \parallel \frac{1}{g_{ds31}}} - \frac{j\omega(C_{gs2}+C_{gs3})+\frac{1}{R_s}}{\frac{1}{\alpha R_s}} \\
= & j\alpha R_s\omega(C_{gs2}+C_{gs3})
\end{aligned}
\tag{12}
$$

To arrive at the last expression above we approximate the admittance Y_1 as $\frac{1}{\alpha R_s}$, where α is the ratio of transconductance between the CS and CG transistors. As α increases, the voltage gain of the circuit increases and the noise figure decreases [8]. The capacitances C_{gsi} are the input capacitances of the transistors. The distortion can be reduced by varying the gate voltage bias of either M_1, M_2 or both at the same time. For practical reasons it is more convenient to change the gate voltage of only one device and leave the other fixed. In this work we chose to vary the gate voltage of M_2 (see Section III).

Examining the terms of g_{m23} and g_{m33}, the sum of these two terms can be made equal to zero at a particular bias point [10]. At that point, the distortion terms associated with $g_{m23}+g_{m33}$ will normally diminish. However, in a low-voltage environment the output conductance of the CMOS device will be highly nonlinear and there is distortion associated with $g_{ds33}+g_{ds23}$.

Biasing devices M_2 and M_3 such that $g_{m23}+g_{m33}$ is at a minimum would imply that $g_{m22}+g_{m32}$ is at a maximum, which increases distortion. Note that the sign of the terms of $g_{m23}+g_{m33}$ and $g_{ds33}+g_{ds23}$ can be made the same and the quantity $g_{m32}+g_{m33}$ is larger than $g_{ds33}+g_{ds23}$. Since $\prod_{i=1}^{3}K_1(\omega_i) \approx K_1(\omega_1)^3$, the high gain ratio at the out-of-phase output of the balun is 'amplified' by this cubic function.

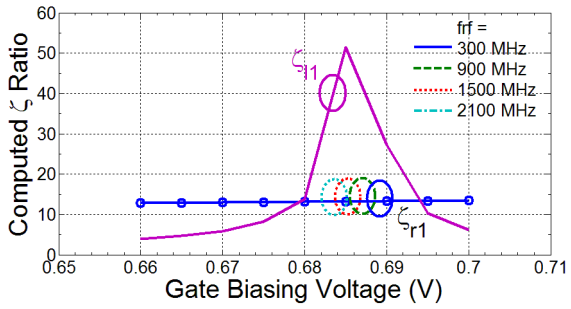


Fig. 2. Computed ζ ratio of the CG-CS active balun based on the analysis.

Using this finding the condition that must hold in order to cancel distortion in the circuit is given by the equation

$$
\zeta = \frac{g_{m23}+g_{m33}}{g_{ds23}+g_{ds33}} = \left|\frac{K_1(\omega_1)}{A_1(\omega_1)}\right|^3. \tag{13}
$$

The value of ζ is established through the bias voltages for M_2 and M_3. If we now let

$$
\zeta_{l1} = \frac{g_{m23}+g_{m33}}{g_{ds23}+g_{ds33}} \tag{14}
$$

and

$$
\zeta_{r1} = \left|\frac{K_1(\omega_1)}{A_1(\omega_1)}\right|^3 \tag{15}
$$

then Fig. 2 shows the utility of Eq.(13). The optimal biasing point for distortion cancellation is when $\zeta_{l1} = \zeta_{r1}$, which is the left-most intersection point between the two curves in the figure. The second intersection point is not useful because the the distortion terms g_{m22} and g_{m32} would be larger which means that more distortion would be produced at that bias point, not less.

III. Experimental Results

The active balun-amplifier circuit was fabricated and measured to verify the analysis presented in the previous section. Extensive two-tone tests were carried out to determine the IIP_3 of the circuit. The two-tone tests were done at different gate bias voltages of the transistor M_2 and also at different frequencies. The gate-source bias voltage of M_3 was kept fixed at a relatively low value.

The measured and simulated IIP_3 is plotted in Fig. 3 versus the gate bias of M_2. The measured results show that an optimal IIP_3 point when M_2 is biased around 0.69 V while the simulated results predict the optimal value to be 0.74 V, a discrepancy of only 7.2%.

The measured and simulated voltage gain, noise figure (NF) and the input reflection coefficient of the active balun circuit are plotted together and shown in Fig. 4.

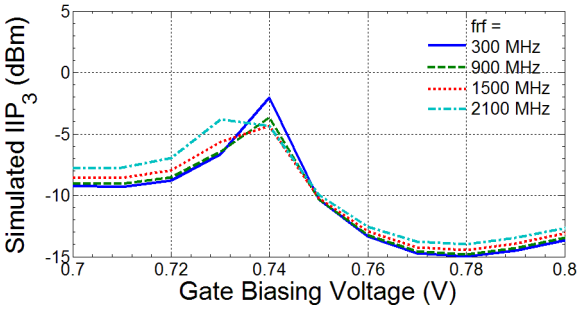
The average voltage gain of the circuit is 16.2 dB over the frequency band 0.3−2.4 GHz. The NF has an average value of 4.0 dB and reaches a minimum of 3.2 dB at 1.1 GHz. The NF increases towards the lower end of the band due to 1/f noise and losses in the off-chip components, particularly the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

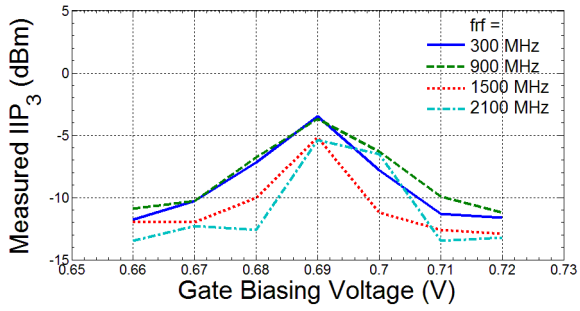
		This work	[1]	[8]	[11]	[2]
DC supply voltage	(V)	0.9	1.8	1.2	1.8	1.0
Frequency range	(GHz)	0.5−2.4	TV Band#	0.2−5.2	0.05−0.86	3.5−6.0
Gain	(dB)	16.2	18.0	15.6	15.0	6.8
Noise figure (NF)	(dB)	≤4.0	2.5−3.0	≤3.5	4.2	4.4
Maximum IIP_3	(dBm)	−3.8	−0.5	≥0.0	2.6	4.0
Phase imbalance	(deg)	10.0†	-	≤2.0	-	≤7.0
Gain imbalance	(dB)	2.0†	-	≤0.7	-	≤1.4
Power consumption	(mW)	15.8	30.0	14.0	10.0	15.0
CMOS node		130 nm	130 nm	65 nm	180 nm	180 nm

#up to 800 MHz.

†average



(a) Simulated



(b) Measured

Fig. 3. IIP_3 of the CG-CS active balun.

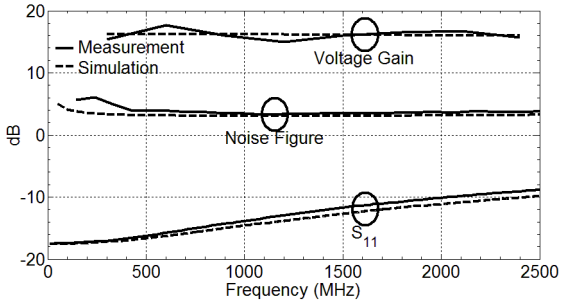


Fig. 4. Measured and simulated S_{11}, noise figure, and the voltage gain vs. RF frequency.

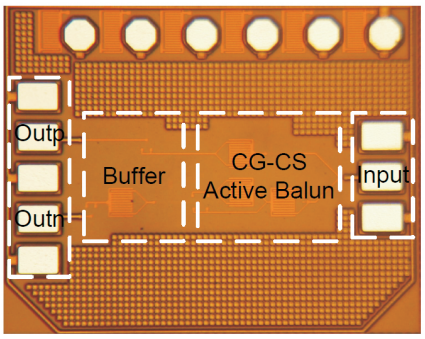


Fig. 5. Chip microphotograph.

bias-T that was used. The input reflection coefficient is better than −10 dB up to 2.1 GHz and gradually increases to −8.5 dB at 2.4 GHz.

The phase and gain imbalances of the active balun-amplifier were also measured and they are in the range of 10° and 2 dB, respectively. A microphotograph of the chip is shown in Fig. 5 and a performance comparison with similar works in presented in Table I.

IV. CONCLUSION

Active baluns must be designed for high IIP_3 so that they do not compromise the linearity of the circuits that follow it in a receiver chain. It is difficult to obtain a high IIP_3 for any active circuit in a low supply-voltage environment and extra care must be taken in the case of active baluns. This paper explored some of the nonlinear phenomema that directly influence the linearity of an active balun-amplifier using the CG-CS topology through a Volterra series analysis.

V. ACKNOWLEDGMENTS

This work was supported, in part, by a grant from the Natural Sciences and Engineering Research Council of Canada. The authors would like to thank CMC Microsystems, Kingston, Ontario, Canada, for access to chip fabrication services.

REFERENCES

[1] D. Im, I. Nam, and K. Lee, "A CMOS Active Feedback Balun-LNA With High IIP2 for Wideband Digital TV Receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 12, pp. 3566–3579, Dec. 2010.

[2] S.-Y. Lee and C.-C. Lai, "A 1-V Wideband Low-Power CMOS Active Differential Power Splitter for Wireless Communication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 8, pp. 1593–1600, Aug. 2007.

[3] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi, "An 800-MHz to 6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[4] K. Jung, W. Eisenstadt, R. Fox, A. Ogden, and J. Yoon, "Broadband Active Balun Using Combined Cascode-Cascade Configuration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 8, pp. 1790–1796, Aug. 2008.

[5] B. Jackson and C. Saavedra, "A CMOS Ku-Band 4x Subharmonic Mixer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1351–1359, June 2008.

[6] C. Saavedra and B. Jackson, "Voltage-variable attenuator MMIC using phase cancellation," *IEE Proceedings−Circuits, Devices and Systems*, vol. 153, no. 5, pp. 442–446, Oct. 2006.

[7] W.-H. Chen, G. Liu, B. Zdravko, and A. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[8] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, June 2008.

[9] V. Aparin and L. Larson, "Modified derivative superposition method for linearizing fet low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 571 –581, feb. 2005.

[10] T. Weldon, D. Lieu, and M. Davis, "Experimental results at one GHz on linearizing an nMOS transistor with a parallel pMOS transistor," in *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, June 2005, pp. 233–236.

[11] K. Han, L. Zou, Y. Liao, H. Min, and Z. Tang, "A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2008, pp. 457–460.