2-Watt Broadband GaN Power Amplifier RFIC using the f_T Doubling Technique

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***Abstract*— A broadband power amplifier (PA) is reported using the f_t doubling technique which delivers more than 2 W of saturated output power over a span of 6 GHz. The PA exhibits a power gain of 12.2 ± 0.2 dB over its operating frequency range, yielding a gain-bandwidth product of more than 1.5 f_t. The PA has an OP_{1dB} and an OIP_3 of more than 31 dBm and 40 dBm respectively. The IC was fabricated using a 0.8-μm GaN process and the core circuit occupies an area of 925 μm X 895 μm.**

I. INTRODUCTION

Often, in circuit design, maximizing one performance metric of the circuit can have an adverse impact on some of the other metrics and vice-versa. Which metric will take precedence and drive the design process is determined by the circuit's end-use. For power amplifiers (PA's) the metrics that are often at odds are power efficiency on one side and linearity and broadband performance on the other. PA's that use class E and F topologies have excellent power efficiency [1], [2] and are attractive for mobile phones, for example, because they are battery-operated. Meanwhile, in cases where linearity and broadband performance are paramount then the class A topology is a suitable choice [3], [4] if there is enough dc power available and if proper measures are taken to dissipate the excess heat. Applications that can benefit from class A PA's include high-performance test equipment and cellular base stations that must handle large numbers of simultaneous phone calls.

This paper describes the design, test and measurement of a broadband fully-integrated class-A PA delivering 33 dBm of saturated output power over a span of 6 GHz. The PA exhibits a power gain of 12.2 ± 0.2 dB over its operating frequency range, it has an OP_{1dB} of 31.3 dBm, an OIP3 of 40.8 dBm and a drain efficiency of 30.4 %. The broadband response was obtained by using a circuit design technique called 'f_T doubling' [5]–[7] and by applying shunt-shunt feedback to the amplifier.

II. POWER AMPLIFIER CIRCUIT

A circuit schematic of the proposed power amplifier is shown in Fig. 1. Transistors M_1 and M_2 form the f_T doubler configuration. It uses a modified Darlington stage, where the common-drain device M_1 drives the common-source device M_2 through a load network consisting of a resistor R_S in series with an inductor L_S. The load network at the source of M_1 is designed so that the input signal RF_{IN} splits equally between M_1 and M_2 through voltage division. The capacitor C_B and resistor R_B are used for AC-coupling the source of M_1 to the gate of M_2. Since devices M_1 and M_2 have the same gate width, each device contributes an equal amount of RF current and power at the output. It can be shown that if $R_S \approx 1/g_m$ and $L_S \approx R_g C_{gs}/g_m$, where R_g is the parasitic gate resistance, C_{gs} is the gate-source parasitic capacitance and g_m is the transconductance of each device, then the input voltage is split equally between M_1 and M_2 over a wide frequency range [5]. The inductor L_S is necessary to achieve equal voltage and power distribution for high frequencies approaching $\omega = 1/R_g C_{gs}$. This ensures a flat gain, output power and linearity over a broad frequency range. With the same voltage applied across each device, the current gain of the f_T doubler stage can be evaluated as $H_{21} = 2\omega_T/j\omega$ where $\omega_T = 2\pi f_T$. The current gain is unity at $\omega = 2\omega_T$, thus the bandwidth can be improved considerably compared to a conventional common-source stage [5], [6]. The source loading consisting of R_S and L_S also improves stability of the f_T doubler. The input impedance can be shown to be [5]:

$$Z_{in} = 2R_g + \frac{2}{j\omega C_{gs}}, \tag{1}$$

which does not include a negative resistance as found in conventional Darlington amplifiers.

After reducing the effective input capacitance due to the gate-source capacitance C_{gs}, the parasitic gate-drain C_{gd} capacitance can have a significant effect on the amplifier's gain and output power at high frequencies. Device M_3 is stacked above M_1 to allow for different drain voltages to be used for M_1 and M_2 by changing the channel resistance of M_3 through its gate bias voltage, $\mathrm{V}_{\mathrm{GAC}}$. Shunt-shunt resistor-capacitor (R_F, C_F) feedback is employed to obtain a wideband input and output impedance match to 50Ω.

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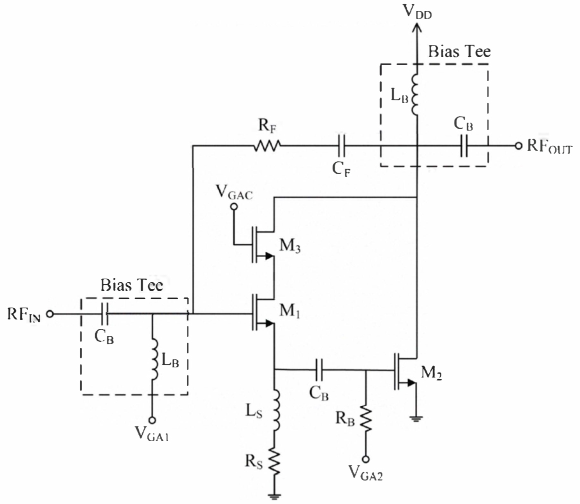

Fig. 1. Circuit schematic of the proposed power amplifier.

TABLE I
SUMMARY OF COMPONENT VALUES FOR THE PA

(W/L)$_{1,2,3}$	L_S	R_S	R_F	R_B	C_F	C_B
600/0.8	0.3 nH	8 Ω	255 Ω	1.2 kΩ	2.5 pF	6 pF

It also helps in achieving a flat gain and unconditional stability across the frequency band.

Table I summarizes the transistor gate dimensions, inductor values, capacitor values and resistor values used in the design of the PA. All of these devices are integrated on-chip, using thin-film nichrome resistors, metal-insulator-metal (MIM) capacitors and spiral inductors.

III. EXPERIMENTAL RESULTS

The PA was fabricated using a 0.8μm GaN HFET process at Canadian Photonics Fabrication Centre in Ottawa, Ontario. The GaN HFETs are processed on semi-insulating SiC substrates. A photograph of the IC is shown in Fig. 2. It occupies an area of 1.38mm^2 including bonding pads and decoupling capacitors, while the core circuit area is 925$\times$895μm^2. The drain supply voltage is 20 V.

The broadband PA was measured directly on-wafer using 40GHz coplanar waveguide (CPW) probes and DC probes. External bias tees were used at the PA input and output (Fig. 1). A preamplifier and an attenuator were used at the input and output respectively to avoid operating the signal generator and spectrum analyzer at excessively high power levels.

Fig. 3 shows the measured saturated output power (P_{SAT}) and output 1 dB compression point (OP_{1dB}) from 1 GHz to 6 GHz. The saturated output power is flat over the frequency band with a mean value of 33.0 dBm and a variation of less than ± 0.8 dBm. The measured OP_{1dB} is higher than 30 dBm over the entire bandwidth, reaching a maximum value of 32 dBm. The mean value is 31.3 dBm and the variation is less than ± 1 dBm from 1 GHz to 6 GHz. The output two-tone third-order intermodulation intercept point (OIP3) was also measured and the results are shown in Fig. 4. It is clear that the OIP3 is above 41 dBm from 1 GHz to 4.5 GHz. Past 4.5 GHz, the measured OIP3 drops slightly to 37.5 dBm at 6 GHz. Overall, the mean OIP3 across the band is 40.8 dBm.

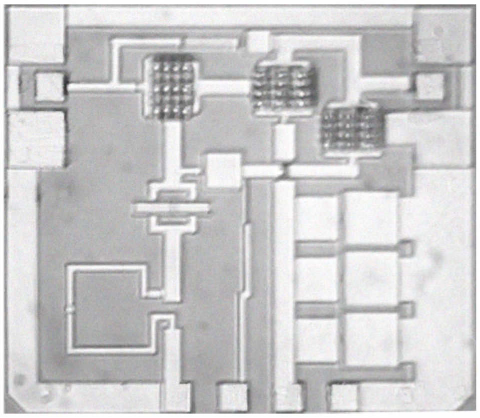

Fig. 2. Photograph of the broadband PA IC.

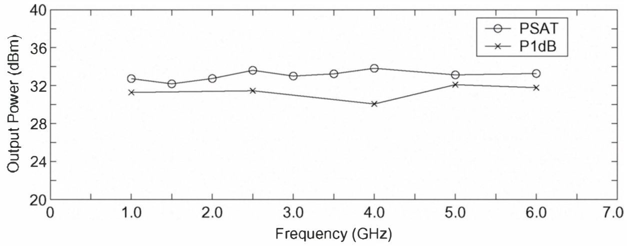

Fig. 3. Measured output P_{SAT} and P_{1dB} from 1 GHz to 6 GHz.

The complete input and output power transfer characteristic of the PA is shown in Fig. 5, Fig. 6 and Fig. 7 for 2.5 GHz, 4 GHz and 6 GHz respectively. The measured drain efficiency is also shown at different input and output power levels. These plots indicate that the linear power gain remains around 12 dB out to 6 GHz, and that the drain efficiency can be as high as 37% in saturation. Fig. 8 shows a plot of the PA's power gain from 1 GHz to 6

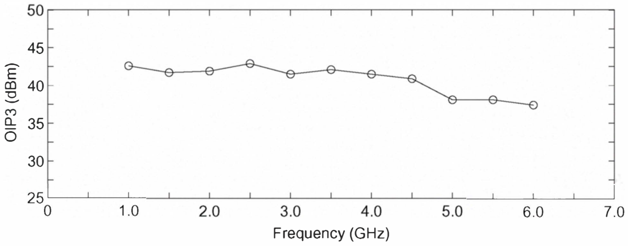

Fig. 4. Measured OIP3 from 1 GHz to 6 GHz.

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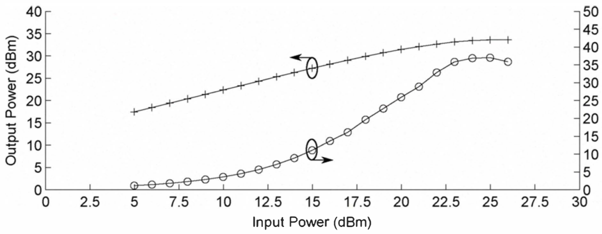

Fig. 5. Measured output power and efficiency vs. input power at 2.5 GHz.

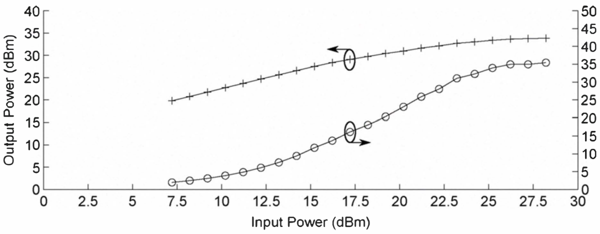

Fig. 6. Measured output power and efficiency vs. input power at 4 GHz.

GHz. It is clear that the gain is very flat out to 6 GHz with a mean value of 12.2 dB and a small variation of ± 0.2 dB. This gives a gain-bandwidth product exceeding 24 GHz, which is a factor of 1.5 higher than the unity current-gain frequency f_T of the devices. Fig. 9 is a plot of the amplifier's drain efficiency at saturation from 1 GHz to 6 GHz. The efficiency reaches a maximum 37 % and remains over 24 % out to 6 GHz, giving a mean value of about 30.4 % over the band.

Table II summarizes this work's peformance.

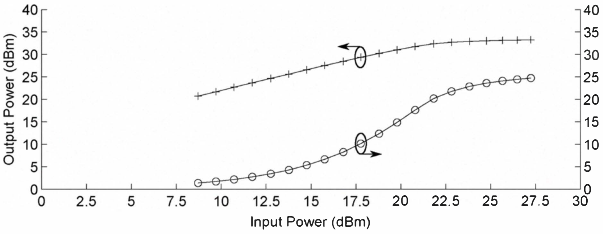

Fig. 7. Measured output power and efficiency vs. input power at 6 GHz.

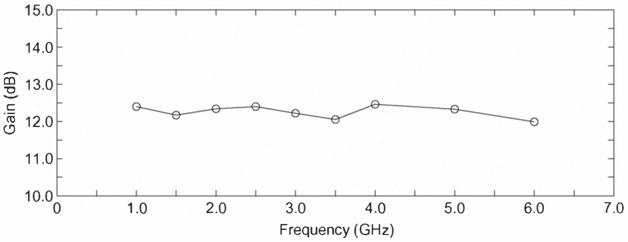

Fig. 8. Measured Gain from 1 GHz to 6 GHz.

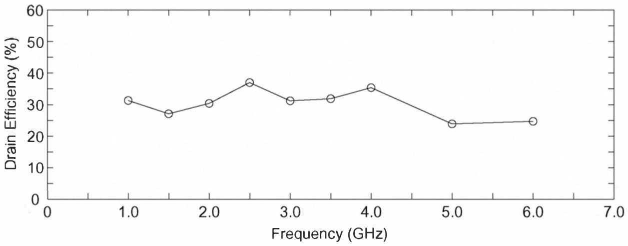

Fig. 9. Measured efficiency at P_{SAT} from 1 GHz to 6 GHz.

TABLE II

SUMMARY OF BROADBAND PA CHARACTERISTICS

Characteristic	Result
Technology	0.8 μm GaN/SiC
Circuit Area	0.83 mm^2
Bandwidth	1–6GHz
Output Power	33 ± 0.8 dBm
Gain	12.2 ± 0.2 dB
1 dB compression	31 dBm
Third-order intercept	40 dBm
Efficiency	Max: 37%

IV. CONCLUSIONS

A new broadband linear power amplifier (PA) has been developed using the f_T doubling technique. It provides more than 2 W of saturated output power and exhibits a flat power gain of 12.2 ± 0.2 dB out to 6 GHz. It also features a high linearity with $OP_{1dB} > 31$ dBm and OIP3 > 40 dBm. The PA was fabricated in 0.8-μm GaN with a low f_T of 16 GHz, thus its gain-bandwidth product is more than 1.5 f_T. It occupies an area of 925μm×895μm.

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