A 3-10 GHz 13 pJ/pulse Dual BPSK/QPSK Pulse Modulator Based on Harmonic Injection Locking

Ahmed M. El-Gabaly* and Carlos E. Saavedra†

*Formerly with Queen's University and now with Peraso Technologies Inc., Toronto, ON, Canada M5J 2L7
†Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada K7L 3N6

***Abstract*—We present a new method to phase-modulate RF pulses through injection locking. The modulator can produce BPSK or QPSK modulated pulses over a frequency span of 3 to 10 GHz. The RF pulses are produced using a fast on/off switching technique to power up and power down a tunable ring oscillator. Experiments show that the modulator's energy consumption ranges from 13 pJ/pulse to 18 pJ/pulse as the carrier frequency varies from 3 GHz to 10 GHz. The energy consumption figures are for 2 ns long pulses with amplitudes of 300 mV at 3 GHz and 200 mV at 10 GHz. The pulse repetition rate is 250 MHz. The chip was fabricated in 130 nm CMOS and the core circuit area is only 0.05 mm^2.**

***Index Terms*—Injection locking, impulse radio, RF pulse modulation, BPSK, QPSK, ring oscillators, CMOS RFIC's.**

I. Introduction

Injection locked oscillators are regularly used in RF systems to carry out functions such as quadrature signal generation, frequency division and beam scanning in antenna arrays [1]–[3]. The competitive advantages of injection locking are its minimal area requirements and energy efficiency. Injection locking can also be used to phase-modulate a carrier. Prior art on injection locked modulators have used active antennas on printed circuit boards [4] or optoelectronic circuits [5], which are not directly applicable to CMOS RFICs. In addition, prior works have focused only on continuous wave modulation.

This paper breaks new ground by showing how to use harmonic injection locking to produce short duration RF pulses over a $3-10$ GHz span that are also digitally phase modulated. The proposed circuit can yield RF pulses with either BPSK or QPSK modulation format, thus making it versatile, power efficient and physically compact. The circuit employs a quadrature ring oscillator that is switched on and off to generate the pulses. By injecting brief current impulses at specific places in the ring structure to kick-start the oscillations, the RF pulses have a consistent phase angle relative to the system clock signal and it is this phenomenon that we exploit to generate BPSK/QPSK modulation. To demonstrate the concept we designed and tested a chip fabricated using a standard 130 nm CMOS process. It can yield BPSK/QPSK modulated pulses of 2 ns duration while consuming only 13 pJ/pulse and 18 pJ/pulse of energy at 3 GHz and 10 GHz respectively.

The proposed pulse modulator is well suited for biotelemetry [6], [7] where low power and compact die area are critical. Interchip communications [8], [9] is another application where pulse modulation is actively investigated for high data rates.

II. Pulse Modulator Description

A circuit diagram of the $3-10$ GHz pulse modulator is shown in Fig. 1. The quadrature ring oscillator and the output buffers are simultaneously pulsed on and off using a clock signal (CLK). The carrier frequency can be varied using two control voltages: V_C and V_{CF} for coarse and fine tuning, respectively. The ring oscillator is stabilized through injection locking to a harmonic of the system clock signal. The injection locking circuits (ILCs) accept complementary clock signals, $\mathrm{CLK}_{I\pm}$ and $\mathrm{CLK}_{Q\pm}$, and they are used to modulate the output pulses. A startup network is used to produce four clock signals, $\mathrm{CLK}_{I\pm}$ and $\mathrm{CLK}_{Q\pm}$, in a time sequence determined by the input data bits, b_0 and b_1, which modulate the carrier pulses. If both bits are used for data, then QPSK modulation is produced and if only one bit is used then BPSK modulation is produced. This modulator does not need passive phase shifting or power splitting/combining structures thus occupying a small area.

A ring oscillator was selected in this design due to its small area and wide frequency tuning range [10]. Its comparatively high phase noise can be mitigated by injection locking to a stable source [1], [11]. Each delay stage in the ring oscillator has two CMOS inverters in a differential arrangement. Delay and thus frequency tuning is achieved by varying the bias current of the CMOS inverters. The ILCs in Fig. 1 each have two inverters in a self-reinforcing loop as shown in Fig. 2. The PMOS and NMOS devices in the latch have been drawn as cross-coupled pairs. The bias currents on the left and right hand side of latch are controlled by clock signals $\mathrm{CLK}_{\mathrm{I}+}$ and $\mathrm{CLK}_{\mathrm{I}-}$, respectively. $\mathrm{CLK}_{\mathrm{Q}+}$ and $\mathrm{CLK}_{\mathrm{Q}-}$ control the latch bias currents on the second delay cell.

To produce very short-duration pulses the oscillator must turn on quickly. The circuit schematic of the fast startup network, which is also used for modulation, is depicted in Fig. 3. Current-starved inverters split the clock signal CLK into two signals CLK+ and CLK- with a very short time delay between them, on the order of tens of picoseconds. Four multiplexers T_1–T_2, T_3–T_4, T_5–T_6 and T_7–T_8 are employed to route CLK+ and CLK- to CLK_{I+}, CLK_{I-}, CLK_{Q+} and CLK_{Q-}, which are used in the ILCs. If data bit b_0=1, the multiplexers will pass CLK+ and CLK- through to CLK_{I+} and CLK_{I-}, respectively. Conversely, if b_0=0 then CLK+ and CLK- are passed on to CLK_{I-} and CLK_{I+}, respectively. A similar process occurs with the quadrature clock signals, CLK_{Q+} and CLK_{Q-}, when data bit b_1 changes from 1 to 0.

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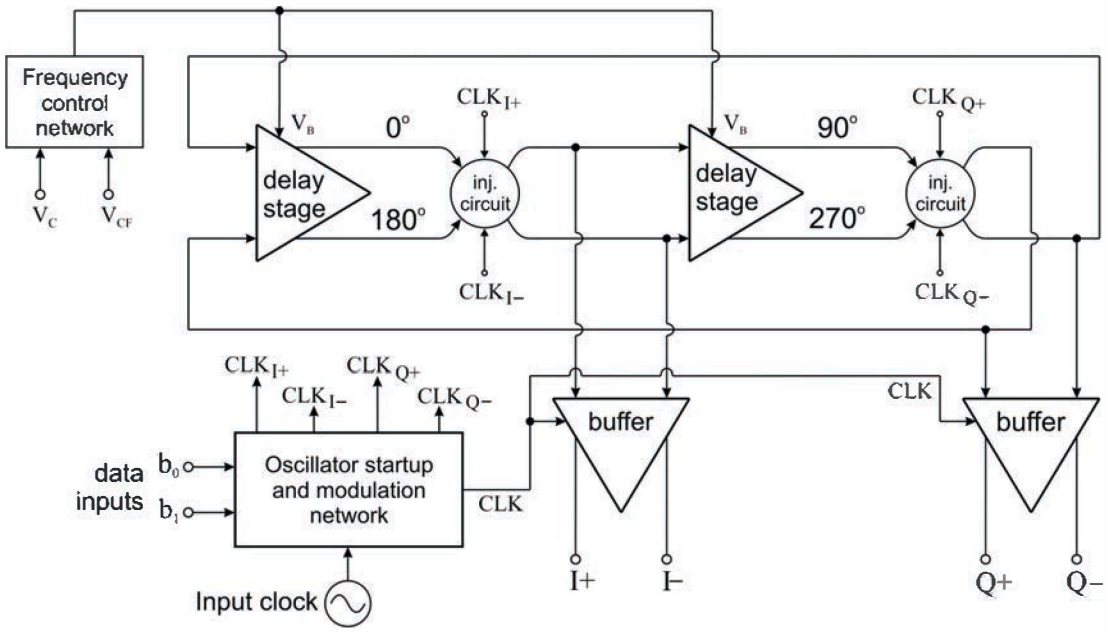

Fig. 1. Block diagram of the dual BPSK and QPSK pulse modulator.

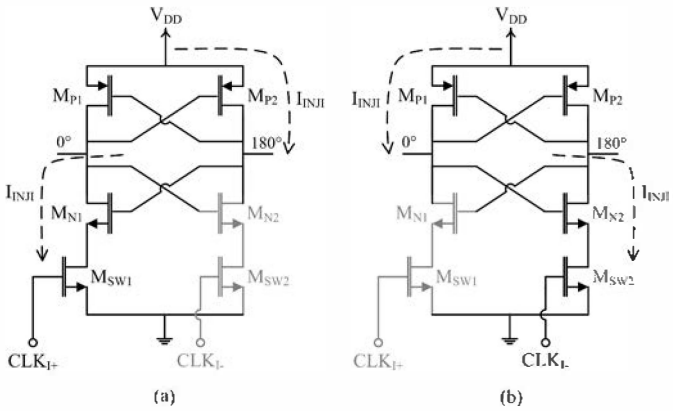

Fig. 2. ILC schematic and injected current flow when (a) b_0=1 and (b) b_0=0.

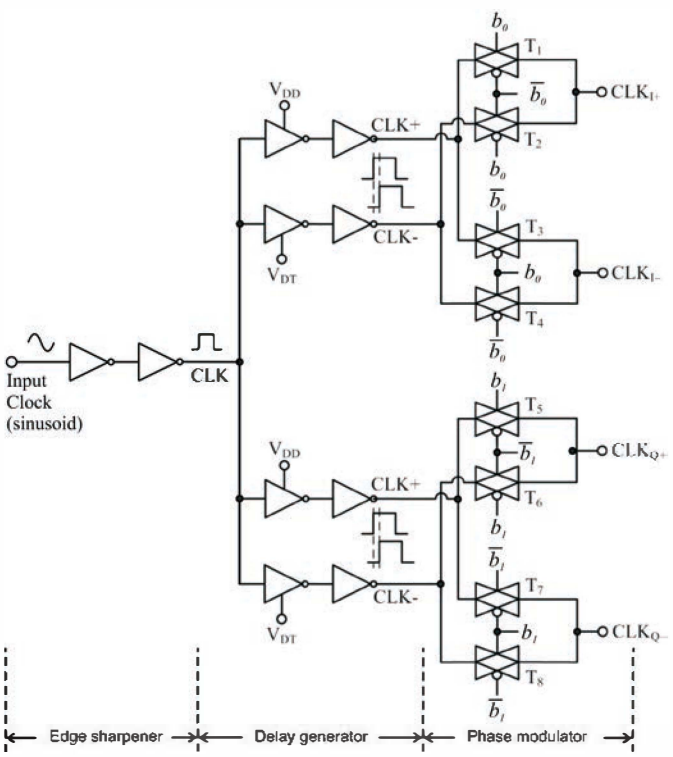

Fig. 3. Circuit schematic of the startup and modulation network.

The bias currents of the cross-coupled pairs in the ILCs are switched on and off using a pair of NMOS switches M_{SW1}–M_{SW2} as shown in Fig. 2. By turning on one side just before the other, say switching on M_{SW1} before M_{SW2}, an initial current I_{INJI} flows for a short time through the oscillator nodes as shown in Fig. 2. In effect, a current impulse is injected at the oscillator nodes, which quickly starts up the oscillations. It also sets the initial phase of the oscillations at the turn-on instant. By setting the same initial oscillation phase at each clock rising edge, the pulses are phase coherent with the input clock and pulse-to-pulse coherency is maintained. The triggering order of switches M_{SW1} and M_{SW2} determines the direction of the injected current impulse I_{INJI} as illustrated in Fig. 2. If data bit b_0=1, switch M_{SW1} activates before M_{SW2}. If b_0=0 switch M_{SW2} activates before M_{SW1}, reversing the direction of the injected current I_{INJI}. A similar process occurs in the second ILC for the quadrature (Q) signal path and is controlled by data bit b_1. In sum, the data bits b_0 and b_1 determine the direction of the injected current impulses $I_{INJI,Q}$ and the oscillation phase takes on one of four quadrature values to implement quadrature modulation. The current injection method depicted in Fig. 2 can also be used in systems that operate up to 24 GHz and beyond [12].

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III. Experimental Results

The pulse modulator was fabricated using a 0.13 μm CMOS process and a photograph of the RFIC is shown in Fig. 4. The chip has an area of 0.85 mm^2 including bonding pads and decoupling capacitors while the core circuit area measures 0.050 mm^2. Chip measurements were carried out on-wafer using a spectrum analyzer (PSA) and a digital sampling oscilloscope (DSA) to observe the output signal in the frequency and time domains, respectively.

The ring oscillator's free-running frequency can be tuned from 3.15 GHz to 10.07 GHz as the control voltage V_C of the delay stages is varied from 0.58 V to 0.93 V. The free-running output power level is about -6.2 dBm at 3.15 GHz, -8.3 dBm at 6.1 GHz and -10.5 dBm at 10.07 GHz.

The oscillator was characterized in pulsed mode using a 250 MHz clock. Figs. 5a and 5b show the oscillator's output spectra at two different center frequencies: 3.75 GHz and 10.25 GHz, respectively. As expected, the power spectrum exhibits peaks at multiples of the clock frequency and those harmonics of the clock are coherent and well-defined.

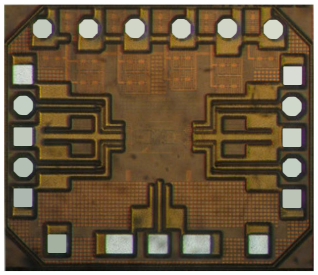
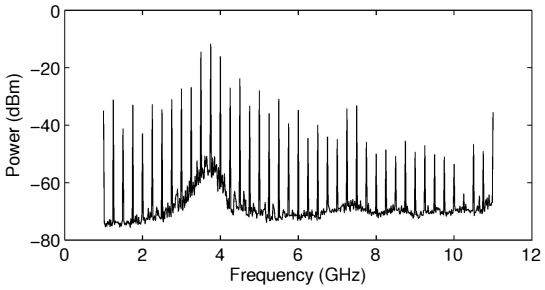
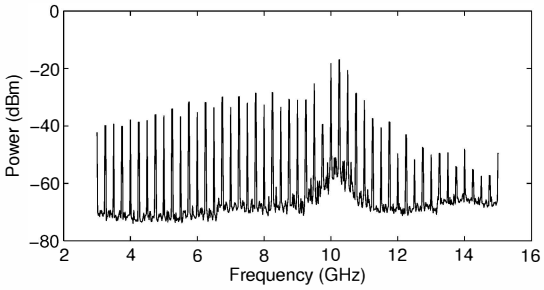


Fig. 4. Photograph of pulse modulator IC.



(a)



(b)

Fig. 5. Pulsed output spectrum at (a) 3.75 GHz and (b) 10.25 GHz.

Fig. 6 shows the measured phase noise (PN) of the generated pulsed output at 10.25 GHz (i.e. the spectral peak at 10.25 GHz in Fig. 5b) plus the measured PN of the 250 MHz clock reference. Basic noise theory predicts that the n^{th} harmonic tone of a periodic signal will have a PN that is higher than the PN of the fundamental tone by the amount

$$20\log(n)\ \text{dB} \tag{1}$$

Considering that pulsing the ring oscillator causes it to become injection-locked to the nth harmonic of the clock signal, we expect that the oscillator's PN will track the PN of the clock signal but offset by the amount given in (1). This prediction is borne out by the plot in Fig. 6, as the measured output phase noise at 10.25 GHz is 33 dB higher than that of the 250 MHz clock reference (n = 10.25/0.25 = 41). A similar result was seen at 3.75 GHz where the output phase noise is 24 dB higher than that of the clock (n = 3.75/0.25 = 15). Altogether, the integrated RMS jitter from 100 Hz to 10 MHz is less than 3.6 ps.

Fig. 7 shows the measured pulsed output in the time-domain at 3.75 GHz and 10.25 GHz with the 250 MHz input clock. It is clear that the oscillations settle within 1 ns from the turn-on instant for all frequency bands. Considering that the DSA is an equivalent time sampling oscilloscope, it samples the signal only once per trigger event. The DSA is thus triggered using the input clock for these measurements. Since the 3.75

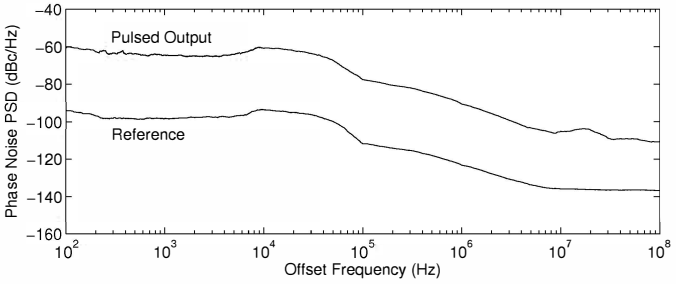
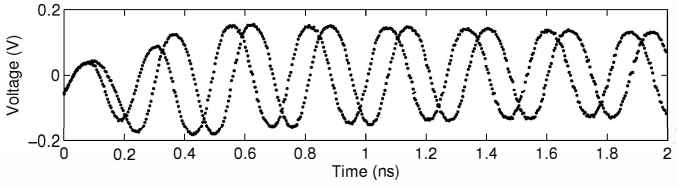
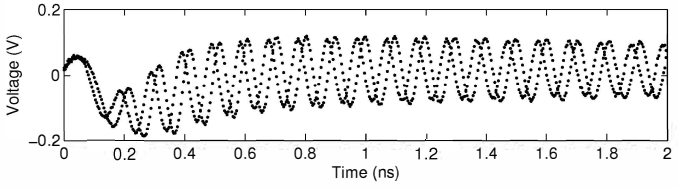


Fig. 6. Phase noise of pulsed output at 10.25 GHz.



(a)



(b)

Fig. 7. Pulsed time-domain I+ and Q+ outputs at (a) 3.75 and (b) 10.25 GHz.

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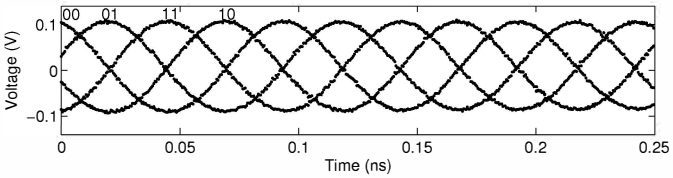

Fig. 8. Pulsed time-domain I+ output for the four data patterns and phase states at 10.25 GHz.

TABLE I
SUMMARY OF PULSE MODULATOR'S PERFORMANCE

Characteristic	**This work**	[13]	[14]
CMOS Process	**0.13 μm**	90 nm	0.18 μm
Frequency (GHz)	**3–10**	3–5	6–10
PRF (MHz)	**250**	500	750
Energy (pJ/p)	**13–18**	56	12
Amplitude (mV)	**300–200**	200	30
Duration (ns)	**2.0**	2.0	0.5
Modulation	**BPSK & QPSK**	BPSK-PPM	BPSK

GHz and 10.25 GHz cycles are clearly visible, the generated pulsed oscillations are indeed coherent with the input clock, and thus pulse-to-pulse coherency is maintained. Furthermore, Fig. 8 illustrates the quadrature signaling capability of the pulsed oscillator at 10.25 GHz, with the four time-domain measurements superimposed, one for each phase state. Phases 0°, 90°, 180° and 270° correspond to the input data patterns (b_0b_1) of 00, 10, 11 and 01 respectively. Similar results were observed at 3.75 GHz. A good quadrature phase shift of approximately 90° $\pm$ 3° is attained between phase states over the 3 GHz to 10 GHz band.

When the system is pulsed with a 250 MHz clock signal the average power consumption P_{AVG} is about 13 mW at 3 GHz and 18 mW at 10 GHz. The energy consumption per pulse, E_p, can be calculated using the expression

$$E_p = \frac{P_{AVG}}{PRF \times 4} \tag{2}$$

where PRF is pulse repetition frequency. Therefore the energy consumption per pulse is less than 13.0 pJ at 3 GHz and 18 pJ at 10 GHz.

Table I summarizes the proposed pulse modulator's performance. It offers QPSK pulse modulation and a high energy efficiency (output voltage per energy consumed).

IV. CONCLUSION

A new 3–10 GHz short-pulse phase modulator based on harmonic injection locking has been developed in 130 nm CMOS. The generated pulses settle within 1 ns and are phase locked to the input clock for coherence. Direct QPSK modulation was demonstrated from 3 GHz to 10 GHz, and a low energy consumption of 13 pJ/pulse and 18 pJ/pulse was achieved at 3 GHz and 10 GHz respectively. The circuit has an active area of only 0.05 mm^2.

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