

A Decade-Bandwidth Low-Noise Mixer RFIC with a Distortion-Canceling Output Amplifier

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Abstract—This paper presents a 1-10 GHz low-noise down-convert mixer RFIC suitable for wideband receivers. A switched transconductor mixing core is adopted to reduce noise at high frequencies. By adding a series inductor to the RF transconductor, a flat 4-5 dB noise figure (NF) and a high gain of 26.5 dB can be achieved over a broad bandwidth out to 10 GHz. A CMOS output amplifier is also integrated on-chip, employing derivative superposition (DS) for high linearity and an OIP3 of 16.5 dBm. The circuit consumes less than 20 mW of dc power and occupies an active chip area of less than 0.2 mm².

I. INTRODUCTION

Several topologies exist for wideband low-noise mixing [1]–[5]. Among the most recent and effective approaches are those based on noise canceling. Noise canceling configurations inherently provide some degree of distortion cancellation as well. Derivative superposition (DS) [6]–[10] has also been utilized in mixers for significant distortion cancellation and a high third-order intercept point (IP3). Nevertheless, the operation frequencies of noise-canceling mixers have been mostly limited to about 5 or 6 GHz. This is primarily because the auxiliary amplifiers used for noise canceling start to contribute significant noise themselves at higher frequencies. The auxiliary amplifiers' signal gain can be relatively low at high frequencies due to their limited bandwidth, thus making their own input-referred noise considerable.

This paper presents a low-noise down-convert mixer RFIC in 130 nm CMOS, operating over a decade of frequency bandwidth from 1 GHz to 10 GHz. A switched transconductor topology is employed with series inductive peaking to achieve a 4-5 dB noise figure (NF) as well as a high gain of 26 dB out to 10 GHz. A CMOS output amplifier is also integrated on-chip, incorporating a new DS technique to realize a high output IP3 (OIP3) of 16.5 dBm. Applying DS at the output of the mixer as opposed to its input allows for optimized bandwidth and NF. The chip consumes less than 20 mW of dc power and occupies an active area of less than 0.2 mm².

II. CIRCUIT DESCRIPTION

A. The Mixing Core

A circuit schematic of the proposed mixing circuit is shown in Fig. 1. A switched transconductor topology [11] is employed to provide low noise performance over a wide bandwidth out to 10 GHz. It consists of three parts: low-noise RF transconductors ($M_1 - M_2$, $M_3 - M_4$), large-swing LO

switches ($M_5 - M_6$, $M_7 - M_8$) and high-impedance IF active loads ($M_9 - M_{10}$). The outputs of the LO buffers are ac-coupled to the source terminals of the RF transconductors. This separates the dc bias current of the RF transconductors from that of the LO buffers, allowing for optimized noise performance and enhanced drive capability respectively.

The RF differential pairs $M_1 - M_2$, $M_3 - M_4$ are biased in moderate inversion with a low dc bias current ($I_{DS} \approx 200 \mu\text{A}$) to reduce their $1/f$ noise. To compensate for the lower transconductance (g_m) in moderate inversion, and to reduce their noise contribution, the width of $M_1 - M_2$, $M_3 - M_4$ is made relatively large ($W = 80 \mu\text{m}$). However a larger device implies higher gate parasitic capacitances (C_{GS}) diminishing the increase in gain and deteriorating the NF at high frequencies. To mitigate this effect, inductors L_G are connected in series with the gates of $M_1 - M_2$, $M_3 - M_4$ to absorb their parasitic capacitance and widen the bandwidth. By considering the differential-mode half-circuit of $M_1 - M_2$ and L_G , where the transistor is modelled by g_m , C_{GS} and the drain-source noise current i_{ND}^2 , the effective transconductance (G_M) and thus the input-referred noise voltage (v_{NI}^2) of $M_1 - M_2$ can be approximated as:

$$G_M \approx \frac{g_m}{1 - \omega^2 C_{GS} L_G} \quad (1)$$

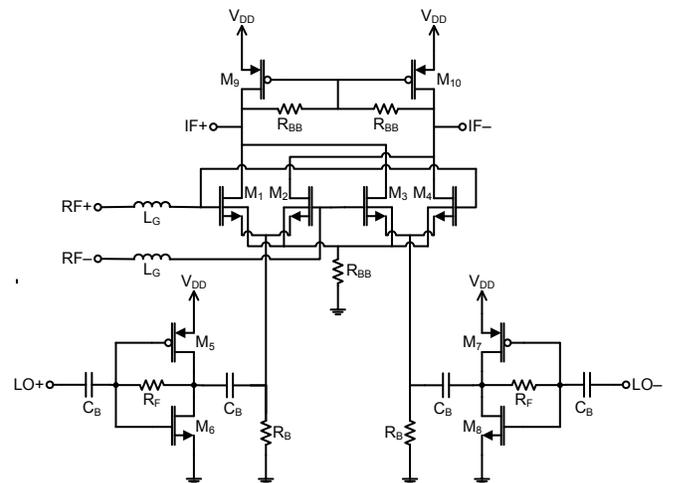
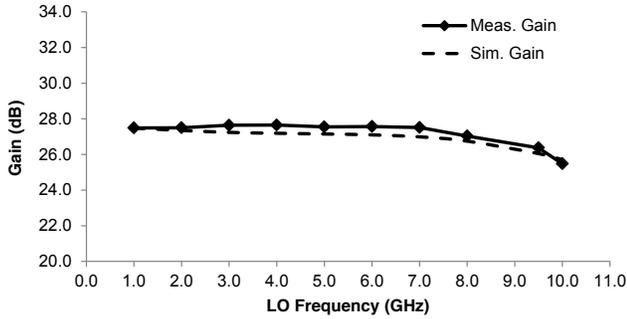
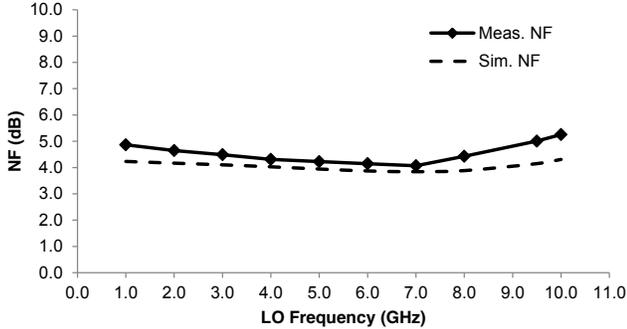


Fig. 1. Circuit schematic of the proposed mixer



(a)



(b)

Fig. 4. Mixer performance over LO frequency: (a) gain and (b) NF.

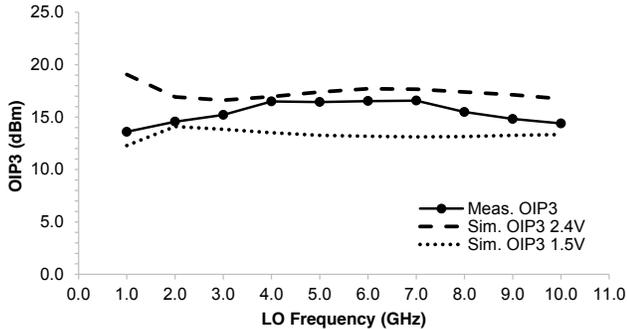


Fig. 5. Measured mixer OIP3 performance.

4.6 ± 0.6 dB are achieved from 1 GHz to 10 GHz. The NF is as low as 4.0 dB at 7 GHz. These results demonstrate that the mixer's 3-dB bandwidth exceeds 10 GHz. The DSB NF was also verified over a broad range of IF frequencies from 5 MHz to 500 MHz. The NF is below 6 dB down to an IF frequency of 5 MHz, indicating low $1/f$ noise.

The OIP3 and output 1-dB compression (OP1dB) points were characterized from 1 GHz to 10 GHz. For these measurements, the IF frequency was fixed at 200 MHz. The frequency spacing between the two tones for the OIP3 measurement was 10 MHz. Fig. 5 is a plot of the measured and simulated OIP3 versus LO frequency. The OIP3 peaks to 16.5 dBm at the center of the band, but drops to 14.4 dBm towards the edges. The simulated OIP3 without distortion cancellation (i.e. $V_{IFB} = 1.5V$ in the IF amplifier), is also shown in Fig. 5. Meanwhile, the mixer's OP1dB (not shown) ranged between

TABLE I
SUMMARY OF THE MIXER'S PERFORMANCE

Characteristic	This work	[3]	[8]	[5]
Chip Area (mm ²)	0.2	0.315	0.10	1.21
DC Power (mW)	20	34.5	20	25.5
Gain (dB)	26.5	17.5	11	15
Bandwidth (GHz)	1–10	1–5.5	1	0.5–5.8
DSB NF (dB)	4.6±0.6	3.9	15.9	4.2
OIP3	16.5	15.6	17.5	–

+1 dBm and +3 dBm over the band. Table I summarizes the proposed mixer's performance.

IV. CONCLUSION

A 1–10 GHz down-convert mixer with an integrated output amplifier has been developed in 130 nm CMOS. The switched-transconductor configuration is adopted with series inductive peaking for high gain (26.5 dB) and low NF (4–5 dB) up to 10 GHz. DS is effectively incorporated in the output amplifier using the body bias of the PMOS devices, to achieve a high OIP3 of 16.5 dBm. The circuit consumes less than 20 mW of dc power and occupies an active chip area below 0.2 mm².

REFERENCES

- [1] A. Amer, E. Hegazi, and H. Ragaie, "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 323–328, Feb 2007.
- [2] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "The blixer, a wideband balun-LNA-I/Q-mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, Dec 2008.
- [3] S. Ho and C. Saavedra, "A CMOS broadband low-noise mixer with noise cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1126–1132, May 2010.
- [4] D. Na and T. W. Kim, "A 1.2 V, 0.87–3.7 GHz wideband low-noise mixer using a current mirror for multiband application," *IEEE Microw. Compon. Lett.*, vol. 22, no. 2, pp. 91–93, Feb 2012.
- [5] B. Guo, H. Wang, and G. Yang, "A wideband merged CMOS active mixer exploiting noise cancellation and linearity enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2084–2091, Sept 2014.
- [6] T. W. Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 223–229, Jan 2004.
- [7] J. Lee, J. Lee, B. Kim, B.-E. Kim, and C. Nguyen, "A highly linear low-noise amplifier using a wideband linearization technique with tunable multiple gated transistors," in *IEEE Radio Freq. Integr. Circuits Symp.*, June 2013, pp. 181–184.
- [8] M. Wang, S. He, and C. E. Saavedra, "+14 dB Improvement in the IIP₃ of a CMOS Active Mixer through Distortion Cancellation," in *IEEE Int. Wireless Symposium*, April 2013, pp. 1–4.
- [9] A. El-Gabaly, D. Stewart, and C. Saavedra, "2-W broadband GaN power-amplifier RFIC using the f_T doubling technique and digitally assisted distortion cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 525–532, Jan 2013.
- [10] K.-H. Liang, C.-H. Lin, H.-Y. Chang, and Y.-J. Chan, "A new linearization technique for CMOS RF mixer using third-order transconductance cancellation," *IEEE Microw. Compon. Lett.*, vol. 18, no. 5, pp. 350–352, May 2008.
- [11] E. Klumperink, S. Louwsma, G. Wienk, and B. Nauta, "A CMOS switched transconductor mixer," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231–1240, Aug 2004.