Workshop
WME

2009 International Microwave Symposium

CMOS Subharmonic Mixers and Applications

Carlos E. Saavedra
Associate Professor of Electrical and Computer Engineering
Queen's University
CANADA

Workshop Organized by: TCC-22

Queen's UNIVERSITY

Outline

- CMOS SHP mixer design considerations
- Analysis of the Gilbert-Cell X2 SHP mixer
- Recent advances: X4 Subharmonic mixer
- Frequency multiplication using SHP mixers
- Conclusion

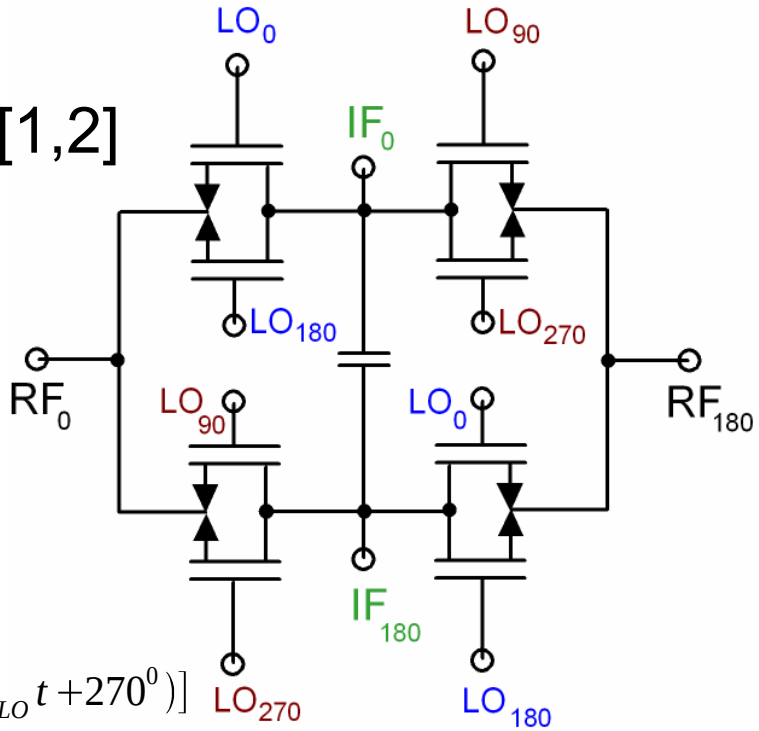
Queen's UNIVERSITY

Design Considerations

- CMOS SHP mixers based on the Gilbert cell have **conversion gain**, even at high multiplication factors
- **High port-to-port isolation** is easily achieved using a differential circuit topology
- In contrast to diode-based SHP mixers **diplexers are not needed** to feed the RF and LO signals to the mixer
- These attributes, however, come at the cost of DC power consumption and lower P_{1dB} and IIP3 relative to diode-based SHP mixers.

Passive CMOS SHP Mixer [1,2]

Concept: replace the FET switches in a ring mixer with doubler circuits



$$IF_0 = RF_0[\sin(\omega_{LO}t)\sin(\omega_{LO}t+180^0)] + RF_{180}[\sin(\omega_{LO}+90^0)\sin(\omega_{LO}t+270^0)]$$

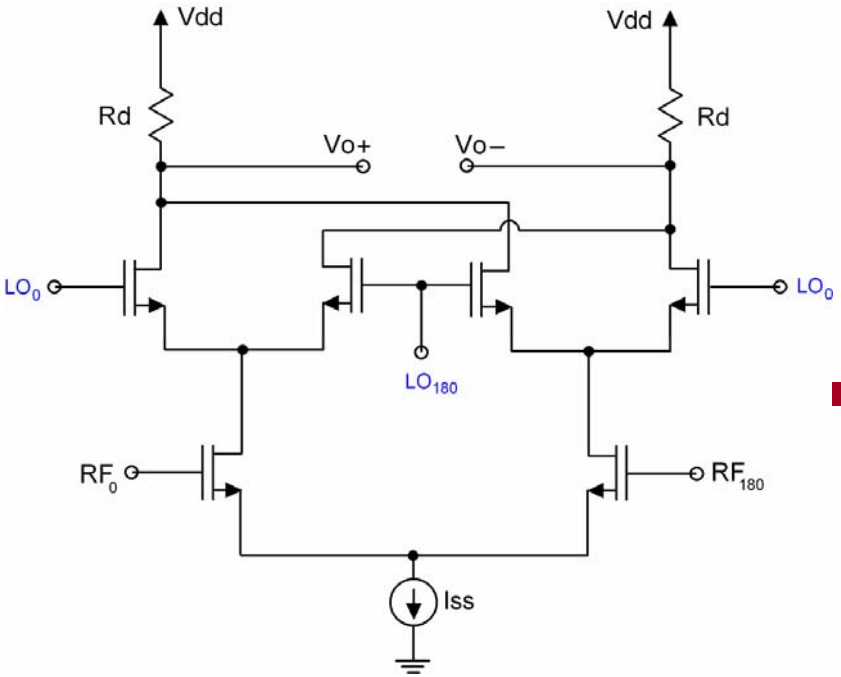
$$= RF_0[-\sin^2(\omega_{LO}t)] - RF_0[-\cos^2(\omega_{LO}t)] = RF_0[\cos^2(\omega_{LO}t) - \sin^2(\omega_{LO}t)]$$

$$= RF_0\cos(2\omega_{LO}t)$$

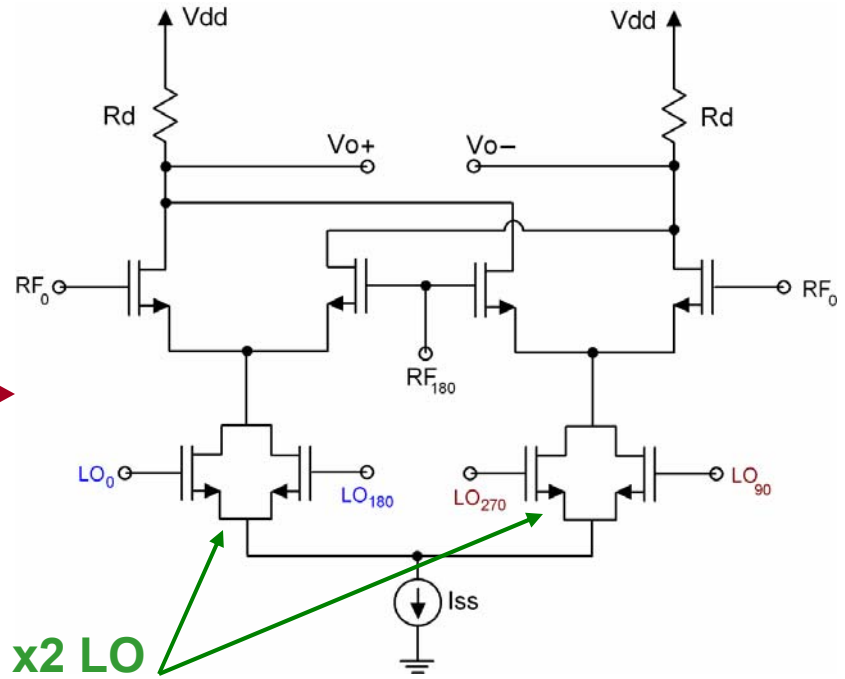
Similarly we can show that, $IF_{180} = -RF_0\cos(2\omega_{LO}t)$

Queen's UNIVERSITY

x2 SHP mixer using a Gilbert Cell [3-5]



Standard Gilbert Cell

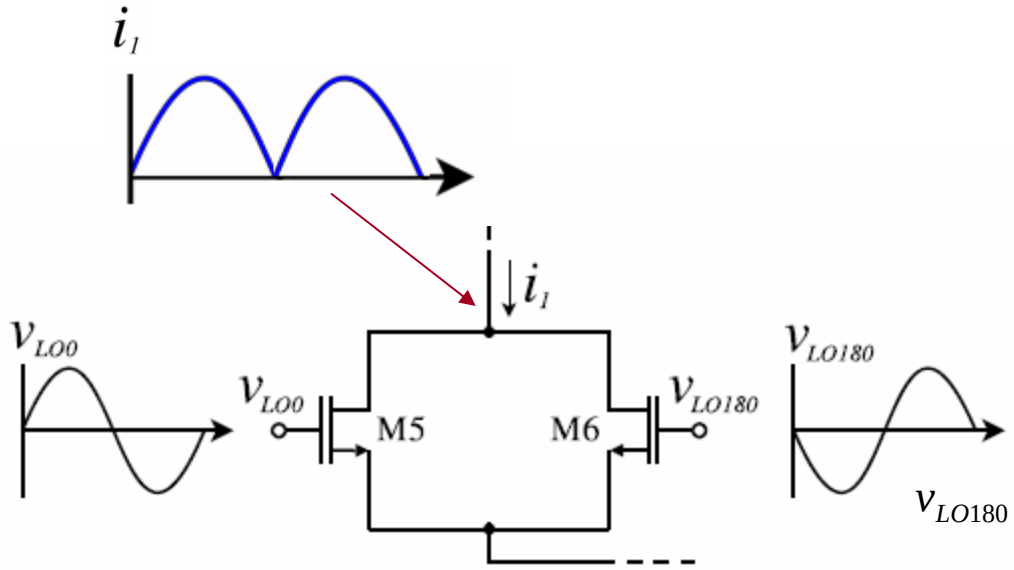


x2 LO multiplication

IMS 2009 BOSTON MA

x2 SHP Mixer Operation Details

$v_{LO0} = A_{LO}\sin(\omega_{LO}t)$



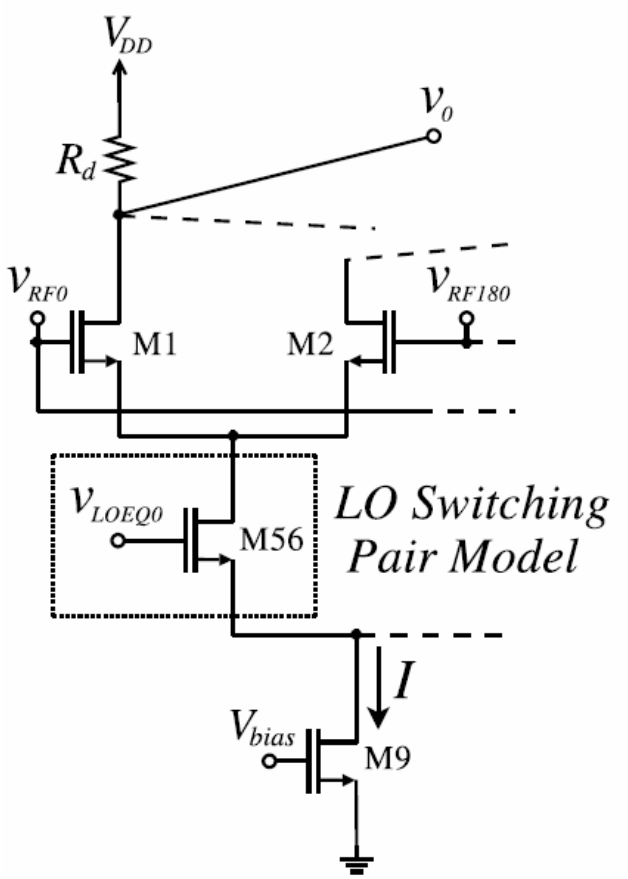
$v_{LO180} = A_{LO}\sin(\omega_{LO}t - \pi)$

$$i_1 = i_a + i_b = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(v_{LO0}^2 + v_{LO180}^2)$$

$$i_1 = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \mu_n C_{ox}\frac{W_1}{L}v_{LO0}^2$$

Using the relationship, $v_{LO0}^2 = v_{LO180}^2$

Modeling the Conversion Gain

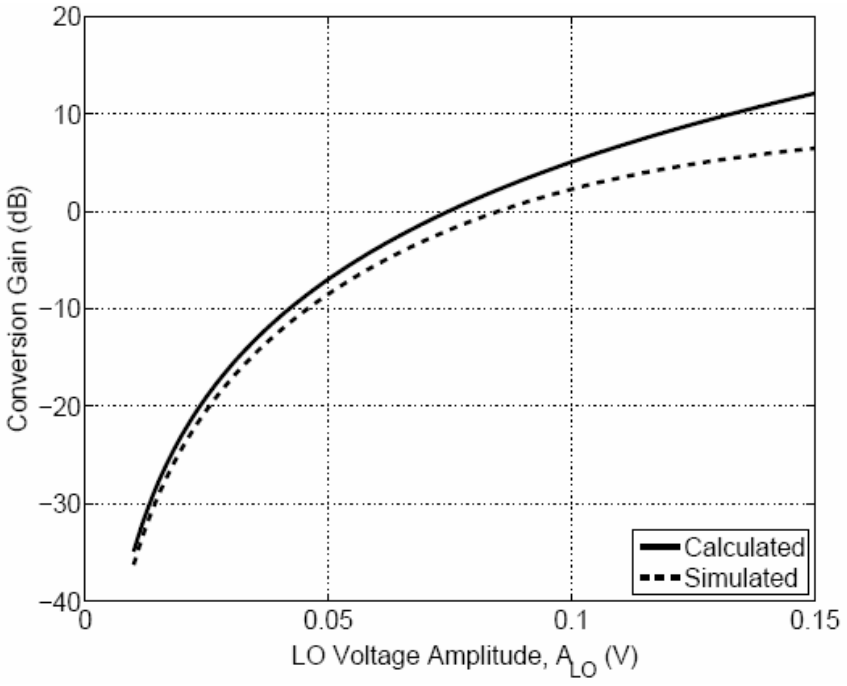


- Converge the two transistors in the X2 doubler network into a *single equivalent* transistor
- The drive signal of the equivalent transistor is,

$$v_{LOeq} \propto \cos(2\omega_{LO}t)$$

- Analyze the resulting mixer circuit as a classic Gilbert-Cell mixer to obtain a a closed-form expression for conversion gain.

Modeling the Conversion Gain – cont'd



$$v_{LOEQ0} \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} cos(2\omega_{LO}t)$$

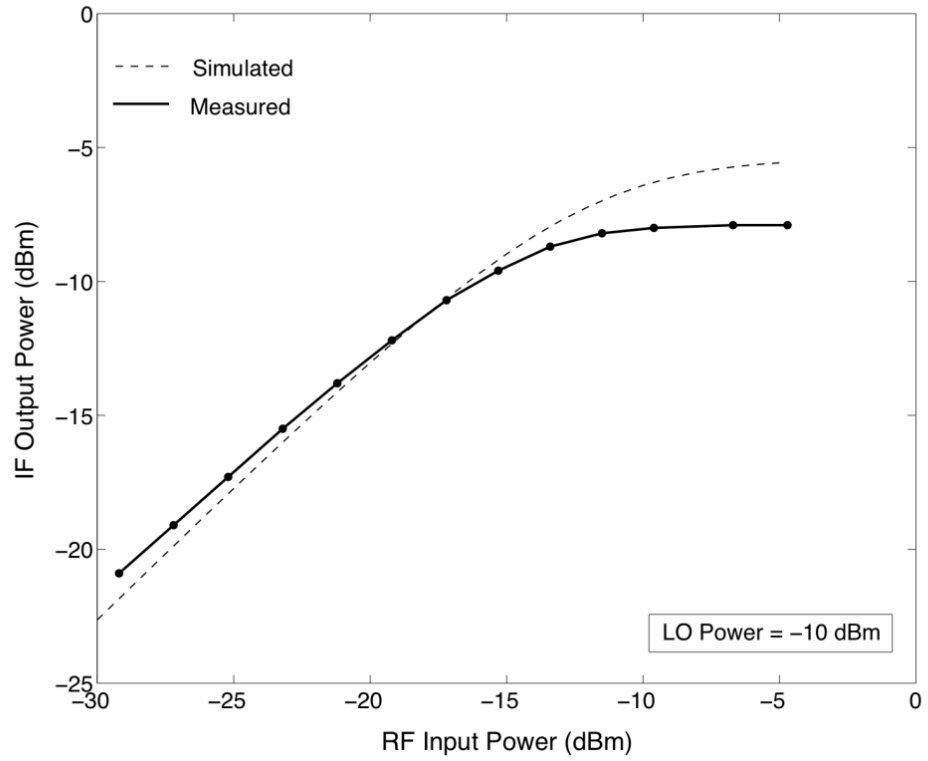
$$v_{LOEQ180} \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} cos(2\omega_{LO}t + \pi)$$

$$CG_{dB} = 20log\left(\frac{R_d I A_{LO}^2}{4(V_{GS(RF)} - V_t)(V_{GS(LO)} - V_t)^2}\right)$$

For more modeling details see Ref. [6]

Queen's UNIVERSITY

CMOS x2 SHP Mixer Power Performance



Conversion Gain ~ 8 dB

$P_{1dB,out}$ = - 9 dBm

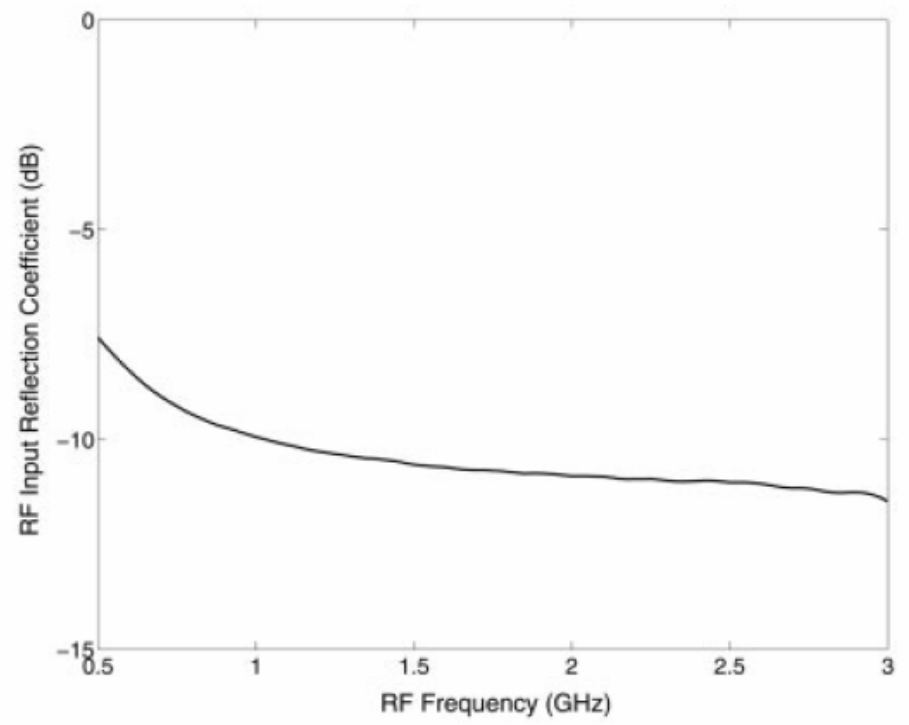
OIP3 = 0 dBm

IMS 2009 BOSTON MA

CMOS Subharmonic Mixers and Applications

Queen's UNIVERSITY

RF input match



Broadband input match obtained using an active balun at the RF port

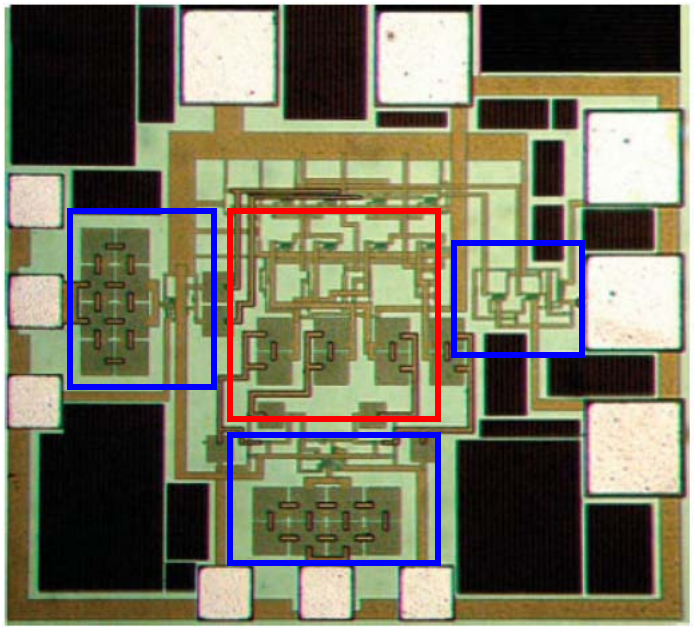
Port Isolations

Ports	*Isolation*
RF–LO	62 dB
LO–RF	58 dB
2LO–RF	68 dB
RF–IF	35 dB
LO–IF	37 dB
2LO–IF	49 dB

IMS 2009 BOSTON MA

Queen's UNIVERSITY

x2 SHP Mixer Chip Microphotograph



RF frequency	2.1 GHz
LO frequency	1 GHz
IF frequency	100 MHz
DC Power	36 mW
Chip Size	0.42 mm^2 incl. pads

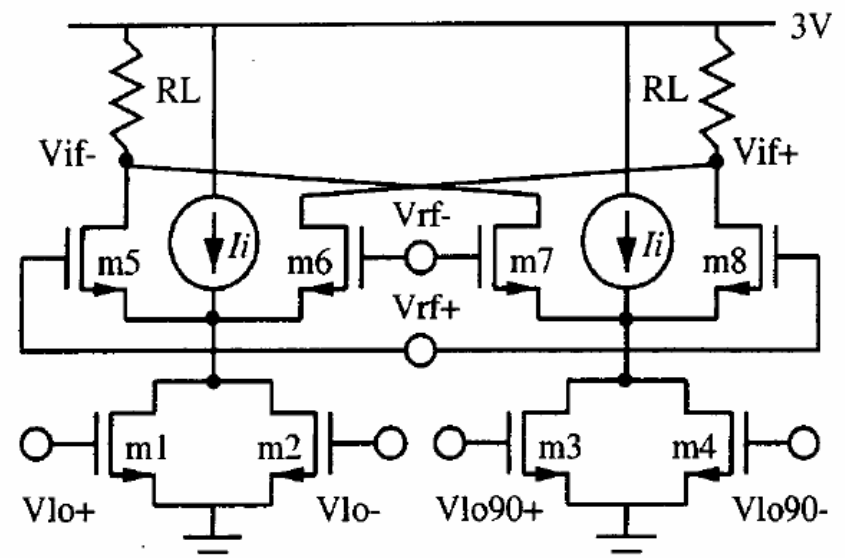
mixer core

input/output active baluns

IMS 2009 BOSTON MA

Queen's UNIVERSITY

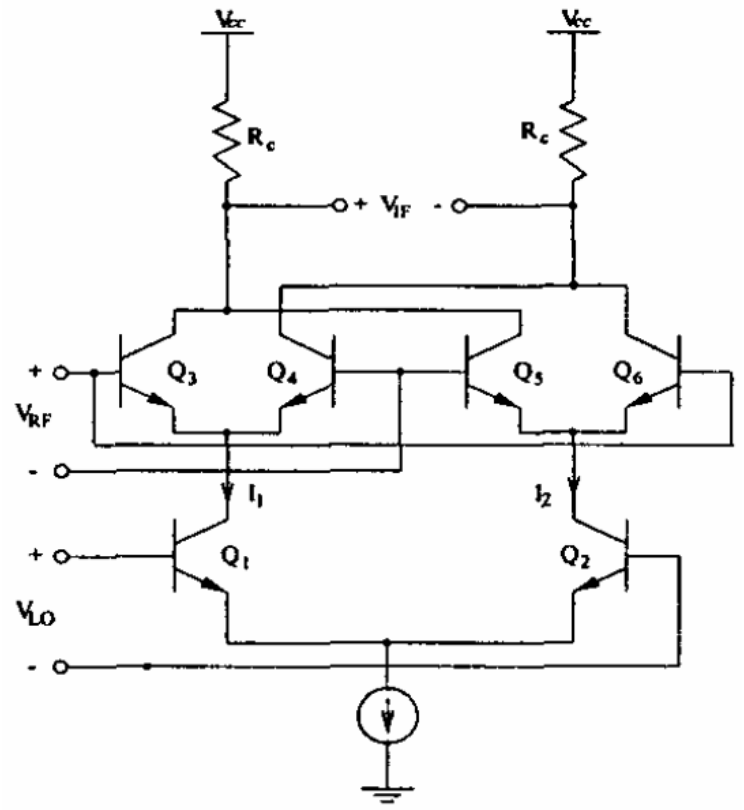
Similar x2 SHP mixer designs [3]



RF Freq	930.1 MHz
LO Freq	465 MHz
IF Freq	0.10 MHz
Conv. Gain	12 dB
P1dB	Not reported
IP3	Not reported
Technology	0.35 µm CMOS

From Ref. [3]

Similar x2 SHP mixer designs [4]



From Ref. [4]

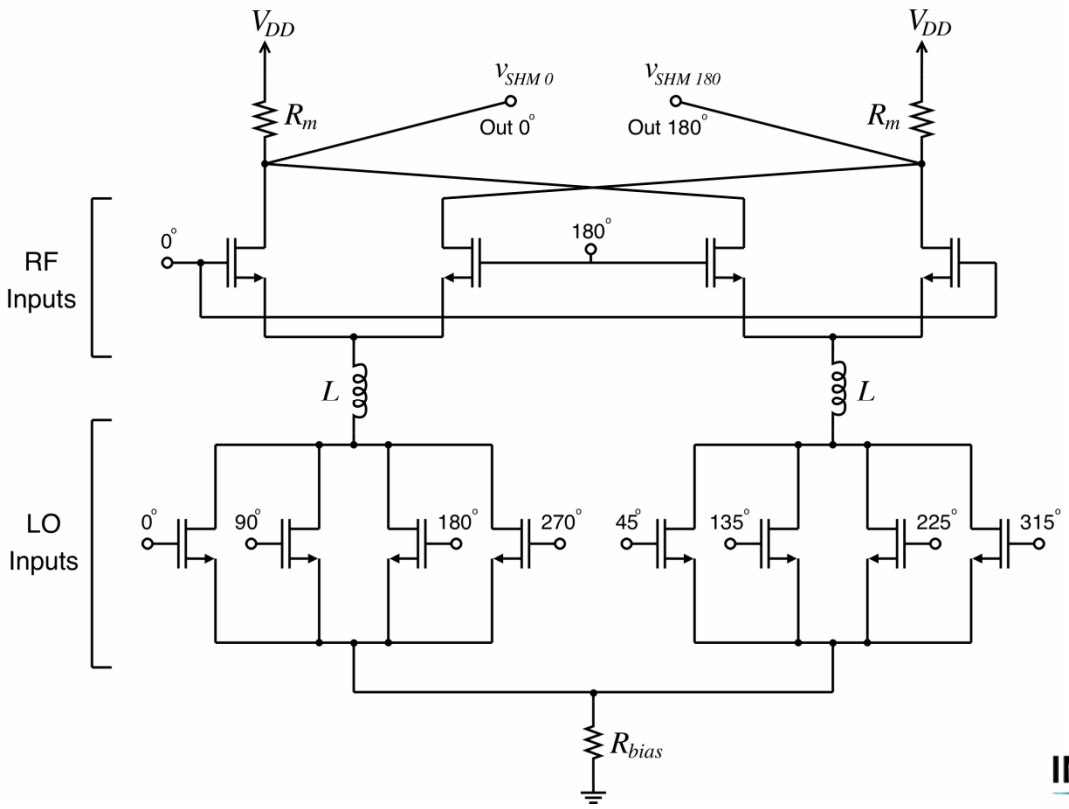
RF Freq	1.90 GHz
LO Freq	0.90 GHz
IF Freq	100 MHz
Conv. Gain	7.5 dB
P1dB	-8 dBm
IIP3	-3 dBm
Technology	0.35 µm BiCMOS

IMS 2009
BOSTON MA

CMOS Subharmonic Mixers and Applications

Recent Advances:

X4 Subharmonic Mixer

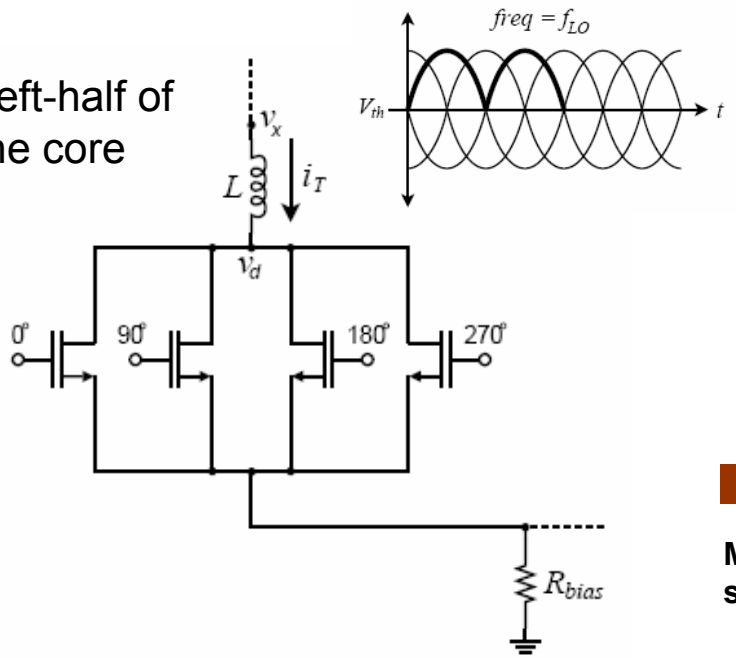


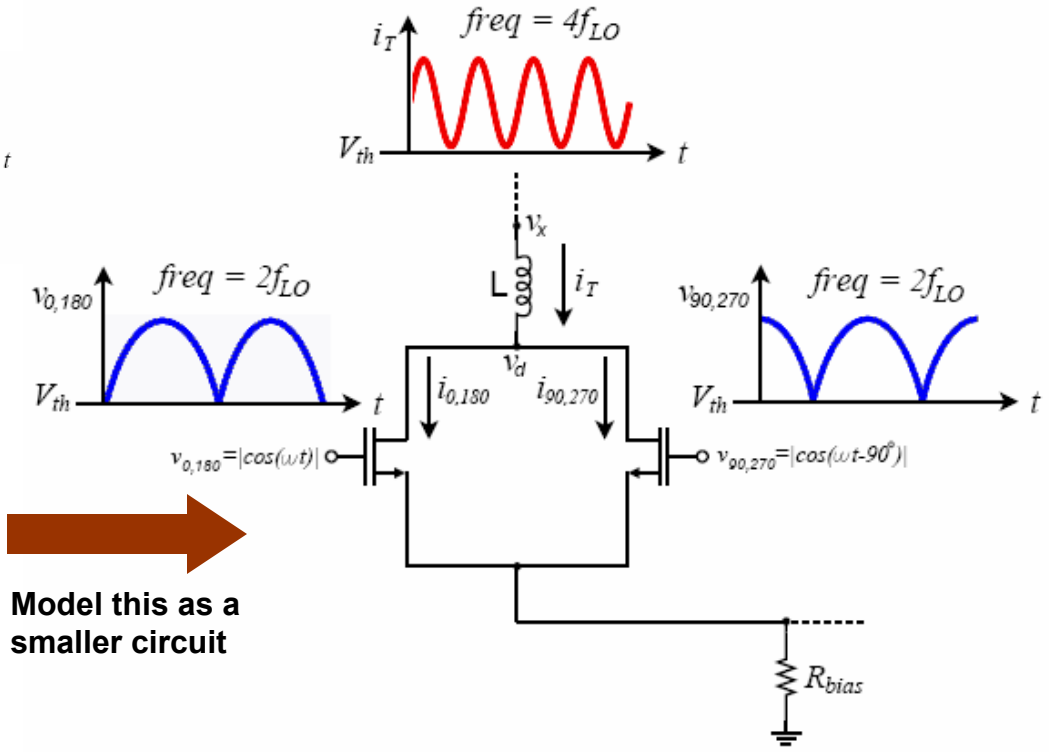
B. R. Jackson and C. E. Saavedra, "A CMOS Ku Band 4X Subharmonic Mixer," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 6, pp. 1351-1359, June 2008.

IMS 2009
BOSTON MA

The LO Multiplication Core - modeling

Left-half of the core





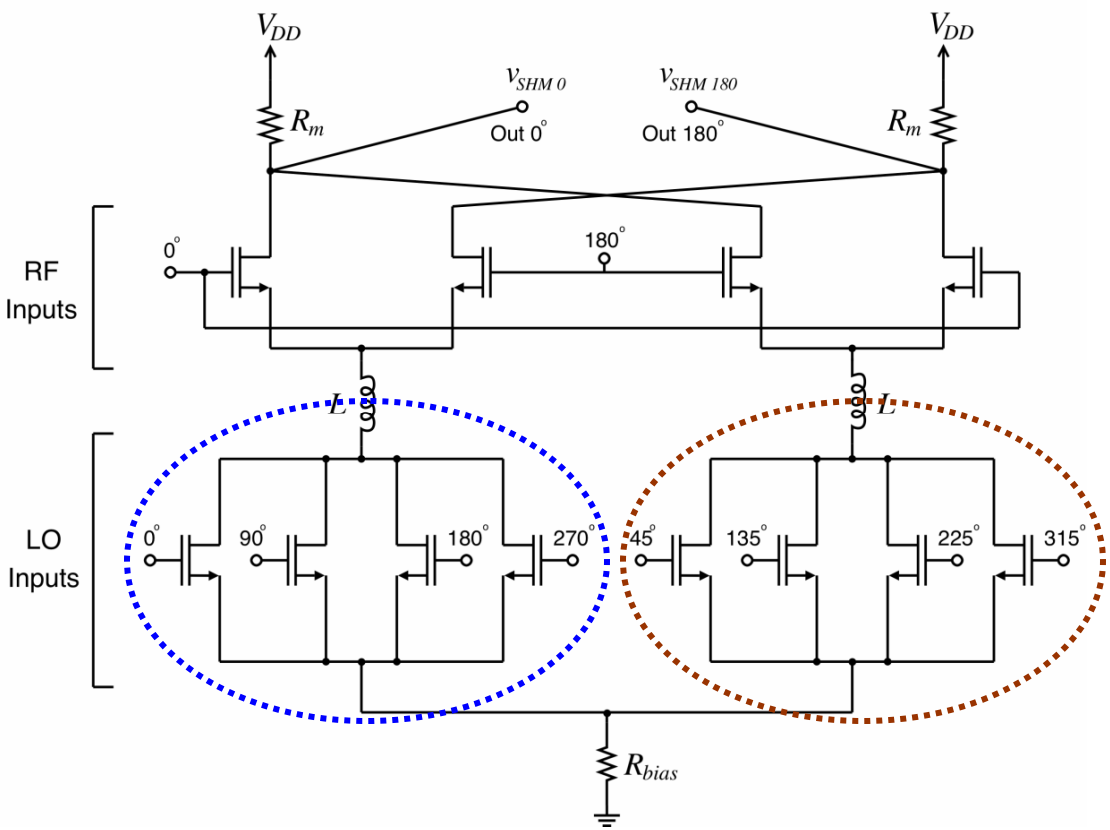
Model this as a smaller circuit

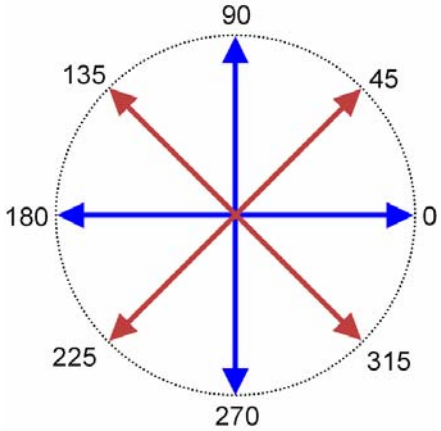
The current at ***4f*$_{LO}$**

$$i_T \approx \frac{1}{2}\mu_n C_{ox} W E_{sat} A_{LO}\left(\frac{15}{16}+\frac{1}{2}\left|\sin(2\omega_{LO}t)\right|+\frac{1}{16}\cos(4\omega_{LO}t)\right)$$

IMS 2009 BOSTON MA

The LO phases in the multiplication core



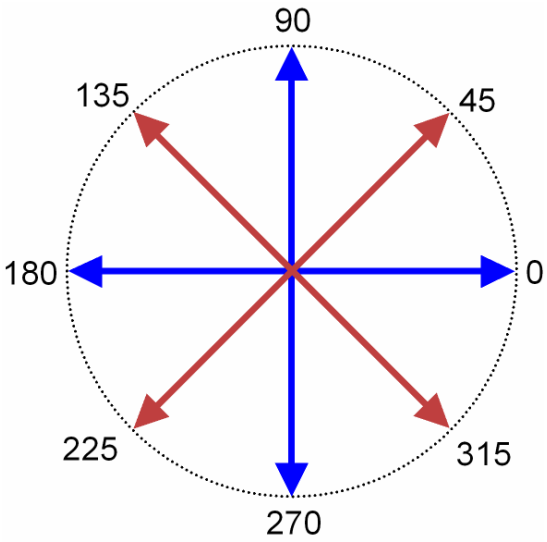


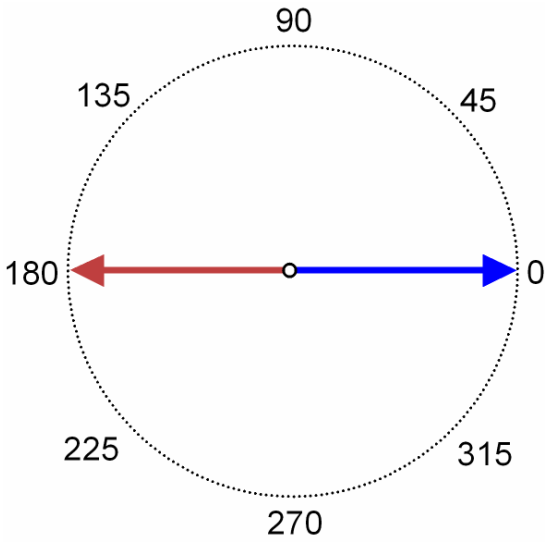
Octet-phase LO signal used to generate the $4f_{LO}$ signal

IMS 2009
BOSTON MA

Queen's UNIVERSITY

Creating a differential at signal at $4\omega_{LO}$:





$$v_{LO}(t) = A_{LO}\sin\left(\omega_{LO}t + n\frac{2\pi}{8}\right) = A_{LO}\sin\left(\omega_{LO}t + n\frac{\pi}{4}\right)$$

n = 0, 1, 2, 3,…,7

$$v_{4LO}(t) = v_d + i_T Z_{ind} \propto \sin\left(4\omega_{LO}t + n\pi\right)$$

n = 0, 1, 2, 3,…,7

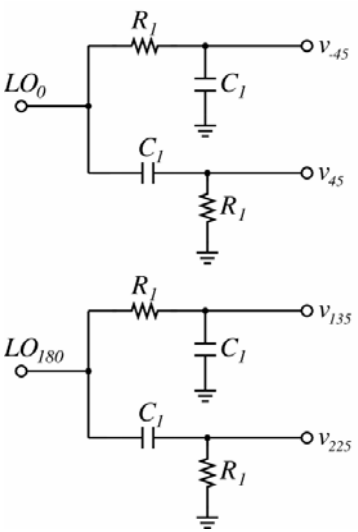
At the frequency, ω, the phases are: 0, π/4, π/2, 3π/4,…7π/4

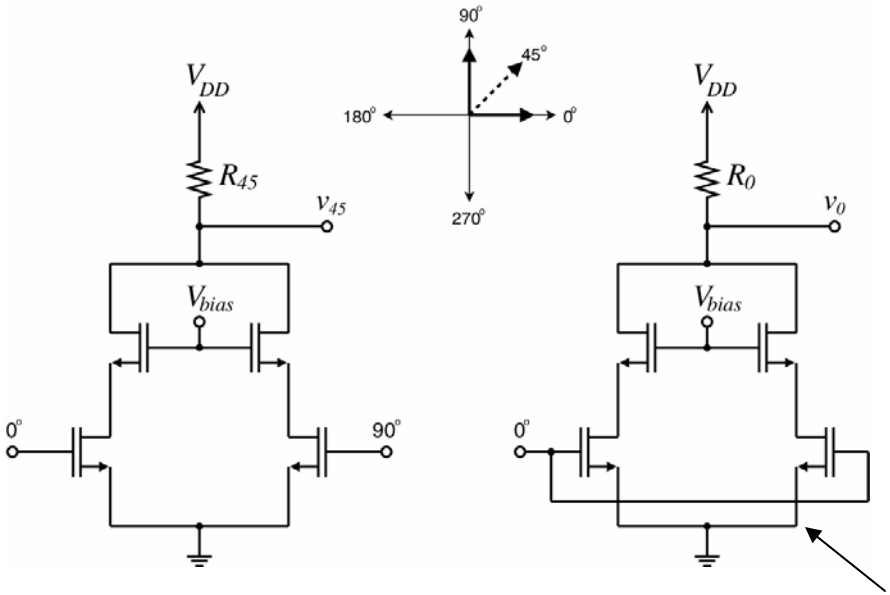
At the frequency, 4ω, the phases are: 0, π, 0, π,…

IMS 2009 BOSTON MA

Queen's UNIVERSITY

LO Octet Phase Generation





Create a set of quadrature signals using a method of your choice

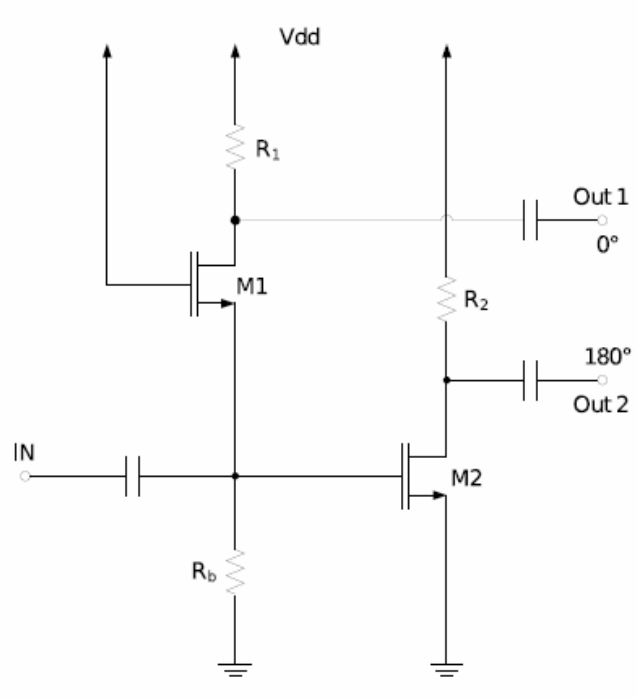
Generate the π/4 vector: add a 0 and a π/2 vector using an active summing junction. Repeat for the other 3 vectors.

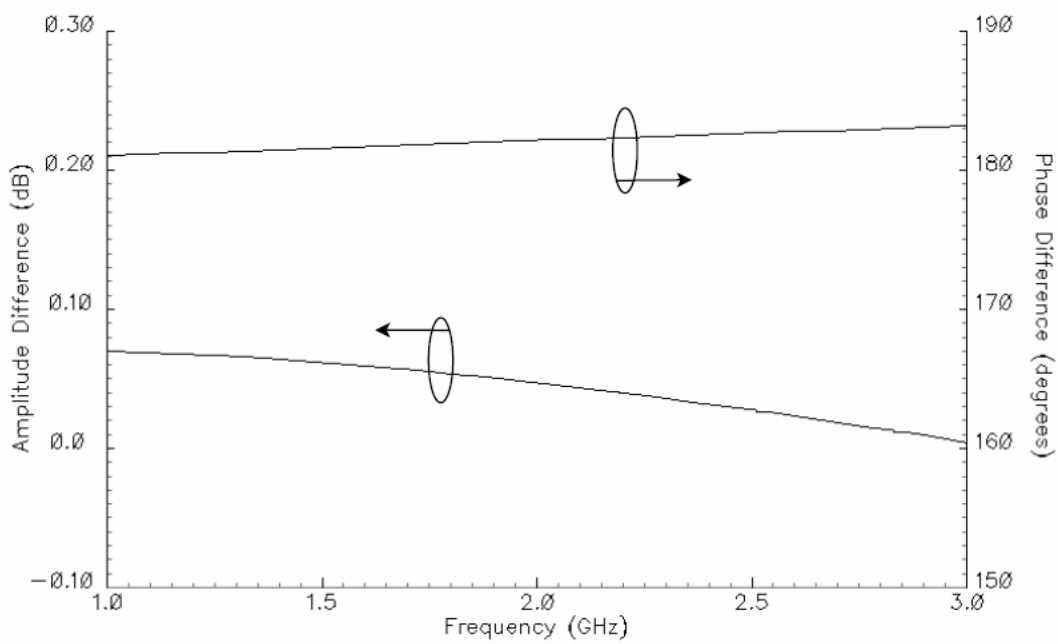
For equalizing the loading effects

IMS 2009 BOSTON MA

Queen's University

Fully integrated x4 SHP Mixer – I/O circuitry



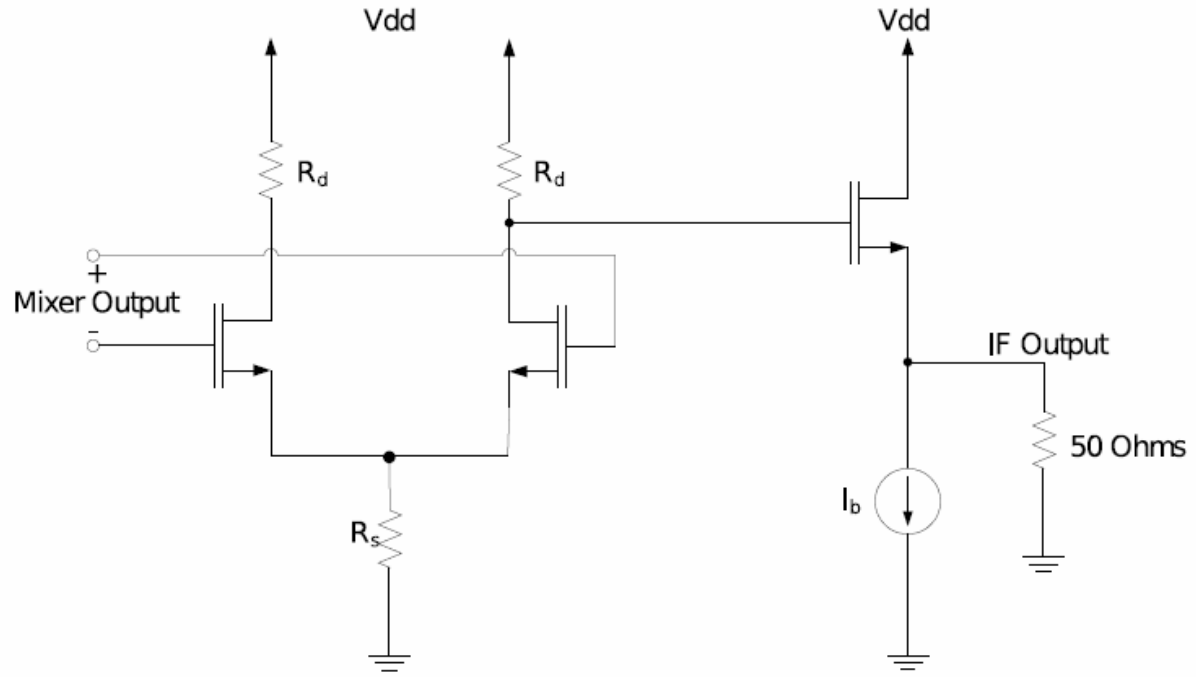


RF active balun

IMS 2009 BOSTON MA

Queen's UNIVERSITY

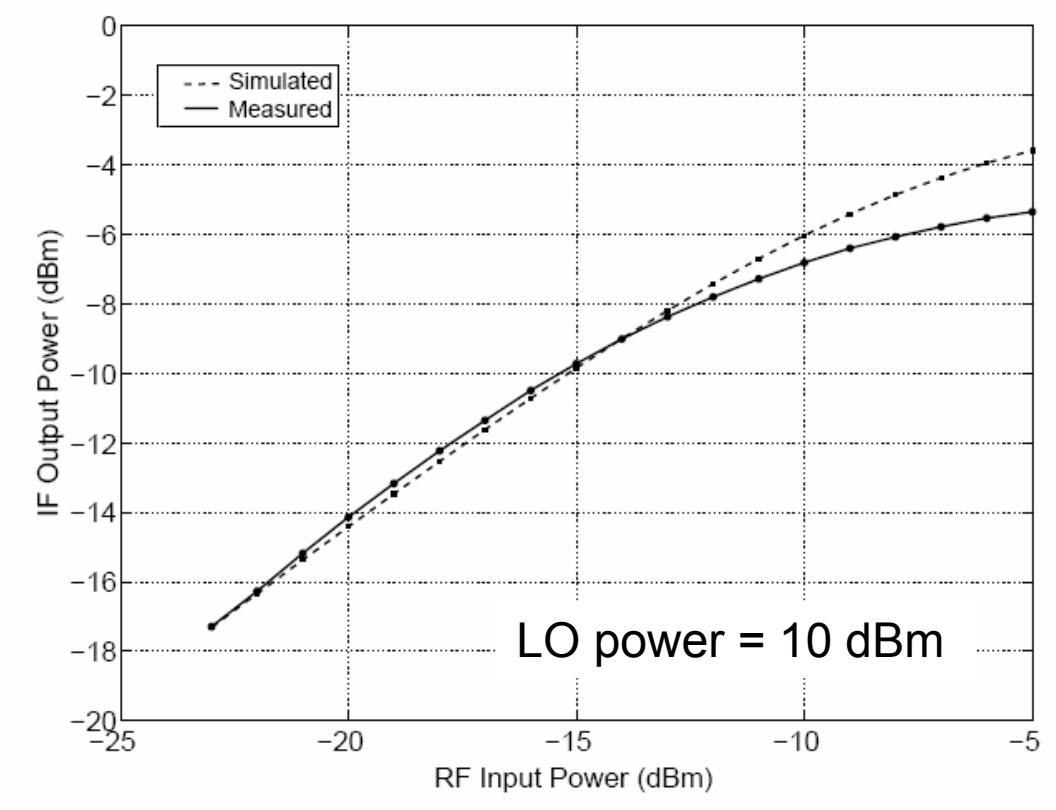
Fully integrated x4 SHP Mixer – I/O circuitry



IF output stage: differential to single-ended conversion

Queen's UNIVERSITY

x4 SHP Mixer Power Performance



Conversion Gain: 6 dB

→ **best reported** to date for a x4 SHP mixer

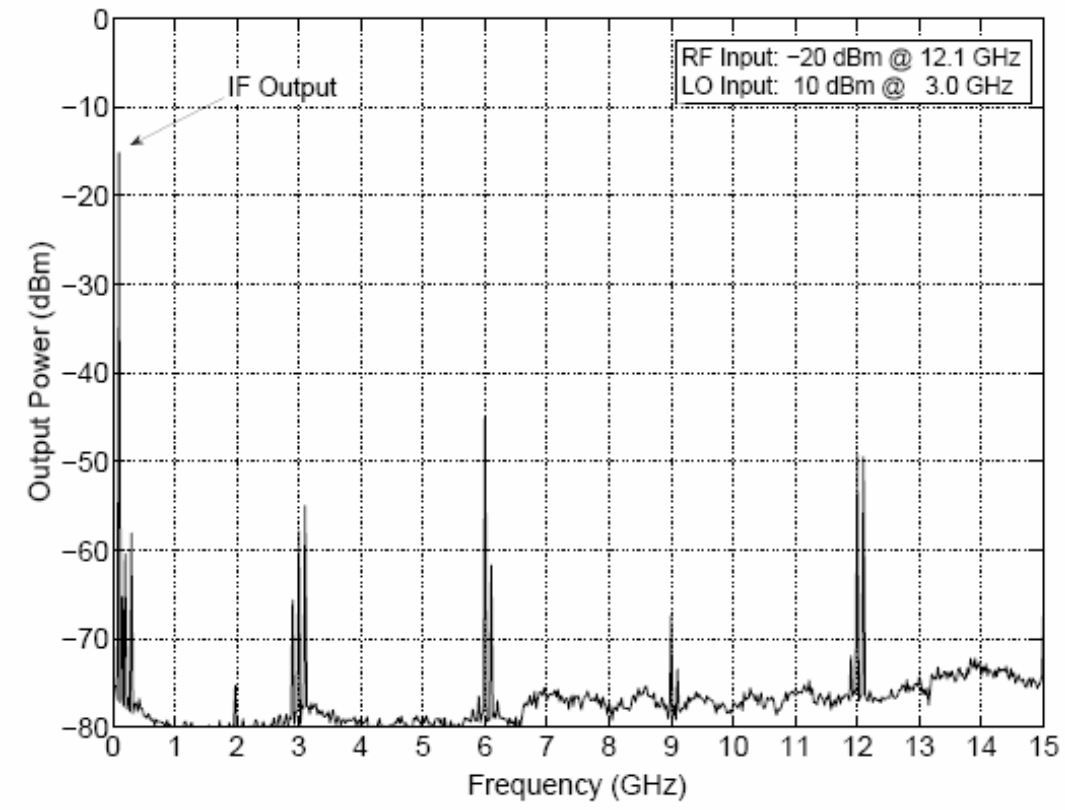
$P_{1dB,out}$: -7 dBm

RF = 12.1 GHz, LO = 3.0 GHz, IF = 100 MHz

IMS 2009 BOSTON MA

Queen's UNIVERSITY

Spectral Response

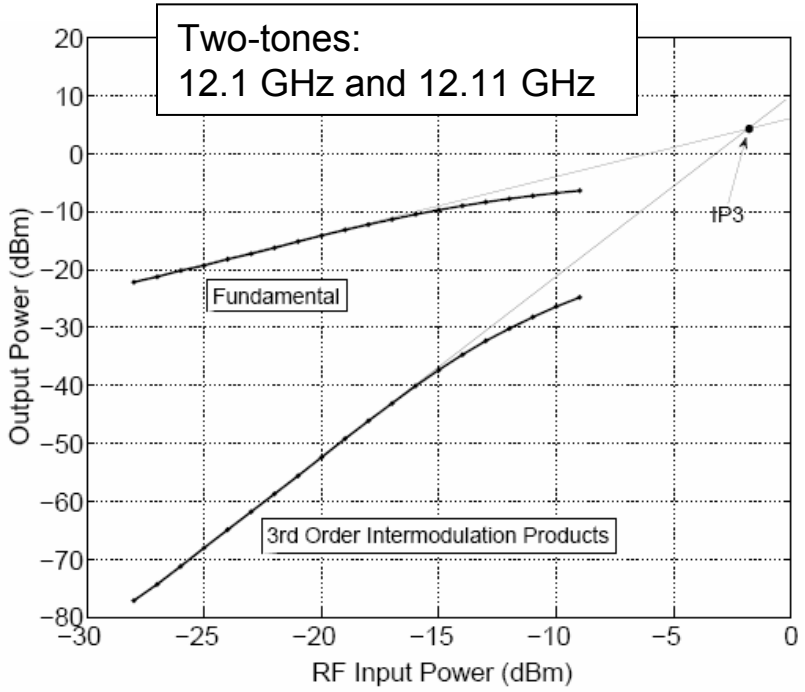


Ports	*Isolation*
RF–LO	43 dB
LO–RF	71 dB
2LO–RF	52 dB
4LO–RF	59 dB
RF–IF	30 dB
LO–IF	68 dB
2LO–IF	55 dB
4LO–IF	59 dB

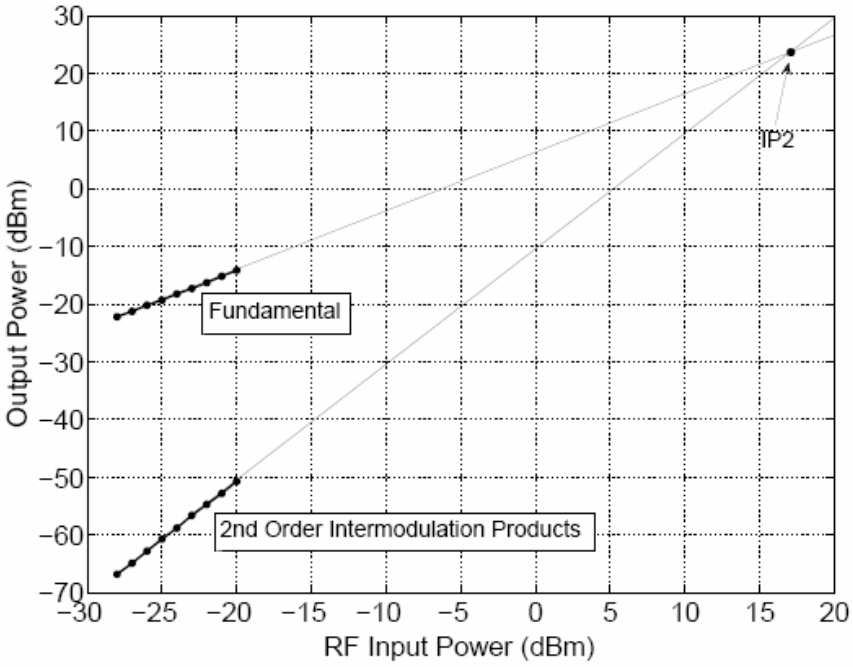
IMS 2009
BOSTON MA

Queen's UNIVERSITY

Intermodulation Distortion Measurements



OIP3 = + 5 dBm



OIP2 = + 24 dBm

Using passive baluns will improve these values

IMS 2009
BOSTON MA

Queen's UNIVERSITY

LO Self-Mixing Performance

How to evaluate LO self-mixing behavior:

1) Measure the DC level at the IF port with no RF and LO input signals: V_{DC1}

2) Measure the DC level at the IF with an LO signal applied and no RF input signal: V_{DC2}

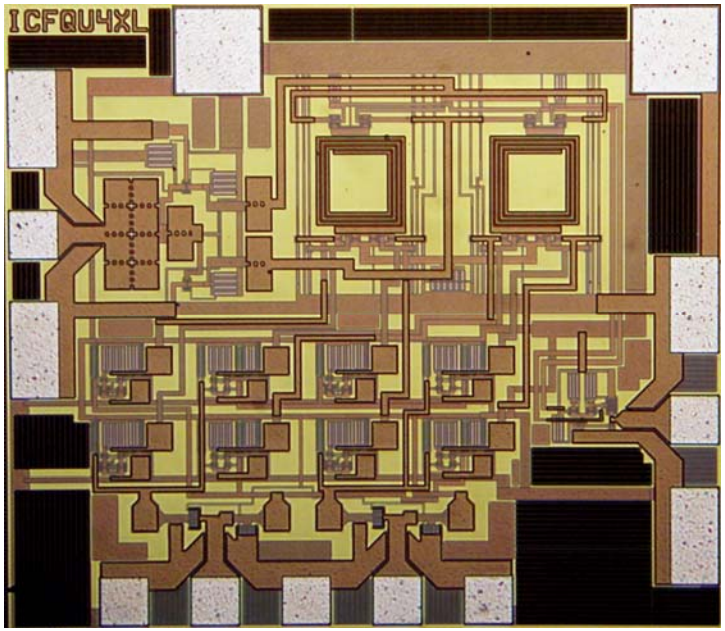
3) LO Self-Mixing is thus: $V_{Self-Mixing} = V_{DC1} - V_{DC2}$

LO input signal used:
+10 dBm @ 3 GHz → V_{rms} = 707 mV

Measured self-mixing voltage at the IF port:
4.2 mV → 44 dB "rejection"

Queen's UNIVERSITY

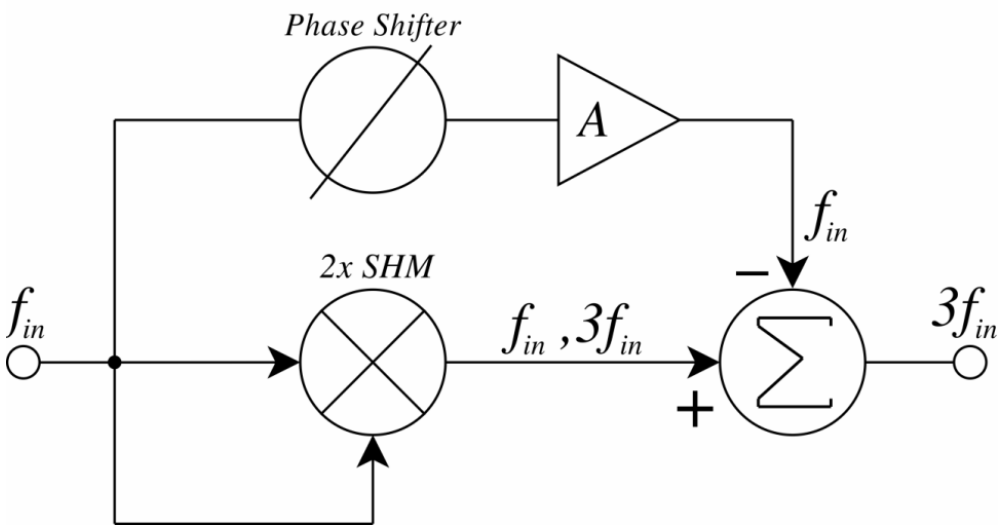
Ku Band x4 SHP Mixer Chip



RF frequency	12.1 GHz
LO frequency	3 GHz
IF frequency	100 MHz
Noise Figure	15 dB (DSB)
Chip Size	0.72 mm^2 incl. pads
DC Power	5 mW (mixer core)
	113 mW (full chip)

IMS 2009
BOSTON MA

Frequency Multiplication with SHP Mixers



odd-order frequency multipliers can be conveniently designed

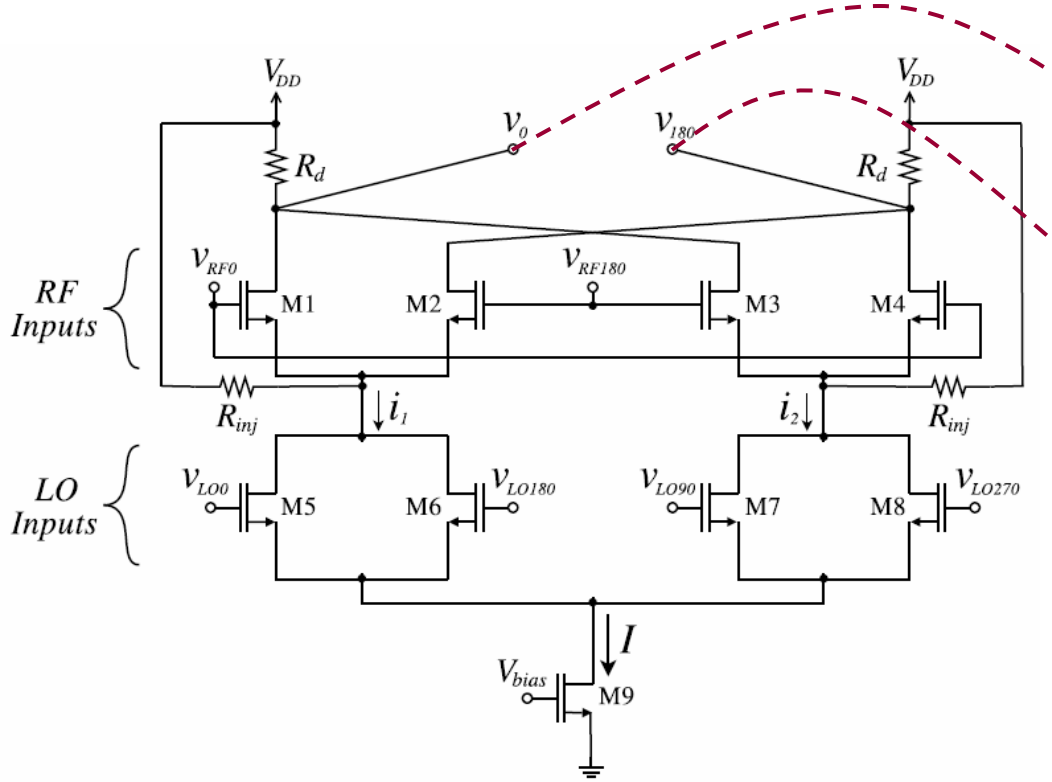
Frequency Tripler with Fundamental Signal Cancellation ⇨ No output filtering needed

B. R. Jackson, F. Mazzilli and C. E. Saavedra, "A Frequency Tripler using a Subharmonic Mixer and Fundamental Cancellation," *IEEE Transactions on Microwave Theory and Techniques,* to appear in 2009.

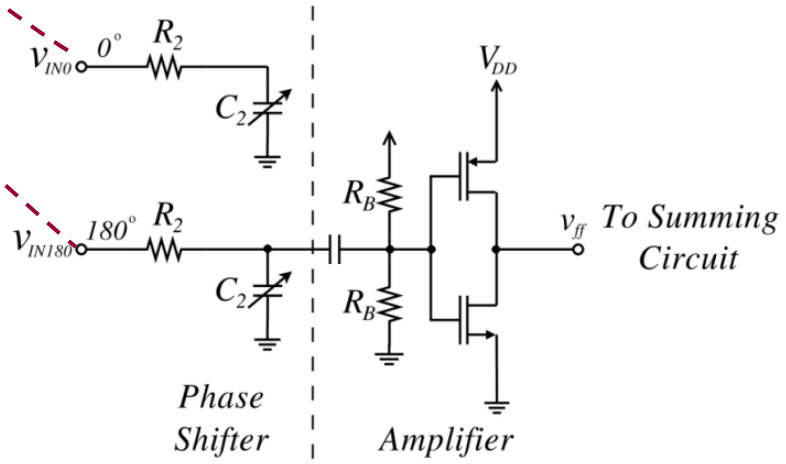
IMS 2009 BOSTON MA

Queen's UNIVERSITY

Frequency Tripler Design



x2 Subharmonic Mixer

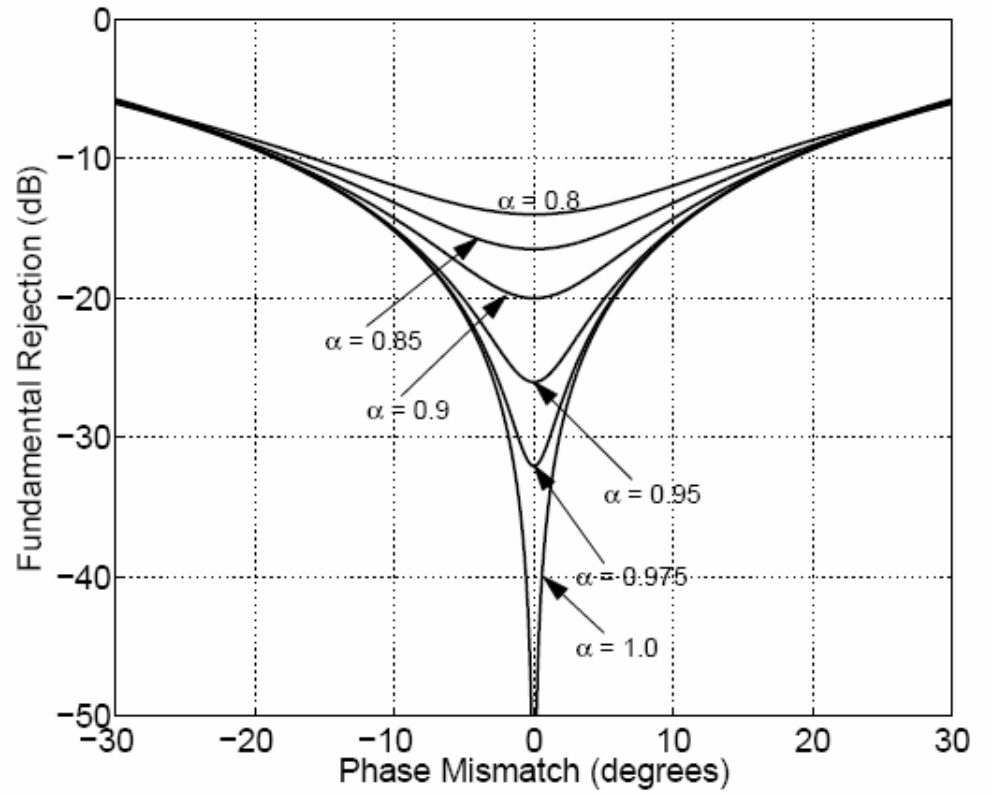


The feedforward path:
Phase Shifter & Amplifier

IMS 2009
BOSTON MA

Queen's UNIVERSITY

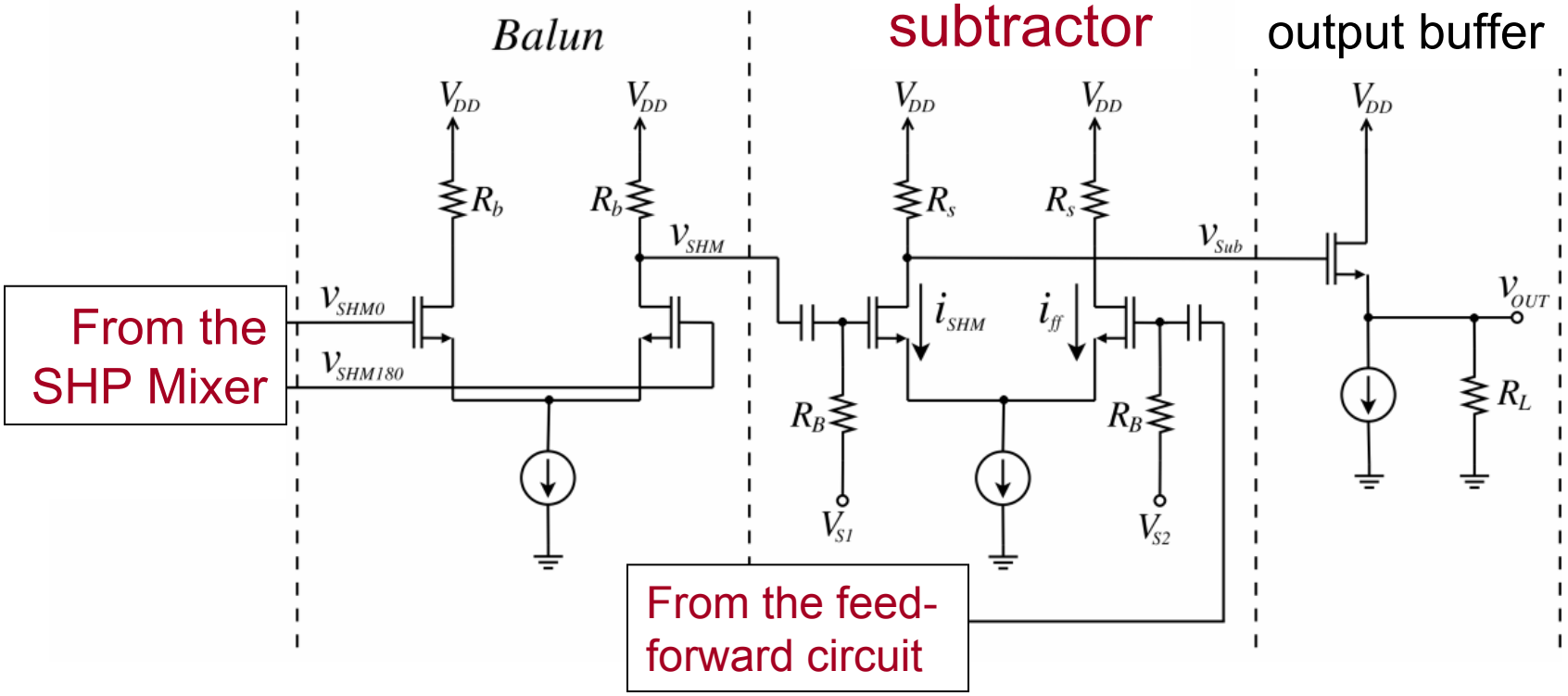
Effect of Phase and Amplitude Mismatch in the Fundamental Cancellation Process



The **phase and amplitude** of the fundamental signal have to be **tuned for maximum** signal **cancellation** at the output.

Queen's UNIVERSITY

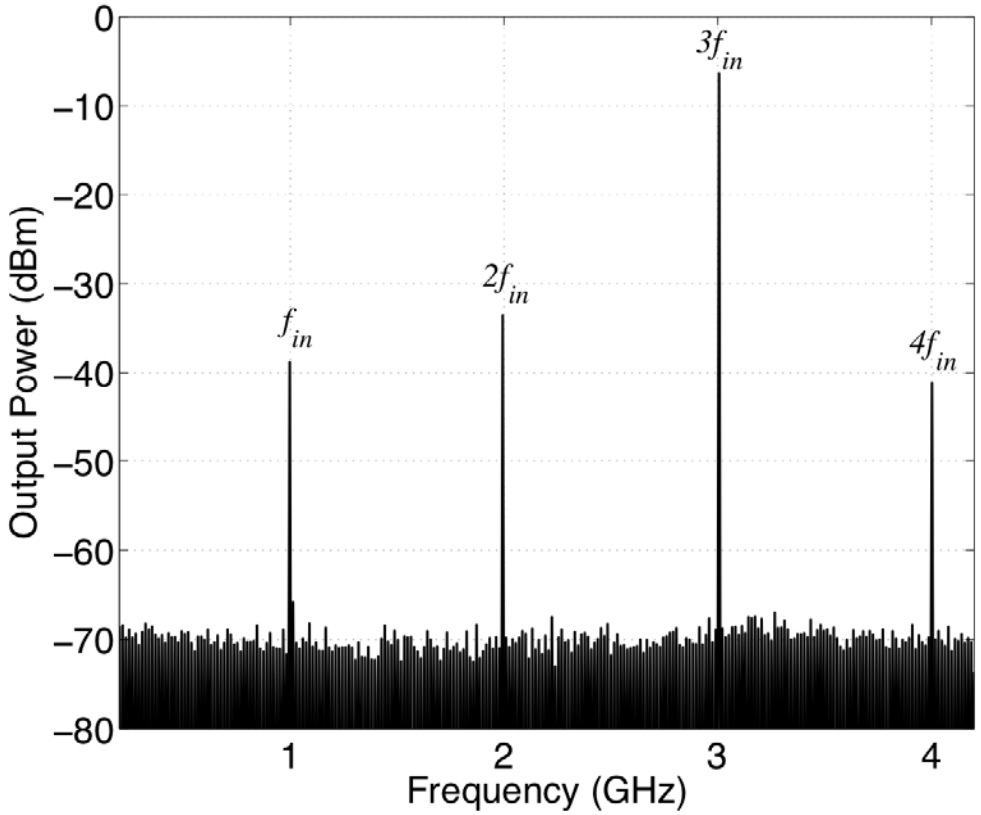
Frequency Tripler Design – cont'd



IMS 2009 BOSTON MA

Queen's UNIVERSITY

Output Spectrum

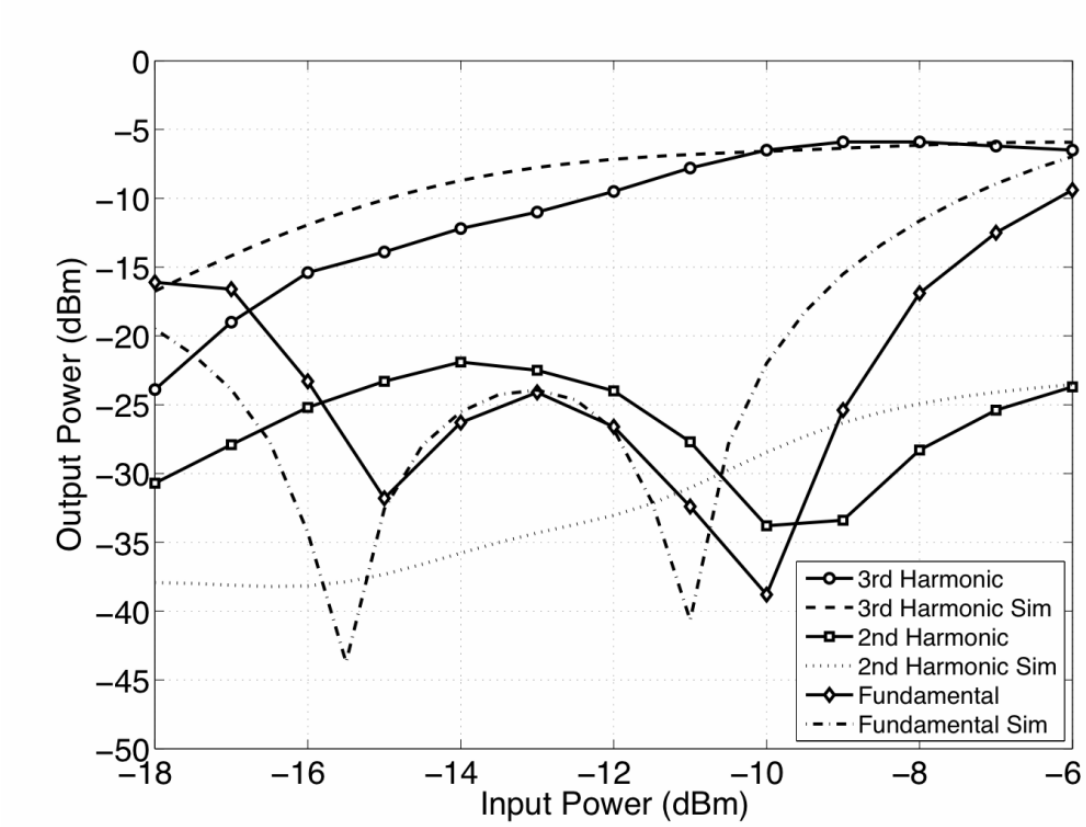


Input Freq.	1 GHz
Input power	-10 dBm
Output Freq.	3 GHz
Conv. Gain	3 dB
Fund. Reject.	30 dB

IMS 2009
BOSTON MA

Queen's UNIVERSITY

Power Performance

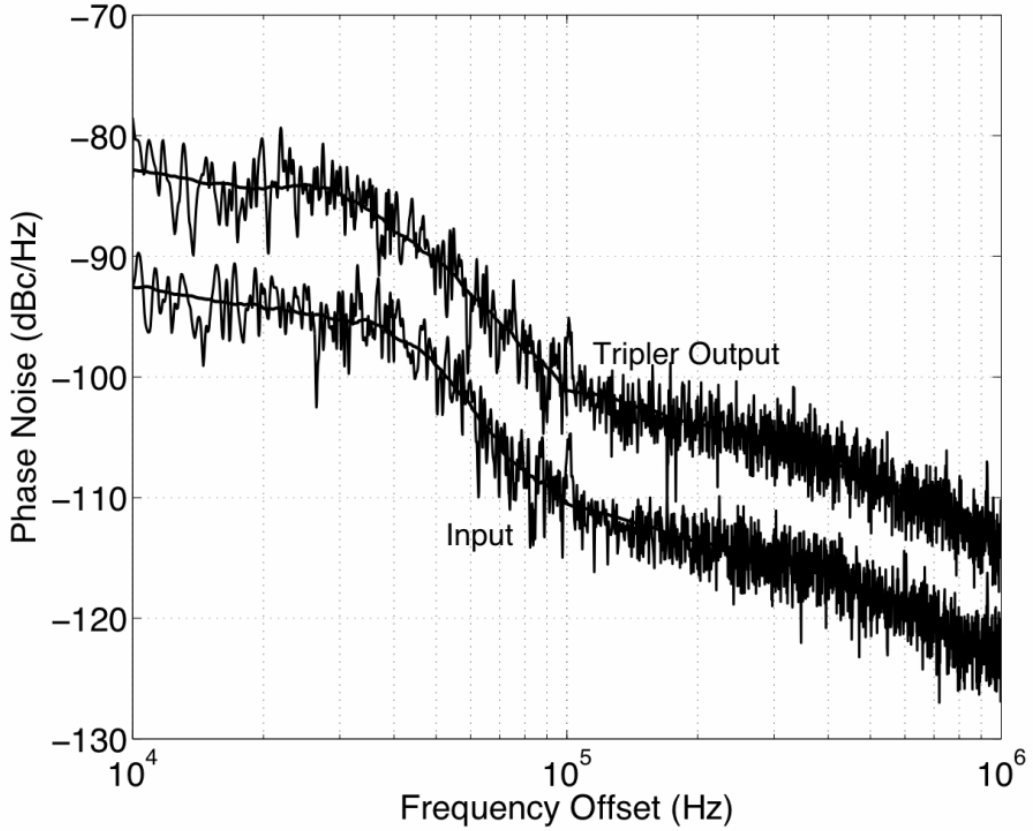


High suppression of the fundamental and other harmonics achieved without on-chip or off-chip filtering.

IMS 2009
BOSTON MA

Queen's UNIVERSITY

Noise Performance



The minimum phase-noise degradation in a multiplier is:

$$20\log(n) = 9.54 \quad dB$$

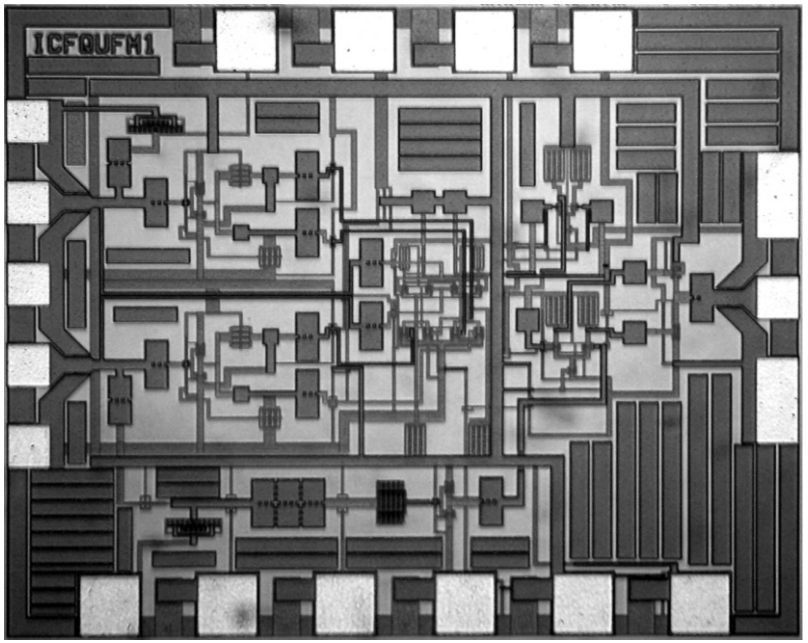
for n = 3. In this work, the degradation is:

9.69 dB

IMS 2009 BOSTON MA

Queen's UNIVERSITY

Frequency Tripler Demonstration Chip



Input freq.	1 GHz
Output freq.	3 GHz
Fund. Reject.	30 dB
Chip Size	0.80 mm^2 incl. pads
DC Power	68 mW (full chip)

IMS 2009
BOSTON MA

Queen's UNIVERSITY

Conclusion

- In general, transistor-based SHP mixers can yield good levels of conv. gain: less than a fundamental Gilbert-Cell but higher than a diode SHP mixer
- Excellent LO-to-RF and LO-to-IF isolation obtained due to the internal multiplication of the LO signal.
- By balancing gain and linearity requirements, the P_{1dB} and IP3 points can be optimized in a CMOS SHP mixer
- Novel circuit concepts can be realized by using SHP mixers such as odd-order multipliers

Acknowledgements

Graduate Students:

- Brad Jackson, Ph.D. student
- Francesco Mazzilli, M.Sc. student

Funding Organizations:

- CMC Microsystems (IC fabrication grants)
- Natural Sciences and Engineering Research Council of Canada (NSERC)
- Ontario Ministry of Training, Colleges and Universities

CMOS Subharmonic Mixers and Applications

About the speaker:

Carlos Saavedra received the Ph.D. and M.Sc. degrees from Cornell University and the B.Sc. degree from the University of Virginia. From 1998-2000 he was with Millitech Corporation and in the year 2000 he joined Queen's University where he is now Associate Professor of Electrical and Computer Engineering and the Coordinator of Graduate Studies. Prof. Saavedra is a member of the Technical Program Committee of the IEEE RFIC Symposium and serves as a reviewer for several journals, including the IEEE T-MTT, IEEE MWCL, IEEE TCAS-II and Electronics Letters. He is a Senior Member of the IEEE.

http://post.queensu.ca/~saavedra/

CMOS Subharmonic Mixers and Applications

References

1. T. H. Teo, W. G. Yeoh, "Low-Power Short-Range Radio CMOS Subharmonic RF Front-End Using CG-CS LNA," *IEEE Trans. Circuits and Systems II: Express Briefs*, Vol. 55, No. 7, pp. 658-662, July 2008.
2. R. H. Kodkani and L. E. Larson, "A 24 GHz CMOS Passive Subharmonic Mixer/Downconverter for Zero-IF Applications," *IEEE Trans. Microwave Theory and Tech.,* Vol. 56, No. 5, pp. 1247-1256, May 2008.
3. Z. Zhaofeng, L. Tsui, C. Zhiheng and J. Lau, "A CMOS Self-Mixing-Free Front-End for Direct Conversion Applications," *IEEE International Symposium on Circuits and Systems,* pp. 386-389, Sydney, Australia, May 2001.
4. K. Nimmagadda and G. Rebeiz, "A 1.9 GHz Double-Balanced Subharmonic Mixer for Direct Conversion Receivers," *IEEE RFIC Symposium,* pp. 253-256, 2001.
5. B. R. Jackson and C. E. Saavedra, "A CMOS Subharmonic Mixer with Active Input and Output Baluns," *Microwave and Optical Technology Letters,* Vol. 48, No. 12, pp. 2472-2478, December 2006.
6. B. R. Jackson, F. Mazzilli and C. E. Saavedra, "A Frequency Tripler using a Subharmonic Mixer and Fundamental Cancellation," *IEEE Transactions on Microwave Theory and Techniques,* to appear in 2009.
7. B. R. Jackson and C. E. Saavedra, "A CMOS Ku Band 4X Subharmonic Mixer," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 6, pp. 1351-1359, June 2008.