Frequency Multipliers

Design Techniques and Applications

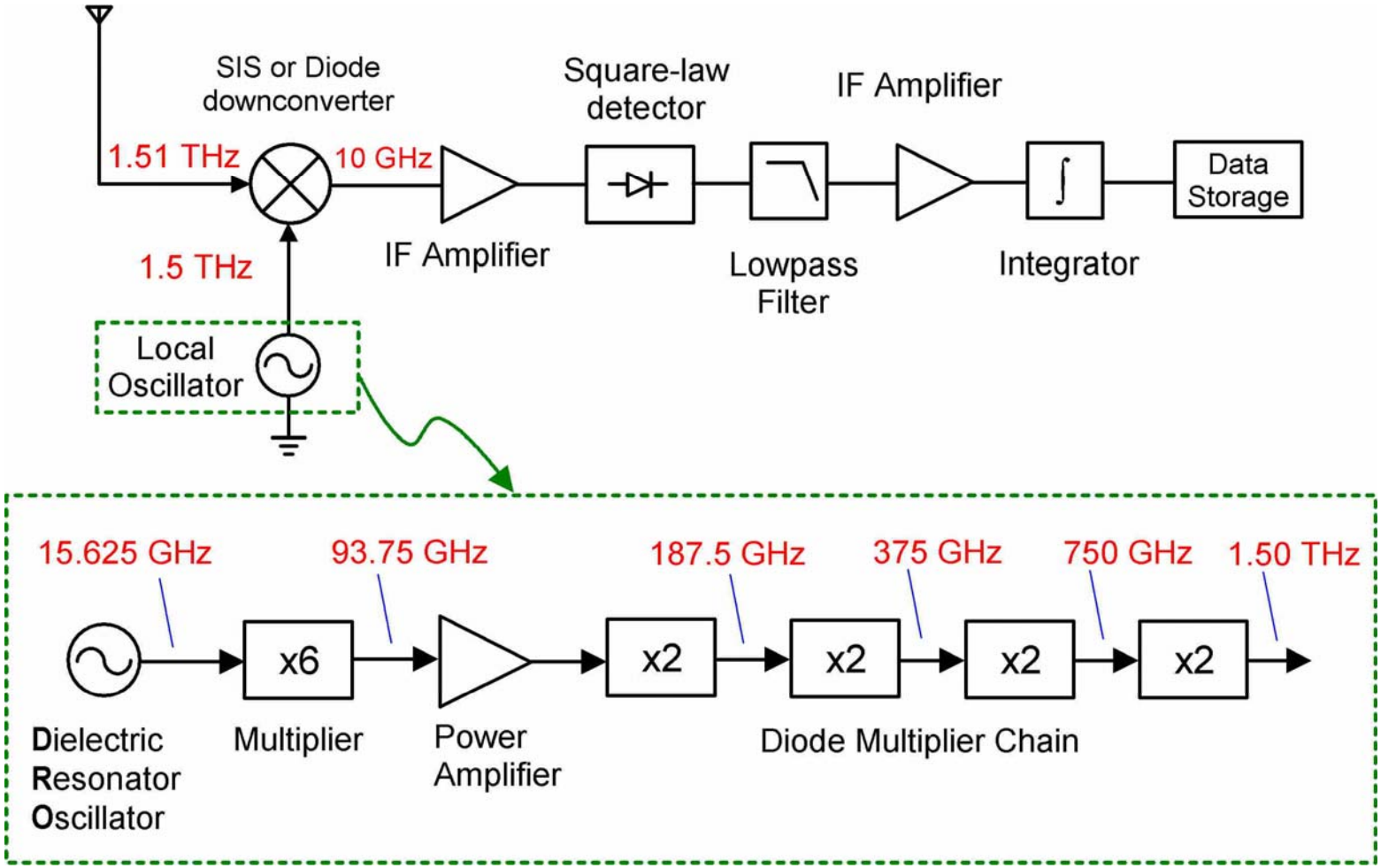
Carlos E. Saavedra
Associate Professor
Electrical and Computer Engineering
Queen's University
Kingston, Ontario
CANADA

Outline

- Introduction – applications
- Noise Concepts in Frequency Multipliers
- Harmonic generation – classical method
- Broadband multipliers
- Advanced concepts in odd-order multiplier design
- Conclusion

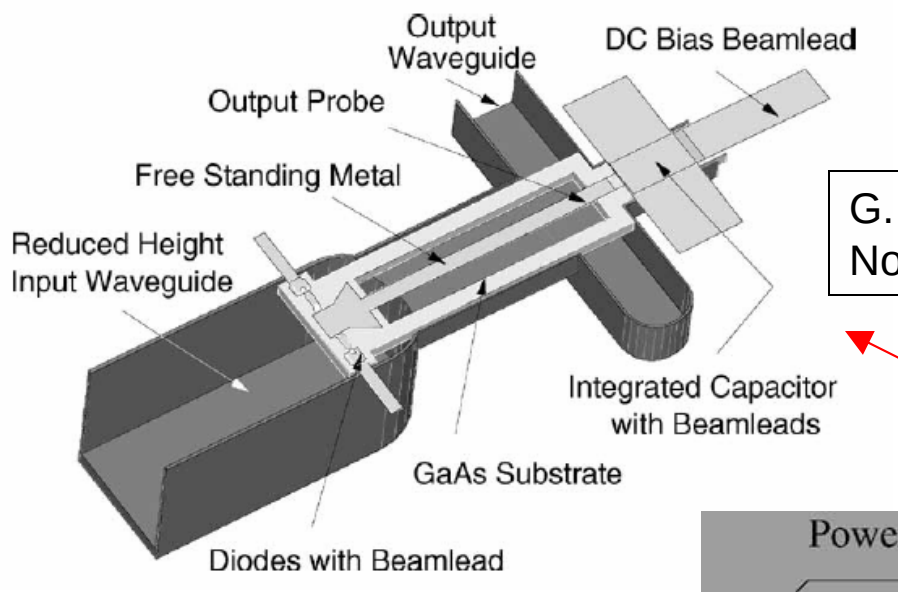
Introduction

Terahertz Receiver for Radio Astronomy



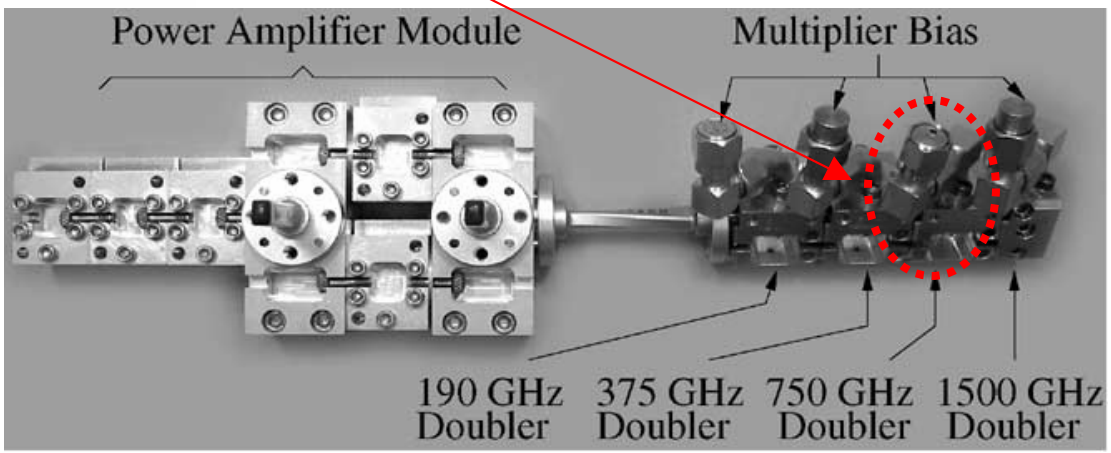
Introduction

Terahertz Receiver – cont'd



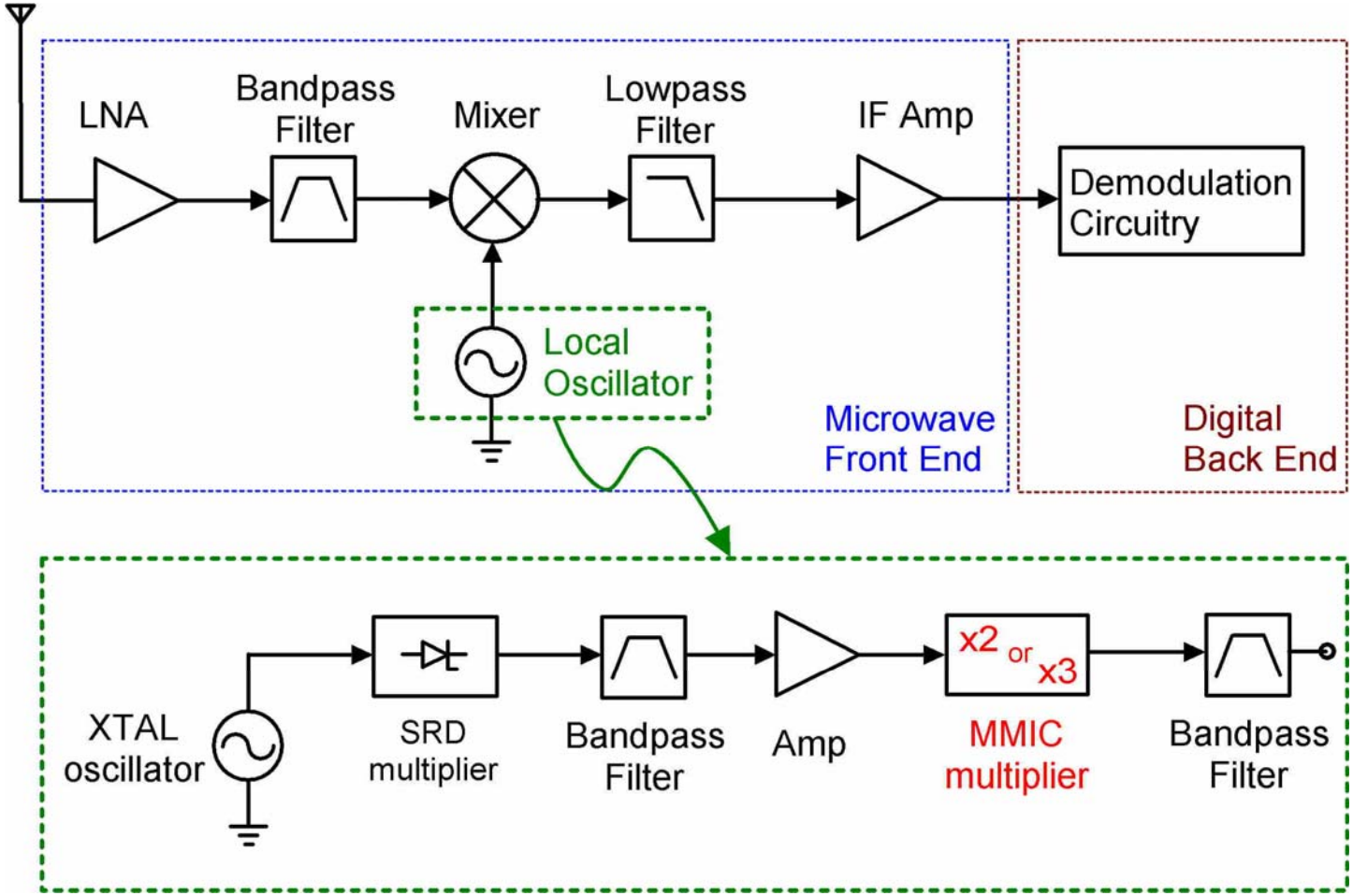
G. Chattopadhyay et. al., IEEE T-MTT, Vol. 52, No. 5, pp. 1538-1547, May 2004.

750 GHz diode multiplier



Introduction

Communications Receiver Front-End



Noise Concepts

An oscillator's output has amplitude and phase fluctuations

$$u(t) = A(t)\cos[\omega(t)t] = A(t)\cos\left[\omega_o t + \frac{d\phi(t)}{dt}t\right]$$

The noise spectral density of the signal is

$$S_\phi(f_m) = 10\log\Delta\phi_{rms}^2 = 20\log\Delta\phi_{rms}$$

After frequency multiplication we obtain

$$v(t) = B_0\cos\left[n\omega_o t + n\Delta\phi(t)\right]$$

$$S_\phi^{(n)}(f_m) = 20\log(n\Delta\phi_{rms}) = 20\log n + 20\log\Delta\phi_{rms}$$

phase noise degradation
relative to input signal

Noise Concepts

Why frequency multiplication is “worth it”

- Typical phase noise (PN) of a 10 MHz Crystal Oscillator:

  -170 dBc/Hz @ 100 kHz offset

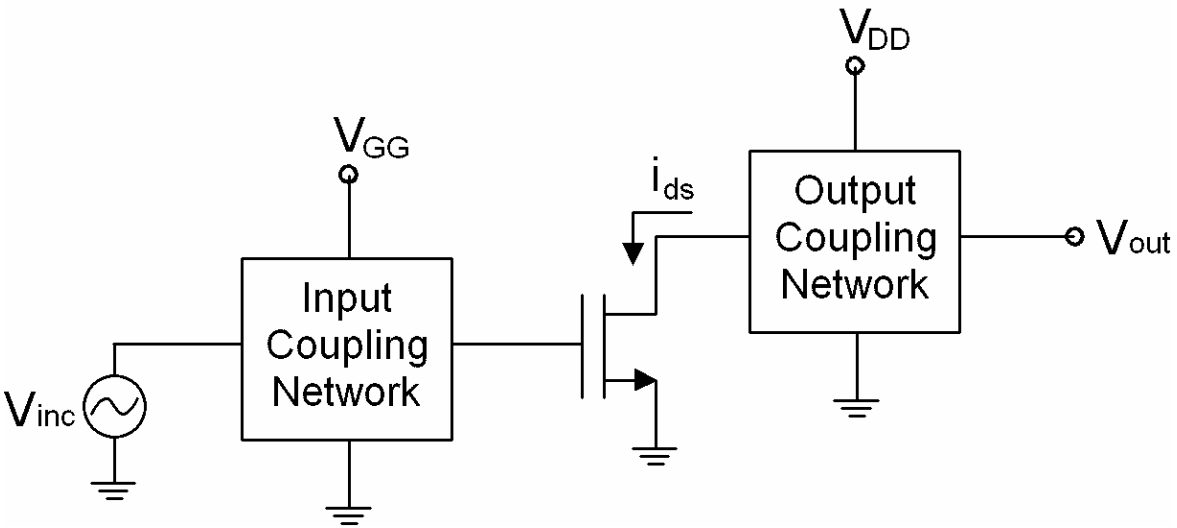
- Using a multiplier chain to get a 2.4 GHz signal degrades this phase noise by 20log(240) = 48 dB, yielding:

  -170 dBc/Hz + 48 dB = -122 dBc/Hz

- Compare this to an on-chip LC-tank oscillator at 2.4 GHz which has a typical PN of -100 dBc/Hz @ 100 kHz offset

Multiplier Techniques

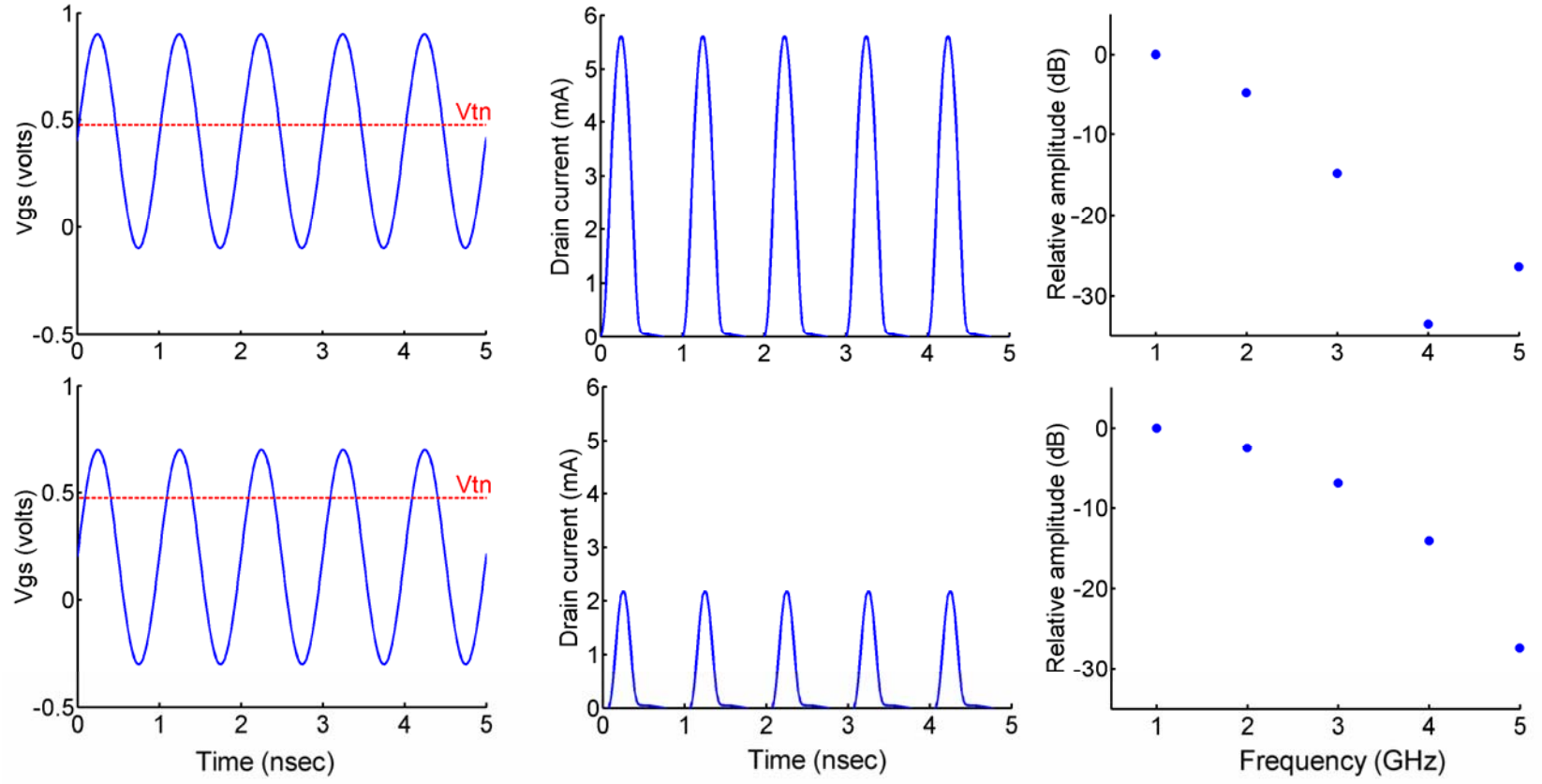
Classic FET multiplier topology [6]



$$i_{ds} = I_{DS} + \sum_{n} I_n e^{j\omega nt}$$ where: $$I_n = I_{pk}\frac{4t_0}{\pi T}\left|\frac{\cos(n\pi t_0/T)}{1-(2nt_0/T)^2}\right|$$

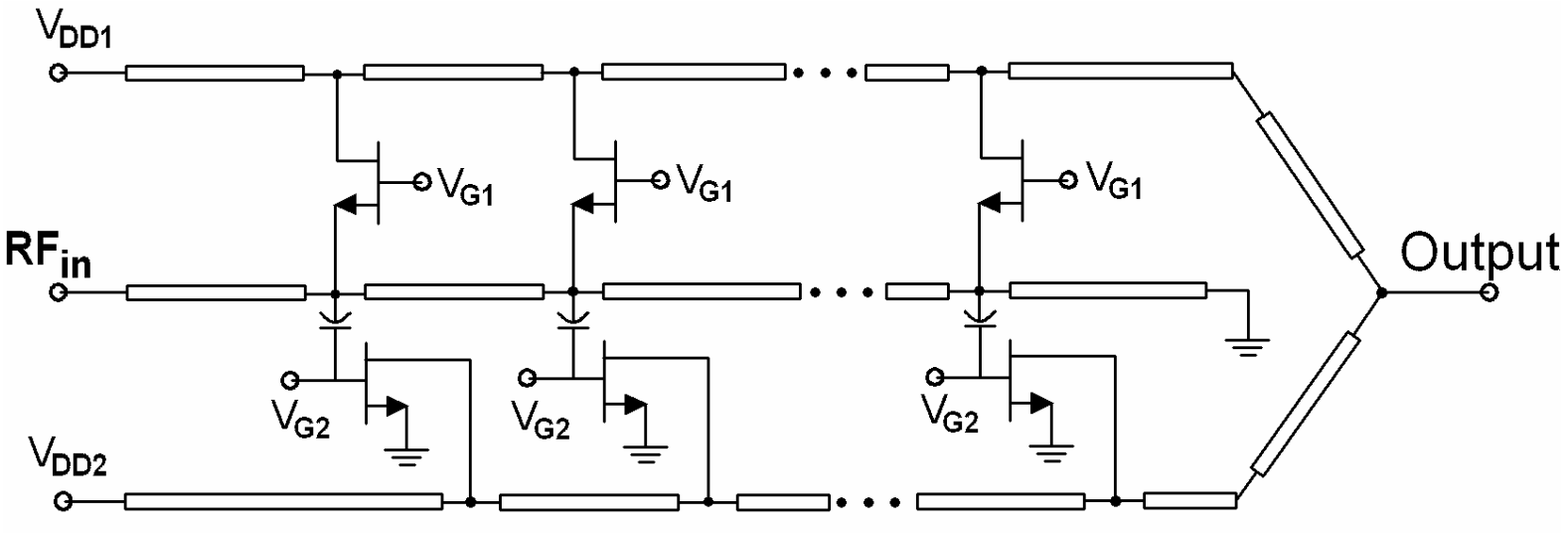
Multiplier Techniques

Harmonic Generation using a FET



Distributed Multipliers

Broadband Multiplier Designs



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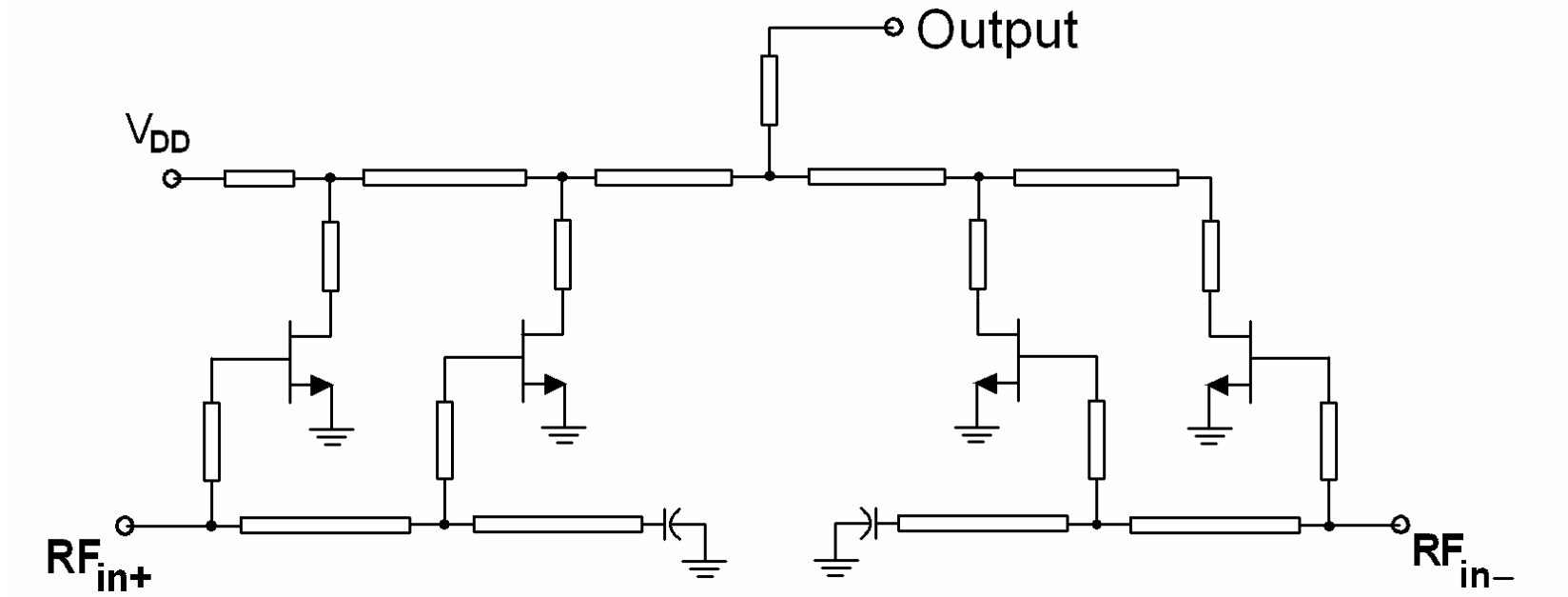
Distributed Multipliers

Broadband Multiplier Designs



K. L. Deng and H. Wang, “A Miniature Broad-Band pHEMT MMIC Balanced Distributed Doubler,” *IEEE Trans. Microwave Theory Tech.,* Vol. 51, No. 4, pp. 1257-1261, April 2003.

Frequency Tripler

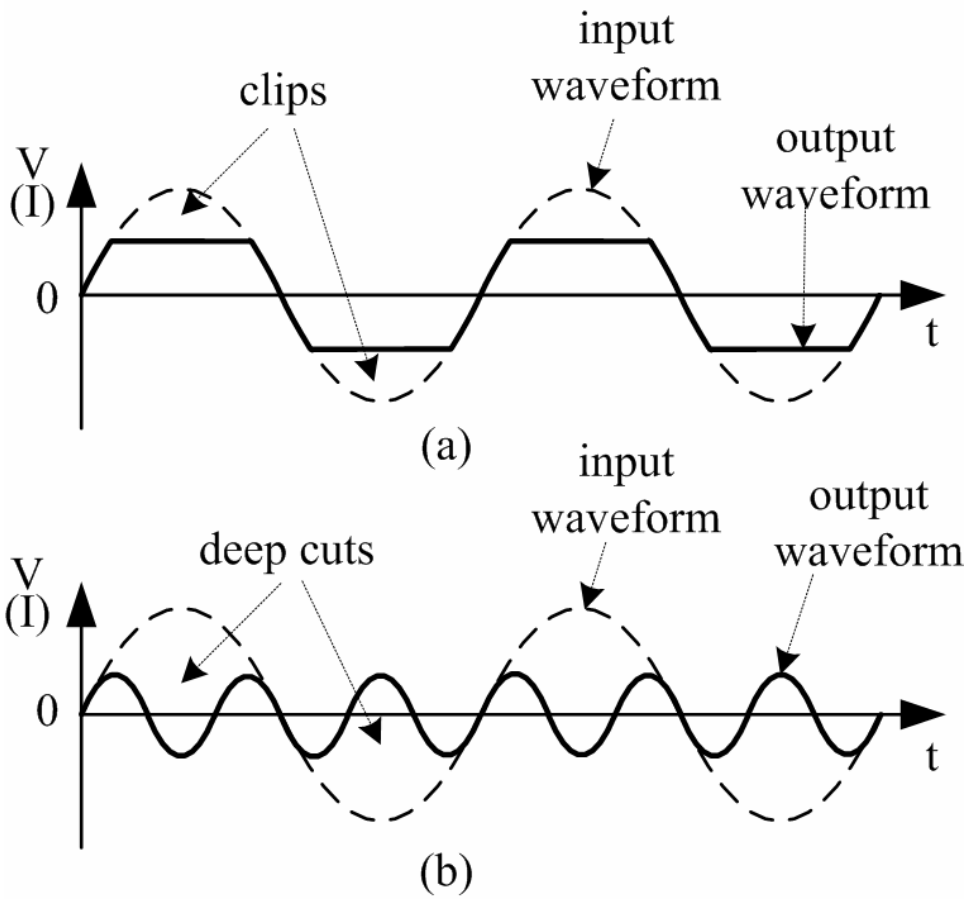
New Concepts in Tripler Design

Typical approach:

clip a sinusoid to generate lots of harmonics and then filter what is not needed

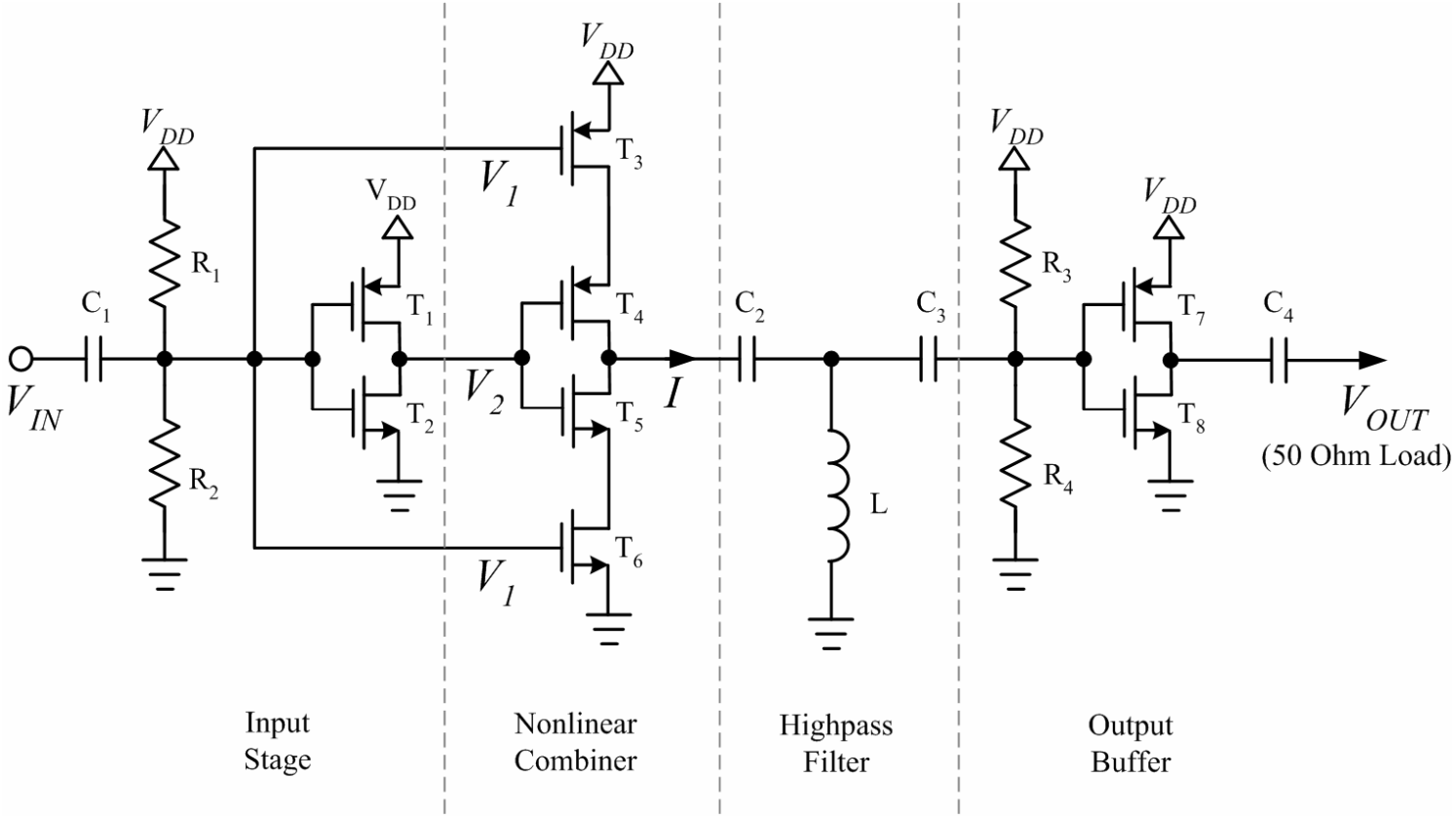
Wave-shaping technique:

make “deep cuts” in the wave to enhance the third harmonic only



Frequency Tripler

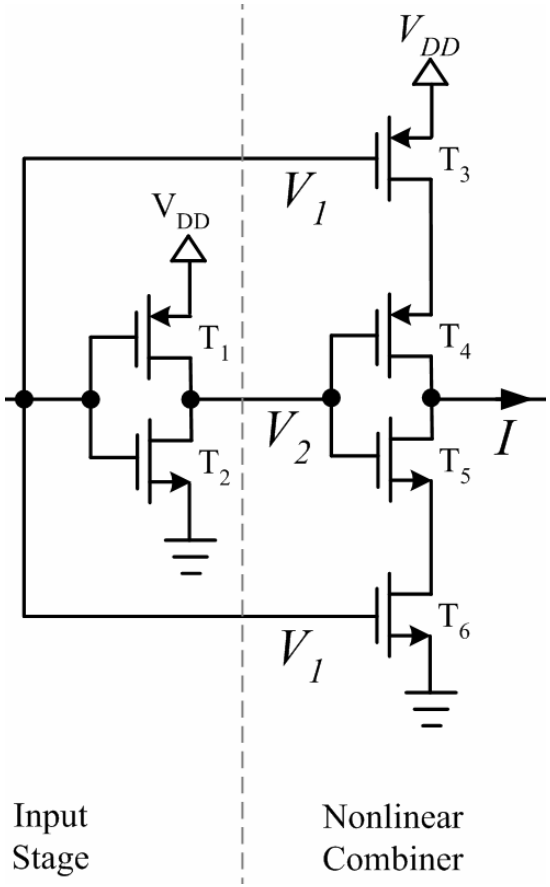
Tripler Circuit Implementation

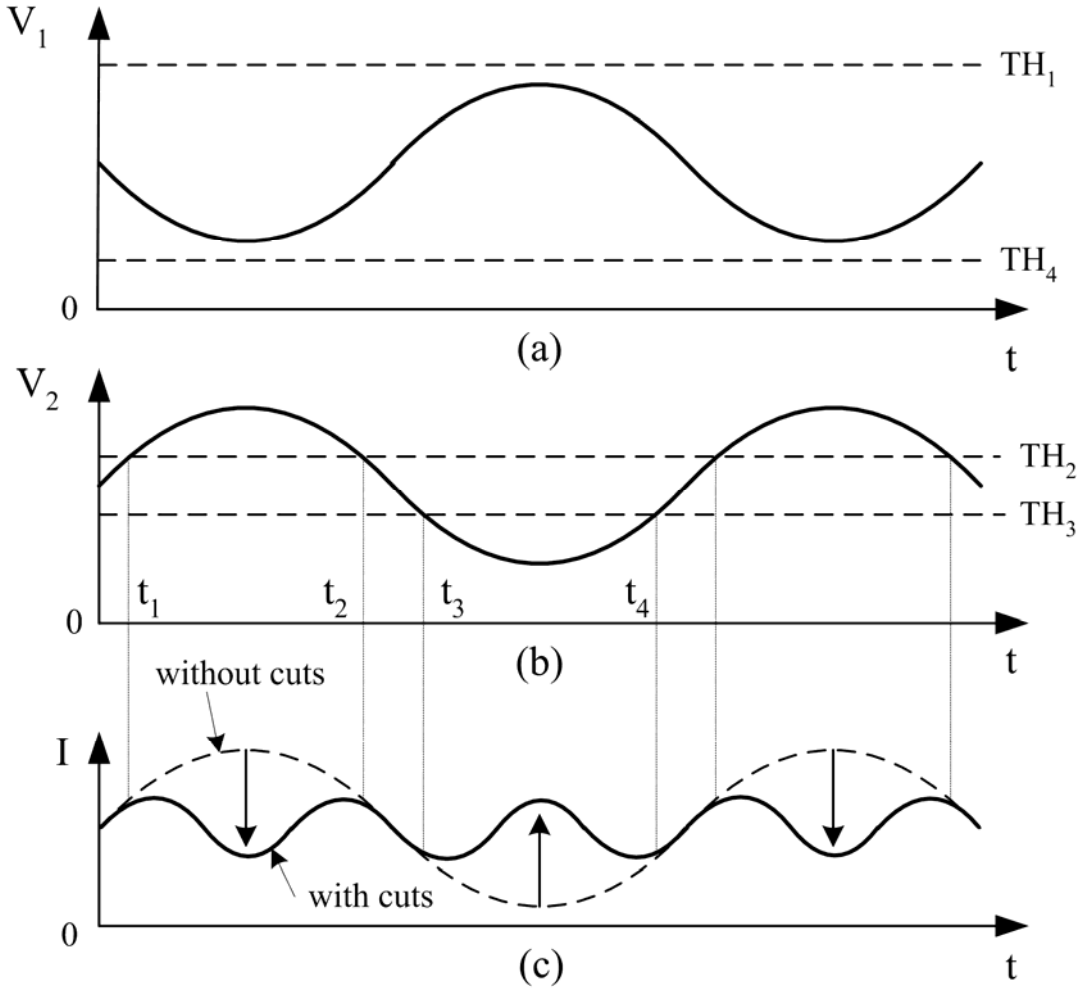


You Zheng and C. E. Saavedra, "A Broadband CMOS Frequency Tripler using a Third-Harmonic Enhanced Technique," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 10, pp. 2197-2203, 2007.

Frequency Tripler

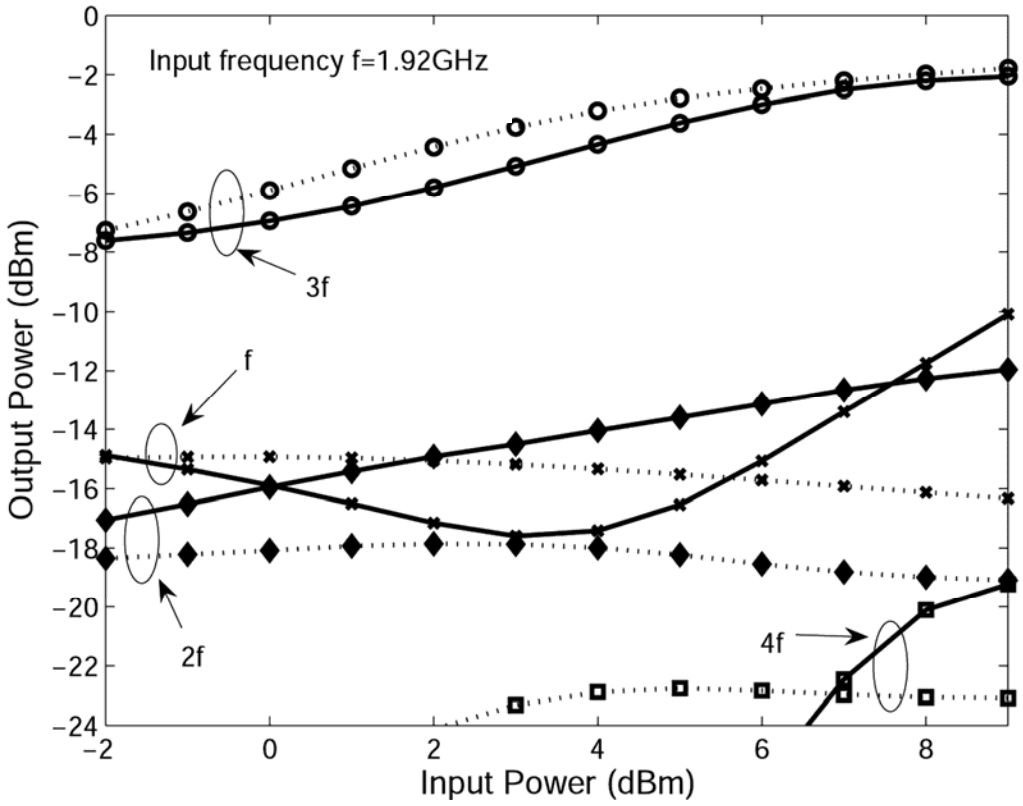
Circuit Core





Frequency Tripler

Measured Results



Conversion Loss = 9.5 dB

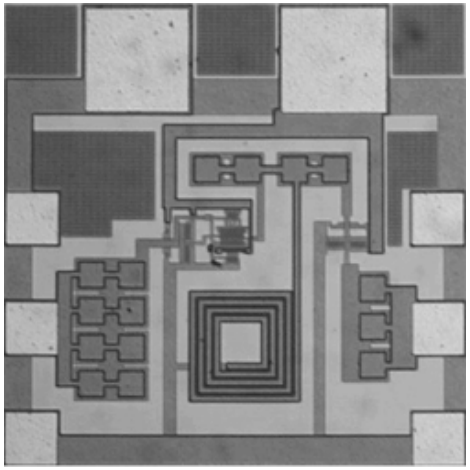
Phase Noise Degrad. = 9.75 dB

Theoretical minimum is 9.54 dB

Fundamental Rejection > 11 dB

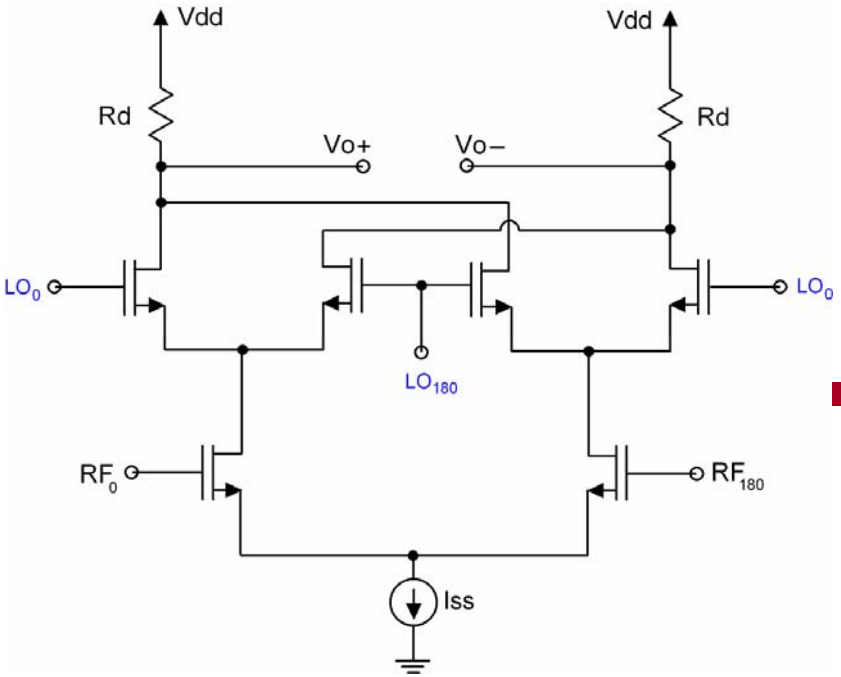
2^{nd} Harmonic Rejection > 9 dB

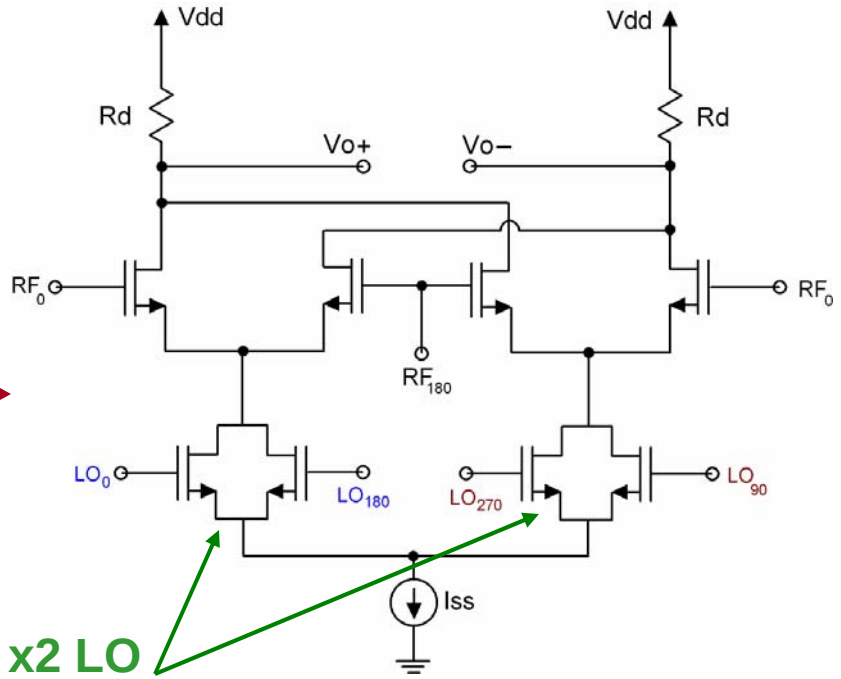
4^{th} Harmonic Rejection > 20 dB



Mixers with LO multiplication

Active x2 Subharmonic Mixer (SHM)

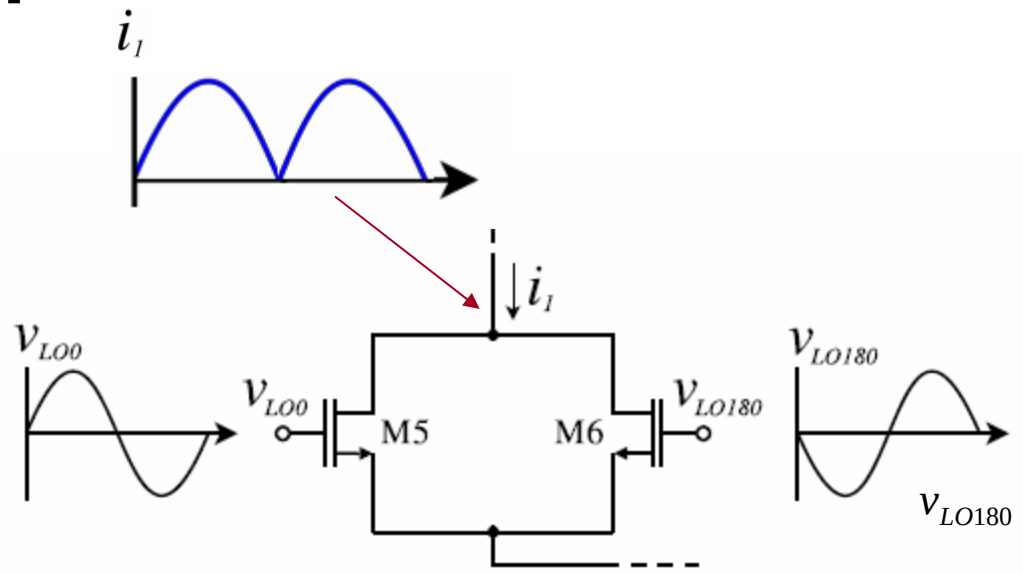




Standard Gilbert Cell

Mixers with LO multiplication

x2 SHM Operation Details



$v_{LO0} = A_{LO}\sin(\omega_{LO}t)$

$v_{LO180} = A_{LO}\sin(\omega_{LO}t - \pi)$

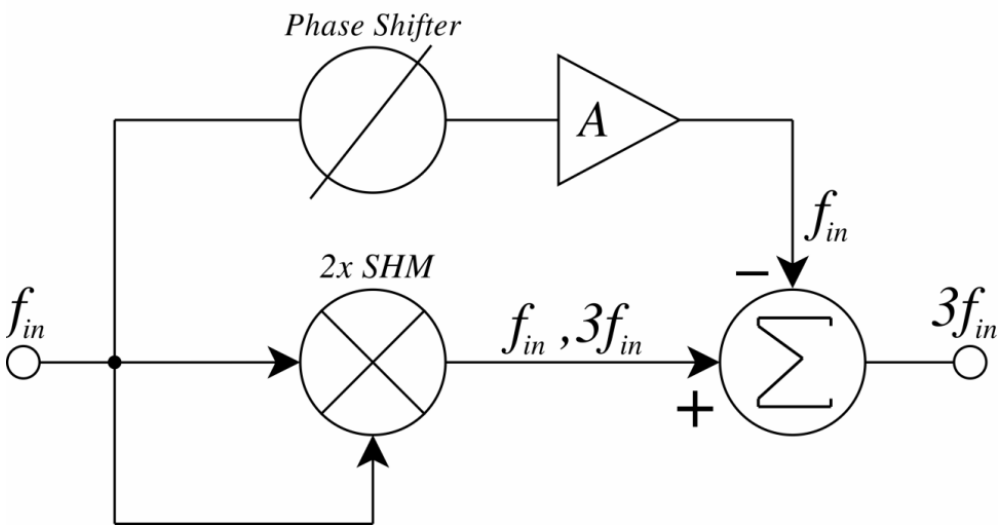
$$i_1 = i_a + i_b = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(v_{LO0}^2 + v_{LO180}^2)$$

$$i_1 = \mu_n C_{ox}\frac{W_1}{L}(V_{GS(LO)} - V_t)^2 + \mu_n C_{ox}\frac{W_1}{L}v_{LO0}^2$$

Using the relationship, $v_{LO0}^2 = v_{LO180}^2$

Recent Advances

Frequency Multiplication using SHM's



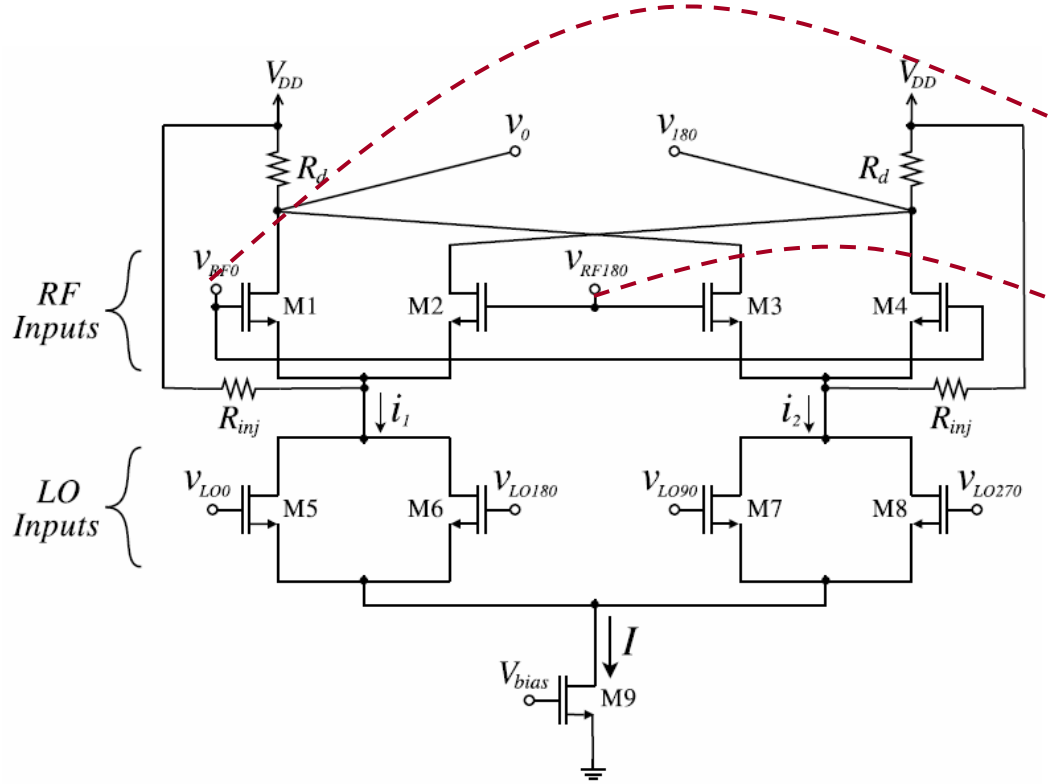
odd-order frequency multipliers can be conveniently designed

Frequency Tripler with Fundamental Signal Cancellation ⇨ No output filtering needed

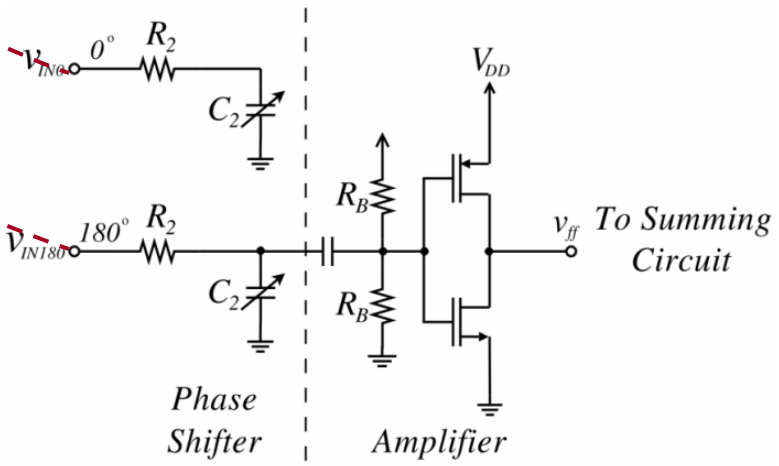
B. R. Jackson, F. Mazzilli and C. E. Saavedra, "A Frequency Tripler using a Subharmonic Mixer and Fundamental Cancellation," *IEEE Transactions on Microwave Theory and Techniques,* Vol. 57, No. 5, pp. 1083-1090, May 2009.

Recent Advances

Frequency Tripler Design



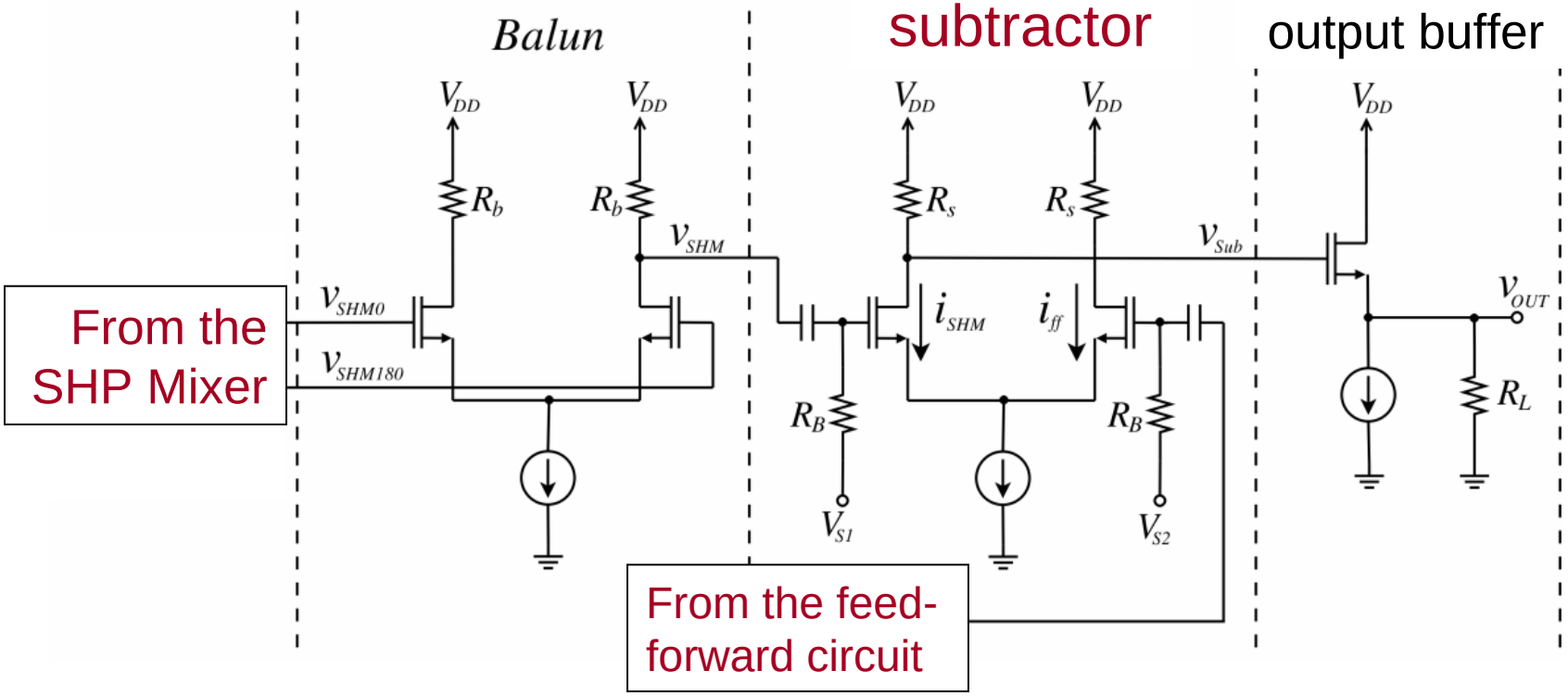
x2 Subharmonic Mixer



The feedforward path:
Phase Shifter & Amplifier

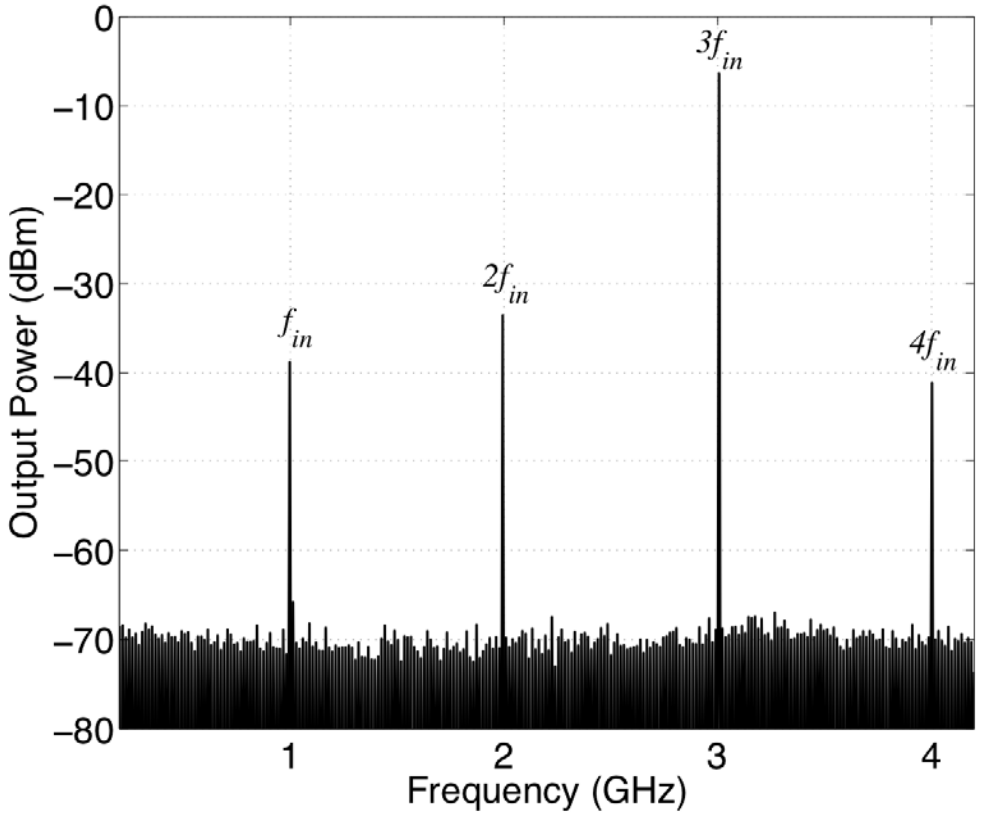
Recent Advances

Frequency Tripler Design – cont'd

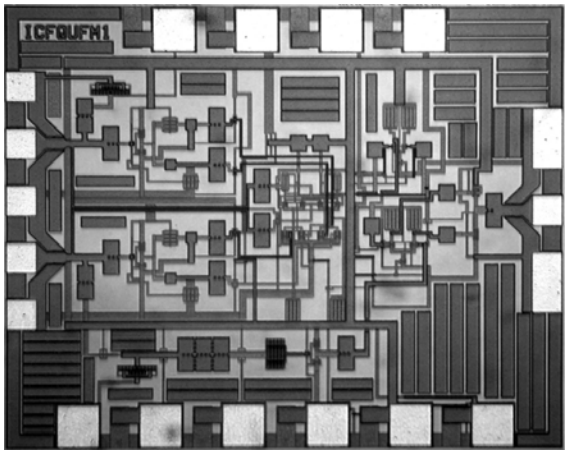


Recent Advances

Measured output spectrum

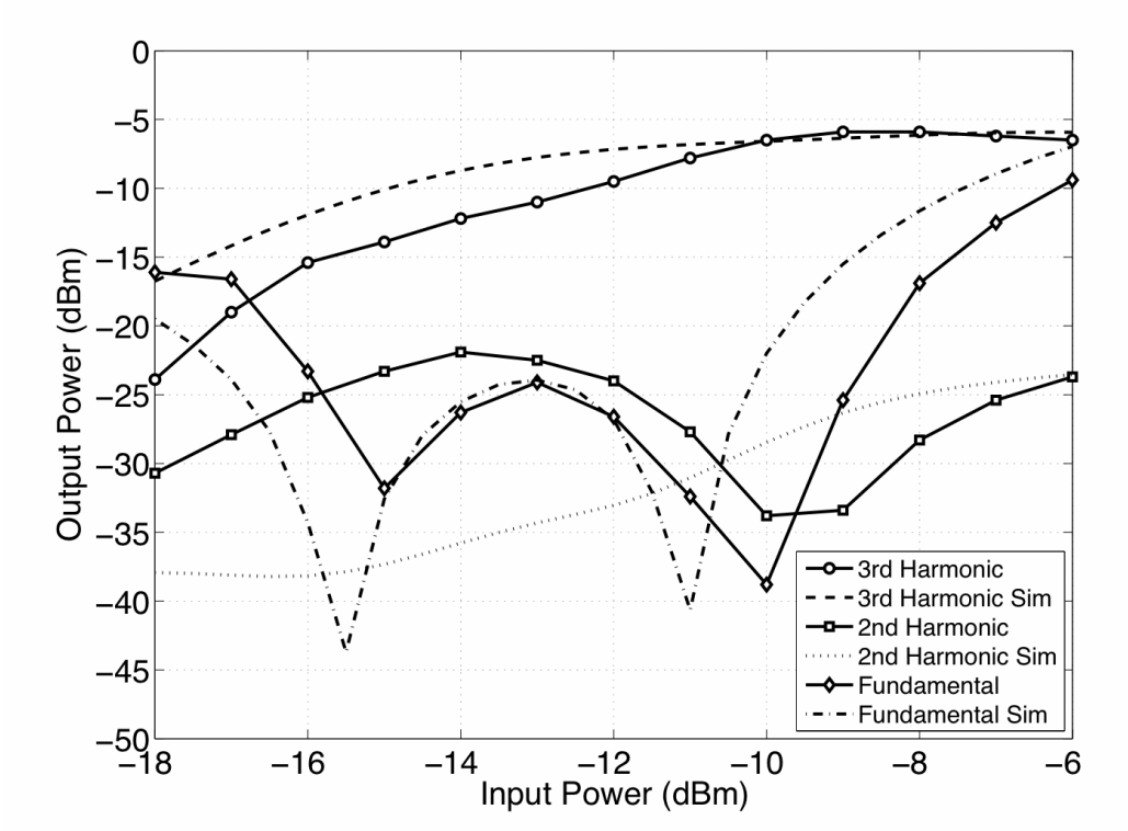


Input Freq.	1 GHz
Input power	-10 dBm
Output Freq.	3 GHz
Conv. Gain	3 dB
Fund. Reject.	30 dB



Recent Advances

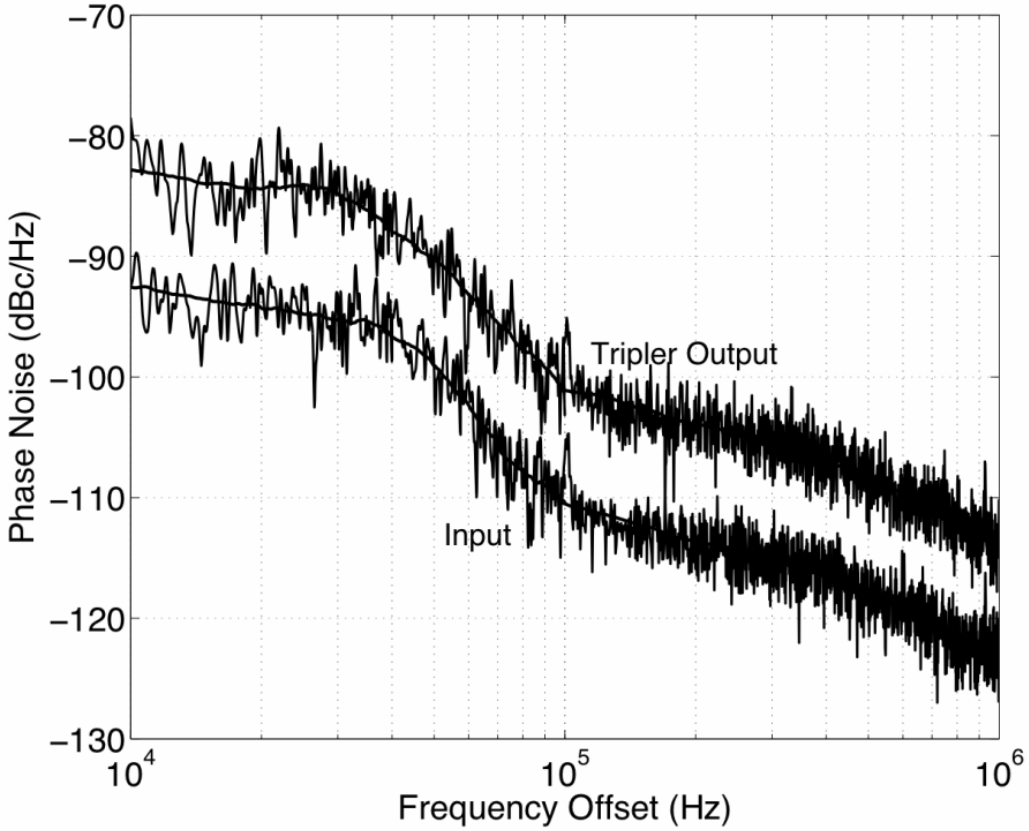
Measured power performance



High suppression of the fundamental and other harmonics achieved without on-chip or off-chip filtering.

Recent Advances

PN Degradation Performance



Phase noise degradation:

9.69 dB

Theoretical minimum:

$$20\log(3) = 9.54 \quad dB$$

Conclusion

- Local Oscillator signal generation is a key driving force behind frequency multiplier design
- Multiplying a very stable low-frequency reference signal can still produce signals with better phase noise than producing them on-chip in the microwave range
- Wave-shaping techniques can be exploited to generate odd-order multipliers
- Recent advances in multiplier design have led to highly compact circuits with excellent fundamental rejection that do not require output filtering

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6. S. A. Maas, *Nonlinear Microwave Circuits*, Artech House: Boston, 1988.
7. B. Schiek, I. Rolfes and H. J. Siweris, *Noise in High-Frequency Oscillators*, Wiley: Hoboken, New Jersey, 2006.

About the Speaker

Carlos Saavedra received the Ph.D. and M.Sc. degrees from Cornell University and the B.Sc. degree from the University of Virginia. From 1998-2000 he was with Millitech Corporation and in the year 2000 he joined Queen's University where he is now Associate Professor of Electrical and Computer Engineering and the Coordinator of Graduate Studies. Prof. Saavedra is a member of the Technical Program Committee of the IEEE RFIC Symposium and is the Vice-Chair of the MTT-S Technical Committee 22 on Signal Generation and Frequency Conversion. He is a Senior Member of the IEEE.

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