Low-Noise Downconverters through Mixer-LNA Integration

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Outline



- Motivation
- Theory

> understanding noise in double-balanced (Gilbert-cell) CMOS active mixers.

- Design studies:
 - > broadband low-noise mixer.
 - > low-noise self-oscillating mixer using a balanced VCO load.





Design study # 1:

A broadband noise-cancelling mixer



Design study # 1



- For the RF stage, select an LNA topology
- Two basic LNA families in wide use today are:
 - noise-cancelling LNA's [7]
 - LNA's with inductive degeneration
- Several noise optimization techniques exist if an LNA with inductive degeneration is chosen:
 - simultaneous noise and input matching technique [9]
 - power constrained noise optimization [10]
 - power constrained simultaneous noise and input matching [11]



- A noise-cancelling RF stage is attractive when the mixer is expected to operate over a wide frequency band.
- As a result of the noise-cancelling action, these LNA's do not require too many inductors, if any, to function and, therefore, they can occupy a very small area on-chip.







Full mixer schematic



MONTRÉA



Low-noise RF stage



Half-circuit

- The signal voltages at nodes x and y are in-phase, but...
- The noise voltages at x and y are out-of-phase
- Thus, the noise currents from M1 subtract at node *z*:

$$\frac{|i_{n_{mn}\text{out}}|^2}{=} \frac{|g_{m3}V_x - g_{m2}V_y|^2}{|i_{n_{mn}}|^2} (g_{m3}R_S - g_{m2}R_1)^2$$

• The key design equation is:

$$g_{m2} = (R_S/R_1)g_{m3}$$





The transconductor's input impedance and gmeff are,

The noise currents associated with the transconductor are,

1100

$$Z_{\rm in} \approx \frac{r_{o1} + R_1}{1 + (g_{m1} + g_{mb1})r_{o1}} \qquad g_{m_{\rm eff}} = g_{m3} + g_{m2} \left[\frac{1 + (g_{m1} + g_{mb1})r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right]$$

se currents associated with the nductor are,
$$g_{m_{\rm eff}} = g_{m3} + g_{m2} \left[\frac{1 + (g_{m1} + g_{mb1})r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right]$$

$$\overline{|i_{nt_{added}}|^2} = g_{m2}^2 4kTR_1 + \frac{4\kappa T\gamma}{\alpha} (g_{m2} + g_{m3}) + \overline{|i_{n_{mn}}|^2} (g_{m3}R_S - g_{m2}R_1)^2$$

$$\overline{|i_{nout_{in}}|^2} = \frac{4kT}{R_S} (Z_{in} ||R_S)^2 g_{m_{eff}} \qquad \overline{|i_{n_{mn}}|^2} = \frac{i_{nd}}{1 + \frac{R_1 + R_S}{r_{o1}} + (g_{m1} + g_{mb1})R_S}$$

and its NF is,
$$F = 1 + \frac{\overline{|i_{nt_{added}}|^2}}{\overline{|i_{nout_{in}}|^2}} \approx 1 + \frac{R_S}{R_1} + \frac{\gamma}{\alpha} \left(\frac{R_S}{R_1} + 1\right) \frac{1}{g_{m3}R_S}$$



- Current bleeding circuit has multiple benefits:
 - allows for different bias currents in the LO and the RF stage.
 - LO switches can be biased with a low overdrive voltage and they can turn ON & OFF more quickly
 - helps with 1/f noise
- Peaking inductor helps extend the frequency response of the mixer.









<u>Measurements</u>





<u>Measurements</u>







CMOS Technology	0.13 μm
RF Frequency Span (GHz) 3 dB Bandwidth	1 - 5.5
Conversion Gain (dB)	17.5 (Power)
NF (DSB) (dB)	3.9 (Average)
P_{1dB} (dBm)	-10.5
IIP3 (dBm)	+0.84
LO - to - RF Isolation (dB)	> 55
S_{11} (dB)	< -8.8
Core Size (mm ²)	0.315
Voltage Supply (V)	1.5
Power Consumption (\mathbf{mW})	34.5

S. S. K. Ho and C. E. Saavedra, "A CMOS Broadband Low-Noise Mixer with Noise Cancellation", *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1126-1132, May 2010.





Design study # 2:

Low-noise self-oscillating mixer (SOM) using a balanced VCO load



Design study # 2



Monolithic integration gives RFIC designers the ability to merge different transceiver components to create a more compact solution that saves dc power and chip area.

Enter....

self-oscillating mixers

SOM's can be implemented using different configurations that can result in interesting design possibilities.



Design study # 2







The RF transconductor

- An LNA-type structure using the simultaneous noise and input match technique is chosen for this design.
- Devices M7 and M8 are for current bleeding, whose benefits were discussed in Design Study #1.



 L_{shunt} resonates with the tail capacitance of the switching core and therefore helps to alleviate 1/f noise.





Oscillator subcircuit – design choices

- Where to connect the oscillator to the mixer? (already discussed on p. 30)
- Which type of oscillator topology to use?
- Within the LC-tank oscillator family, topologies abound. Yet, if oscillator tunability is desired, the general circuit to the right is a good candidate.





- The oscillator on the previous slide has a single tail current, yet the mixer in question needs to see a balanced load.
- This can be fixed by realizing that the cross coupled transistors can be split as shown in the figure below:









Full SOM schematic





- Current flows in the SOM circuit when VLO+ is high.
- Nodes "plus" and "minus" act as a differential terminal for the IF currents.
- The situation is reversed when the LO waveform has the opposite phase.





The mixer's load impedance varies with time. We must model the behavior of that impedance to predict the conversion gain of the mixer.





• Using Fourier analysis, Rload can be written as:

$$R_{\text{load}} = R_{\text{max}} - \frac{2\tau_r}{T_{\text{LO}}} \left(R_{\text{max}} - \frac{1}{2g_{mdc}} \right) - \frac{4\tau A}{T_{\text{LO}}} \frac{\sin(\omega_{\text{LO}}\tau)}{\omega_{\text{LO}}\tau} \frac{\sin(\omega_{\text{LO}}\tau_r)}{\omega_{\text{LO}}\tau_r} \cos(2\omega_{\text{LO}}t) + \cdots$$

where $\tau = T_{LO}/2 - \tau_r$ and $A = R_{max} - 1/2g_{mdc}$

- The effective g_m of the RF stage is: $g_{m_{eff}} = \frac{g_m \omega (L_s + L_g)}{Z_0}$
- The conversion gain of the SOM is: $CG = \frac{2}{\pi} \frac{\sin(\pi f_{\text{LO}} t_{sw})}{\pi f_{\text{LO}} t_{sw}} g_m R_{\text{load}}$
- Keeping only the first terms of Rload leads to:

$$CG_{\rm som} \cong \frac{2}{\pi} \frac{\sin(\pi f_{\rm LO} t_{sw})}{\pi f_{\rm LO} t_{sw}} \frac{g_m \omega (L_s + L_g)}{Z_0} \left[R_{\rm max} - \frac{2\tau_r}{T_{\rm LO}} \left(R_{\rm max} - \frac{1}{2g_{mdc}} \right) \right]$$





Measurements









<u>Measurements</u>







<u>Measurements</u>







<u>Measurements</u>

RF return loss



Technology	0.13 µm CMOS
RF Freq. (GHz)	7.8 - 8.8
Conversion Gain (dB)	11.6
DSB Noise Figure (dB)	4.39 (min)
Input P_{1dB} (dBm)	-13.6
IIP3 (dBm)	-8.3
LO - RF leakage (dBm)	-59
Chip size (mm ²)	0.47 (core)
DC Power (mW)	12 (core)

S. S. K. Ho and C. E. Saavedra, "A Low-Noise Self-Oscillating Mixer using a Balanced VCO Load", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 8, pp. 1705-1712, August 2011.



Final remarks



- To reduce the noise figure of a CMOS double-balanced mixer, the RFIC designer should focus on:
 - minimizing the noise contribution of the RF transconductance stage
 - ensuring that the mixing core is driven by an LO signal with fast transitions
- Any one of a number of LNA topologies can be used for the RF stage of the mixer. A noise-cancelling configuration, for example, can produce very broadband operation.
- Incorporating current bleeding into the mixer can help reduce 1/f noise and it also gives the designer more freedom to chose the bias currents in the RF and LO stages.
- SOM's, in which a mixer, an LNA and an oscillator are merged into one unit open innovative design opportunities.



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