A Microwave Frequency Divider Using an Inverter Ring and Transmission Gates

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Abstract—In this letter, a divide-by-four frequency divider is presented that uses a CMOS inverter ring interspersed with transmission gates. The presence of the transmission gates prevents the inverter ring from oscillating. The signal to be divided is applied to the control voltage to the transmission gates. The integrated circuit operates at an input frequency of 2.2 GHz and yields an output signal at 0.55 GHz. The power dissipation is 14.4 mW. The IC was fabricated using 0.18 μm CMOS technology.

Index Terms—Frequency divider, inverter ring, RF CMOS, transmission gates.

I. INTRODUCTION

A FREQUENCY divider circuit takes a periodic input signal and generates a periodic output signal at a frequency that is a fraction of the input signal. The input waveform can be either analog or digital. Frequency dividers are found in phase-locked loops, phase shift keying demodulators, and frequency synthesizers, to name a few prominent applications.

Analog divide-by-two frequency dividers operating on the principle of regenerative feedback [1] have been demonstrated for frequencies well into the millimeter-wave range [2]. Other analog divider implementations use the mechanism of injection locking [3], [4].

Most digital frequency dividers can also operate with analog input signals. Some of the more mature CMOS digital dividers use cross-coupled toggle flip-flops in a feedback configuration implemented with D-latches [5]–[7]. These are called "static" frequency dividers. With this approach, a division ratio of 2 is obtained. A diverse number of dividers use the D-latch approach have been suggested and the differences between them relate to how the latches are actually implemented. In contrast to the static dividers, circuits using dynamic CMOS logic have also been suggested [8].

A different method for achieving frequency division in the analog/digital domain consists of using a chain of inverters. In [9] this mechanism is used to implement a basic divide-by-two and a divide-by-four system. In [10] a variation of the inverter chain is used to implement a high-speed divide-by-two system as a building block for a 64:1 divider. In this work, a CMOS divide-by-four divider is implemented operating at an input frequency of 2.2 GHz and yielding an output signal at 0.55 GHz.

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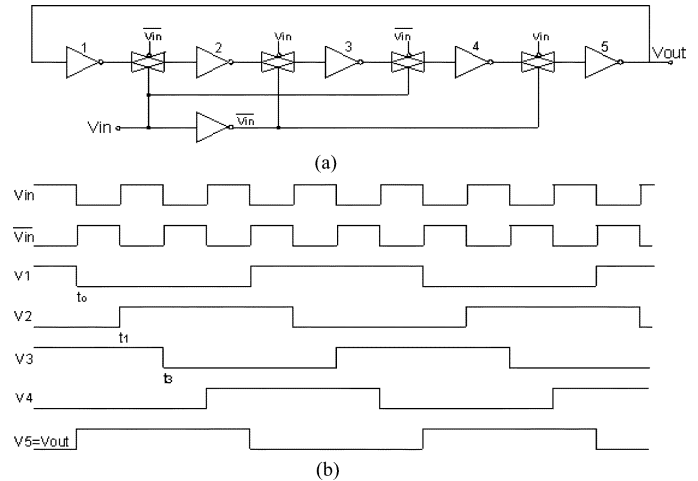
Fig. 1. Divide-by-four frequency divider (a) block diagram and (b) timing diagram.

The divider uses an inverter ring approach. In comparison to the circuits in [9], this divider uses less inverters. The upper frequency limit of this inverter is easily modeled as compared with other circuits.

II. CIRCUIT DESCRIPTION

The suggested frequency divider is shown in Fig. 1(a). The circuit consists of a ring of five CMOS inverter circuits separated by transmission gates. It is well known that an odd number of inverters arranged in a ring configuration is unstable and will tend to oscillate. In the circuit illustrated in Fig. 1, however, the presence of the transmission gates (TGs) prevents the oscillations because the gates separate one inverter from the other, thereby breaking the feedback loop. The input signal, Vin, and its complement are the control signals to the transmission gates. Suppose that the output of inverter 1 changes state from logic 1 to 0. This change in states will propagate through the inverter chain at a rate determined by the input clock frequency, Vin. Since there are four transmission gates, it will take four clock periods for the change in state to propagate through the chain. Thus the output signal, Vout, changes states only after every four cycles of Vin and thus frequency division is achieved. Fig. 1(b) depicts representative waveforms in this frequency divider. The top two waveforms are the input signal and its complement. The subsequent signals are the outputs of each inverter. Assume, for instance, that the first inverter is at logic 1 and transitions to logic 0 at t_0. Because the first transmission gate is off, the change in logic states in inverter 1 will not propagate to inverter 2 until time t_1. In a similar fashion, the change in the output of inverter
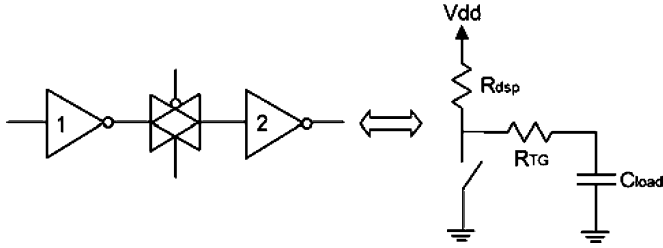
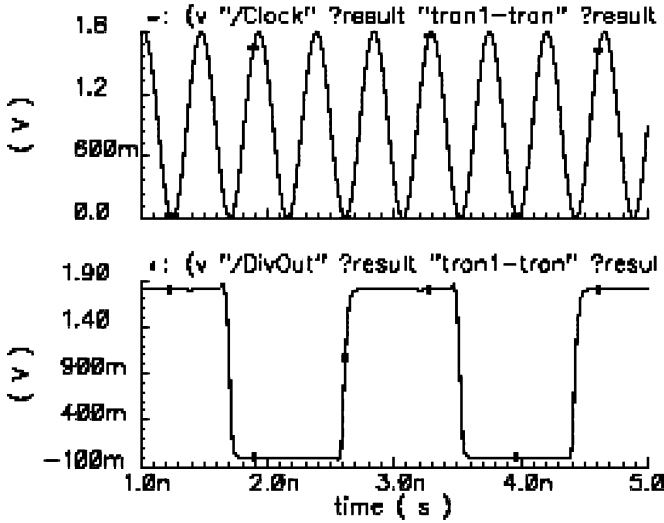Fig. 2.   Circuit model for an inverter-transmission gate-inverter cascade.

Fig. 3.   Post-layout time-domain simulation of the frequency divider using the Cadence Spectre simulator.

Fig. 4.   Experimental results (a) input signal at 2.2 GHz and (b) output signal at 0.55 GHz and its harmonic at 1.1 GHz.

2 will not reach inverter 3 until the second transmission gate is on, which occurs at time t_3. Continuing in this manner, it is seen that the output of any given inverter will only experience one full cycle after there have been four input cycles.

An interesting additional result of this circuit is that the outputs of the inverters 1 and 3 are offset by 90° from each other and inverters 2 and 4 are also offset by 90°. The end-result is that this frequency divider generates waveforms that are in quadrature with one another, which can be very useful in a variety of communications systems such as phase shift-keying demodulators.

The circuit presented in this work was implemented using 0.18 μm CMOS technology. In the logic inverters, the NMOS and PMOS devices were scaled such that $(W/L)_p = 1.5(W/L)_n$. The same scaling ratio was used for the transmission gates. The upper frequency limit of this type of frequency divider depends on the propagation delay through the inverters and the transmission gates. Consider the simplified circuit model for an inverter and a transmission gate cascade shown in Fig. 2. Here, inverter 1 is charging up the load capacitance (C_{load}) represented by inverter 2 through the PMOS resistor, R_{dsp}, and the ON resistance of the transmission gate, R_{TG}. The duration of the clock signal applied to the transmission gate has to be long enough for the voltage across C_{load} to reach at least $V_{dd}/2$, which is the threshold voltage for the switching of the next inverter gate. Otherwise, inverter 2 will not change states and the frequency divider will cease to operate. The resistance R_{ds} for a PMOS or NMOS device is $R_{ds} = (di_d/dV_{ds})^{-1}$, and the load capaci-

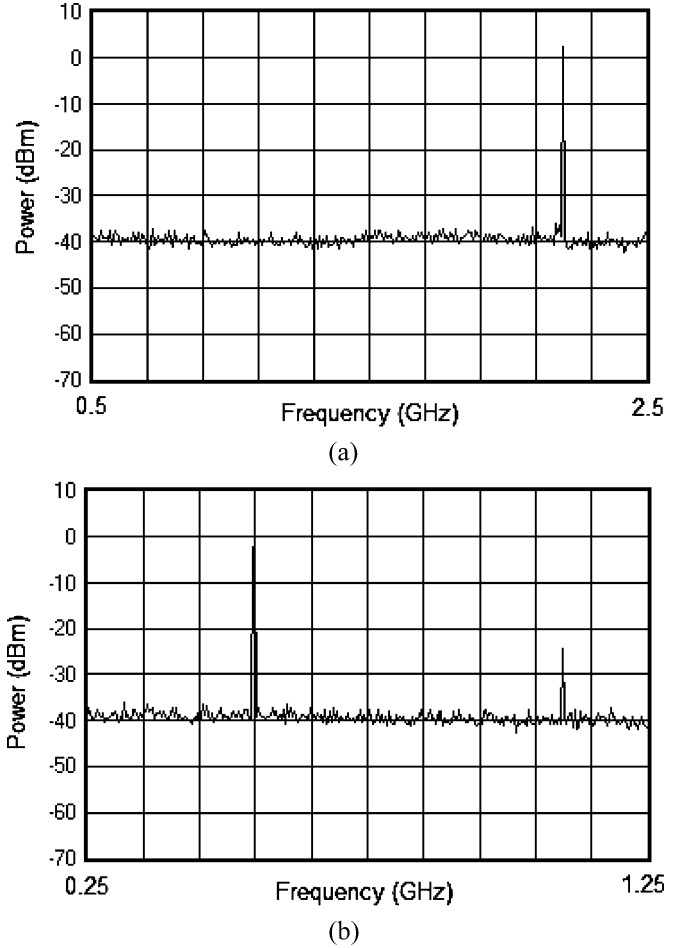tance is given, to a first approximation, by $C_{ox}(W_n L_n + W_p L_p)$, where W and L are the width and length of the inverter transistors. The resistance R_{TG} is equal to $R_{\text{eq,n}} \parallel R_{\text{eq,p}}$, where $R_{\text{eq,n}}$ and $R_{\text{eq,p}}$ are the NMOS and PMOS equivalent resistances and they depend on the time-varying voltage across C_{load} [11].

III. SIMULATION AND EXPERIMENTAL RESULTS

The circuit in Fig. 1 was first simulated using Agilent's Advanced Design System. After the ADS simulations were successful, the circuit was laid out using Cadence Virtuoso. A post-layout circuit extraction was performed and the frequency divider was again simulated in the time-domain. The results of that simulation are depicted in Fig. 3. The top trace shows the input signal with a frequency of 2.2 GHz, an amplitude of 0.9 V and a dc offset of 0.9 V. The bottom trace in Fig. 3 is the output signal of the frequency divider with a frequency of 0.55 GHz, or a period of 1.82 ns.

Experimental results from the fabricated integrated circuit are presented in Fig. 4. The input frequency was set to 2.2 GHz and a dc bias was superimposed on the RF signal using a bias tee. Fig. 4(a) shows the spectrum of the input signal and Fig. 4(b) depicts the spectrum of the divide-by-four output signal. In addition to the fundamental at 0.55 GHz, the output signal has harmonics, which can be easily filtered out if the desired signal is
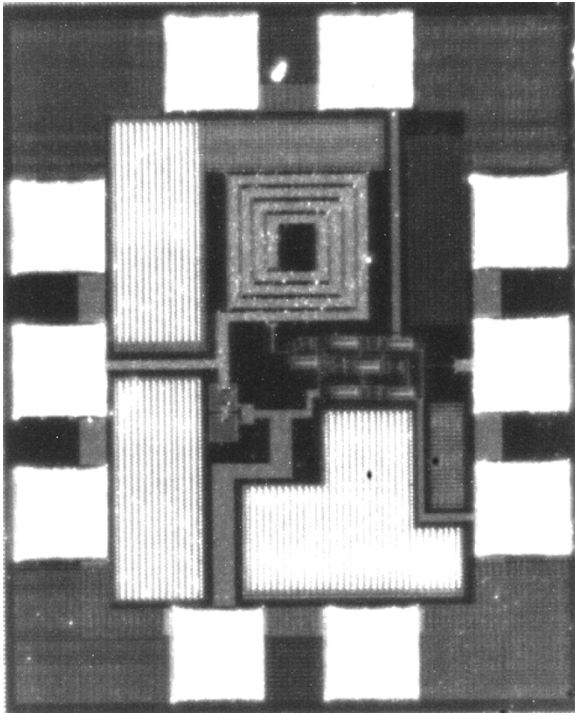
of 2.2 GHz. The power dissipation is 14.4 mW. Using a similar topology, higher division ratios are possible, such as divide-by-eight with a ring of seven inverters interspersed with six transmission gates.

Fig. 5. Integrated circuit microphotograph.

a sinusoid. This integrated circuit consumes 14 mW of power, and measures 720 μm by 600 μm including the bonding pads. A photograph is shown in Fig. 5.

IV. CONCLUSION

In this work, a divide-by-four frequency divider has been designed and tested. The divider operates at an input frequency

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