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A wideband quadrature generator IC using a varactor-compensated feedback network

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Abstract In this paper a novel quadrature generator is presented that exhibits a 110% operating frequency bandwidth. Existing circuits are unable to provide a quadrature signal over such a large fractional bandwidth. They are also highly susceptible to component tolerances that can often shift the center operating frequency rendering the circuit unusable. In this work, this issue is mitigated with the use of a negative feedback network that is able to actively compensate the circuit using varactors to match the operating frequency. In this manner, the bandwidth of the quadrature generator can be significantly increased. Simulation results show an operating frequency span from 1 to 6 GHz while maintaining a phase error below 5° and ±2 dB in amplitude error. The circuit, without bonding pads, uses an area of only 0.17 mm^2.

Keywords Quadrature generator · Feedback · Varactor · Wideband · RF

1 Introduction

In many transceivers, quadrature signals are produced using either a quadrature oscillator or a quadrature generator in conjunction with a basic oscillator. One example of a quadrature oscillator is the cross coupled quadrature oscillator. This circuit is composed of two VCOs coupled together in order to achieve a quadrature output [1, 2]. However, since this design requires the use of two identical oscillators, this effectively doubles its power consumption and occupied area.

Another method to generate a quadrature signal is the use of a differential oscillator at twice the desired frequency. A divide-by-two frequency divider is then used to generate the quadrature signals [3]. The advantage to this approach is that there is a very low phase error. however the issue with this design is that the oscillator needs to generate a signal at twice the frequency. This is difficult to achieve at the lower end of the microwave spectrum (≤15 GHz).

The RC-CR or a polyphase network [4, 5] has the ability to produce quadrature signals over a wide bandwidth. However, their limitation is that they are unable to maintain the amplitude balance between the quadrature signals with respect to the frequency. In this paper, we remove this limitation by using a pair varactors within the RC-CR network to actively match the frequency of operation. This novel approach results in a very wideband quadrature signal generator with a 140% bandwidth at 3 GHz.

2 Circuit description

The basic RC-CR quadrature phase generator depicted in Fig. 1. has the severe restriction that it is only able to provide a perfect amplitude balance at one specific frequency ($\omega = 1/RC$).

If the resistance is held constant then the capacitance required to maintain amplitude balance over frequency is shown in Fig. 2 for the case that $R = 180\ \Omega$. Thus, if a varactor is substituted for the capacitor, the capacitance can be tuned to match the amplitude across a large bandwidth. The only limitation of this circuit is in the available tuning range of the varactors.

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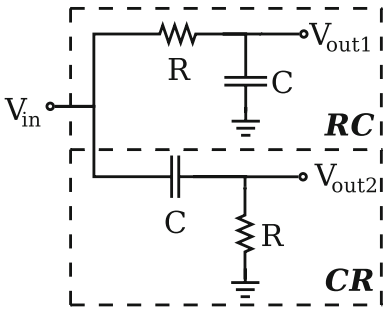


Fig. 1 RC-CR quadrature generator

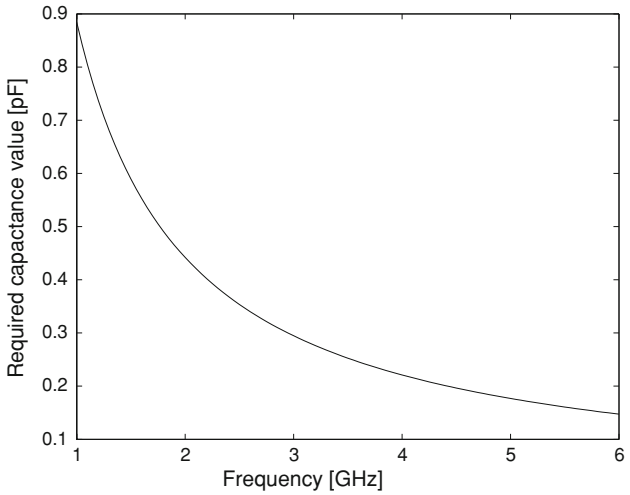


Fig. 2 Required capacitance value to maintain amplitude balance if resistance is set to 180 Ω

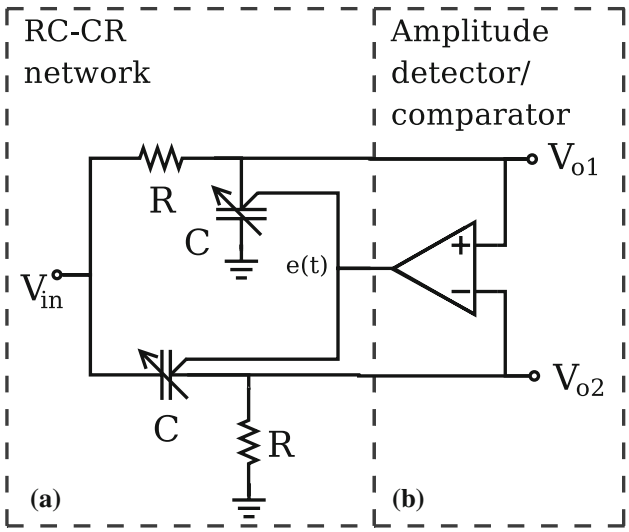


Fig. 3 Block diagram of feedback quadrature generator

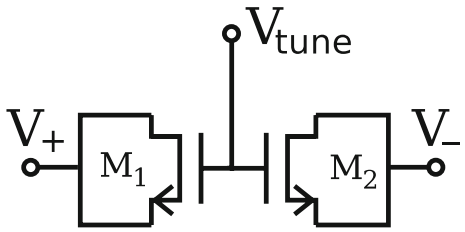


Fig. 4 Schematic of a differential inversion mode varactor

A functional block diagram of the design proposed in this paper is depicted in Fig. 3. By using a varactor to adjust the capacitance to the proper value with respect to the frequency of operation (Fig. 3a) it is possible to significantly expand the bandwidth of the network. The error correction control signal ($e(t)$) used to adjust the varactor's capacitance to the appropriate value is determined with an amplitude detector and comparator circuit (Fig. 3b).

2.1 Varactor

The varactor used in this paper is the basic inversion mode varactor. This device is composed of a transistor with its source and drains tied together. When a gate voltage is applied to the circuit, a depletion region is formed under the gate. The size of this depletion region is dependent on the magnitude of the gate voltage. As this depletion region separates the source and drain from the gate, the larger the depletion region, the smaller the resulting capacitance.

The inversion mode varactor is itself a single ended device. However the capacitor in the CR network (Fig. 1) is required to be differential. In order to produce a differential varactor, two single ended varactors are then placed back to back in series. The schematic for the device is shown in Fig. 4. The control voltage V_{tune} is then used to vary the capacitance.

The device that is used in this paper was laid out and consists of an array of 60 transistors measuring 2 μm × 0.5 μm each. The simulated results of the varactor capacitance and series resistance versus control voltage are shown in Fig. 5. Note that the series resistance is very small and its value changes in an opposite manner to the capacitance with respect to the control voltage.

From Fig. 2, it is seen that for operation between 1.5 and 5 GHz, the required value of the capacitor ranges from 0.55 to 0.2 pF. Comparing this to Fig. 5, it is seen that this lies within the simulated varactor range, meaning that this varactor can be used to cover a wideband.

2.2 Amplitude detector and comparator feedback network

The proposed system is able to determine the amplitude difference between the quadrature outputs and feed the resulting error signal, $e(t)$ back to the varactor network to

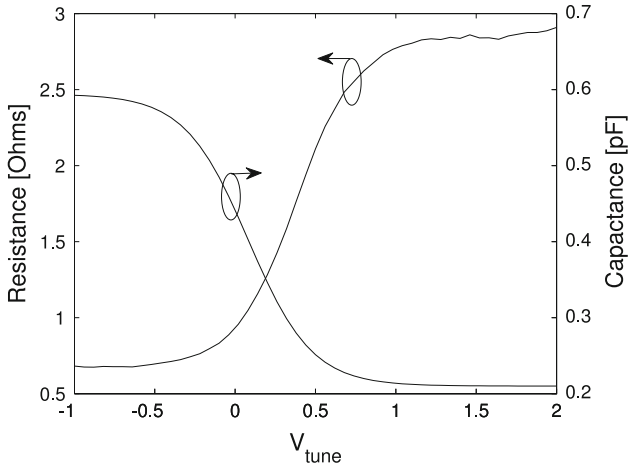


Fig. 5 Simulated results of the varactor

compensate the phases. The comparator circuit is not trivial to design because subtracting two AC voltages (V_{o1} and V_{o2}) that are in quadrature only produces another AC signal with a phase of 45°, which is not very useful. In order to properly compare the amplitudes of the two outputs, the signals need to be aligned. Thus a large portion of the stages for the amplitude detector described in this section is devoted to aligning the two waveforms in preparation for the error signals to be fed into the comparator.

The expanded block diagram depicting all the stages of the amplitude detector and comparator is shown in Fig. 6. The signals that enter the amplitude detector are from the previous RC-CR network in Fig. 3a. These signals (V_{o1} and V_{o2}) are originally 90° apart.

In order to ensure that the next stage does not produce any loading effects onto the previous network, a common source buffer circuit is placed at the beginning of this amplitude detector circuit (Fig. 6i).

The first step to align the signals is that another 90° RC-CR varactor compensated phase shifter is employed to shift the signals a further 90° out of phase (Fig. 6ii). This second RC-CR network also uses the same varactors (to compensate for its own frequency dependent amplitude difference) and $e(t)$ signal from the previous stage. Again, to ensure this RC-CR network is not affected by the next stage, another set of common source amplifier buffers (Fig. 6iii) are placed at the output of this RC-CR network.

The signals are now 180° from each other. These signals are then passed through two circuits that produce 0° and 180° phase shifts (Fig. 6iv). At the outputs of this stage, the signals will now be perfectly aligned.

At this point, if the two different amplitude signals are subtracted from each other, another sinusoid will result. A rectifier circuit (Fig. 6v) will need to be employed to remove the negative half of the signal. Once this has taken place, the signals can now be subtracted from each other. This process is done using a differential amplifier (Fig. 6vi).

A low pass filter (Fig. 6vii) that also functions as the feedback system loop filter is then used to smooth out the resulting wave to produce a DC signal. This DC signal is the varactor's control signal used to adjust the phases of the output signals V_{o1} and V_{o2}.

2.2.1 *Differential pair*

In Fig. 6iv), a circuit is required to produce a 180° phase. A differential pair is one such circuit that can provide both a 0° and 180° phase shift. This is accomplished by exciting each differential pair single endedly at opposite sides as shown in Fig. 7a, b. In this manner both 0° and 180° phase shifts will be created.

Because both differential pairs on each of the branches are the same, they will exhibit the same gain properties across the frequency bandwidth. Other wideband phase shifters can also be used for generating the 180° signal such as a simple inverting amplifier, which can have the added benefit of lower power consumption.

2.2.2 *Rectifier circuit*

Once the signals are aligned, after emerging from the 180° phase shifters in Fig. 6iv, the signal will need to be rectified (Fig. 6v) in preparation for the comparator stage. The

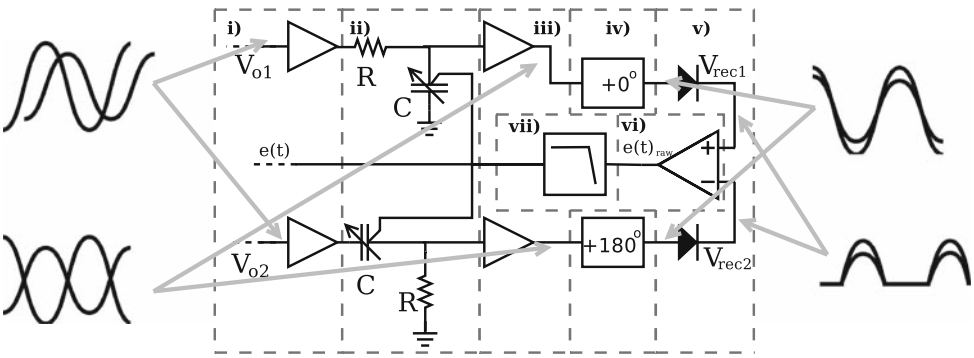
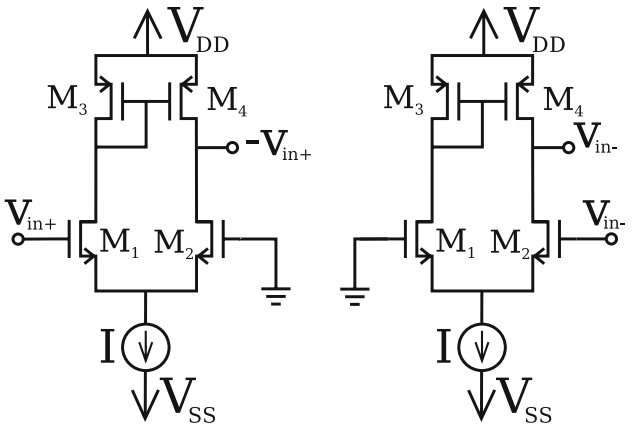


Fig. 6 Expanded block diagram of amplitude detector



(a) 180° phase shifter **(b)** 0° phase shifter

Fig. 7 Differential pairs used to produce 0° and 180°

ideal rectifier is a diode with a 0 V threshold voltage. This is particularly difficult to implement because the cutoff voltage for this technology is 0.7 V which is approximately the same signal levels used in RF circuits.

The use of a modified common source amplifier was employed and is shown in Fig. 8a. By biasing the transistor so that it is on the edge of turning on, when the input is in the negative region, the output will remain at 0 V. But when the input is positive, the transistor turns on, and the signals are passed.

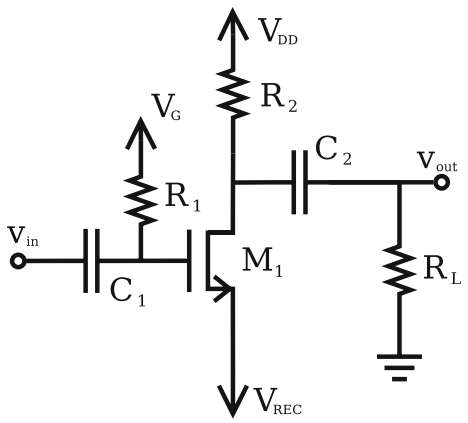
This subcircuit was simulated and the results are shown in Fig. 8b. The dashed line is the original wave and the rectified wave is the solid line.

2.2.3 *Comparator and loop filter*

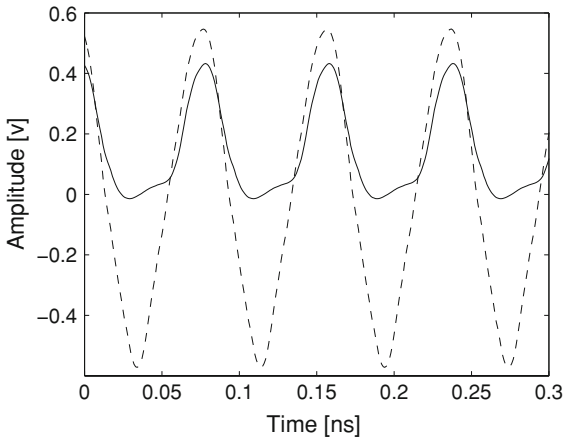
The final stage of the feedback loop is composed of an analog comparator circuit (Fig. 6vi) in which the two aligned and rectified waveforms are subtracted from each other. The output is connected to the varactors through an RC filter and is shown in Fig. 9.

A differential pair is used because it can also function as an analog subtractor. The two rectified signals v_{rec1} and v_{rec2} are then connected to the input of the differential pair and subtracted from each other. Figure 10a, b depicts the signals before and after the comparator.

Note that the output of the comparator is composed of both the RF component as a result of the subtraction and a DC signal. The output of the comparator is directly coupled through the RC low pass filter to the varactor. Figure 10c is the signal after it has passed through the RC low pass filter. The DC component is set so that it will provide the starting operating point for the varactor's capacitance. The additional RF component is then smoothed using a basic RC low pass filter (Fig. 6vii).



(a) Schematic of rectifier circuit



(b) Simulations of before (dashed line) and after (solid line) the rectifier

Fig. 8 Schematic and simulated results of the rectifier circuit

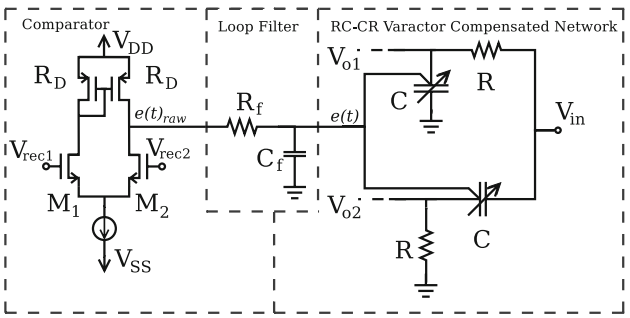
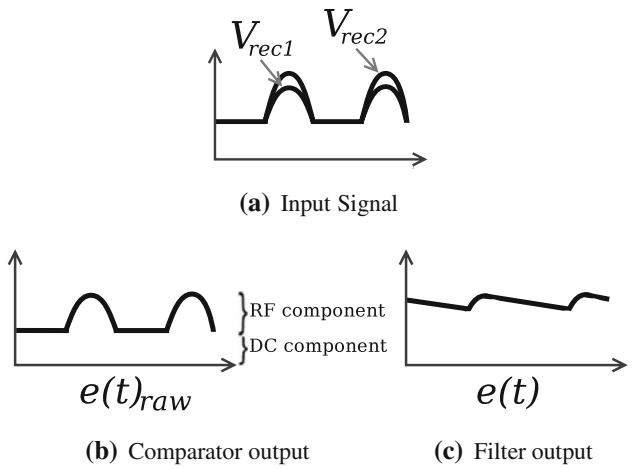


Fig. 9 Final stages of the feedback loop depicting the interface between the comparator and the varactor

The RC low pass filter functions both to smooth out the half sine waveform and also as a loop filter that is used to adjust the settling time of the system. Figure 11 illustrates the combination of DC and RF signals that vary the varactor's input capacitance. In order to ensure the system is inherently stable across the frequencies of interest, and the pole of the loop filter was chosen to be intentionally smaller



(a) Input Signal

(b) Comparator output **(c)** Filter output

Fig. 10 Signals associated with comparator stage

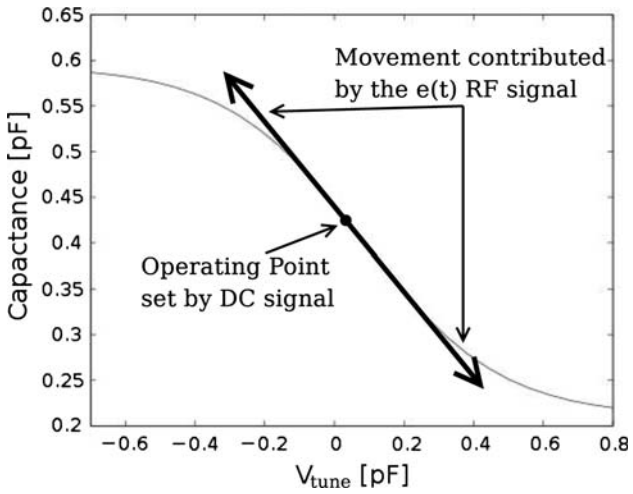


Fig. 11 Movement contributed by both DC and RF signal that change the varactor's capacitance

than required. The trade-off of a larger settling time is acceptable because the frequency is not expected to change often (i.e. only at startup).

3 Simulated results

The entire circuit was laid out using standard 0.18 μm CMOS technology and occupies 0.17 mm^2 without bonding pads and 0.28 mm^2 with bonding pads. The layout of the circuit in Cadence is shown in Fig. 12.

3.1 Simulated time domain results

A typical time domain simulation is shown in Fig. 13. The result of the DC voltage produced from the feedback loop

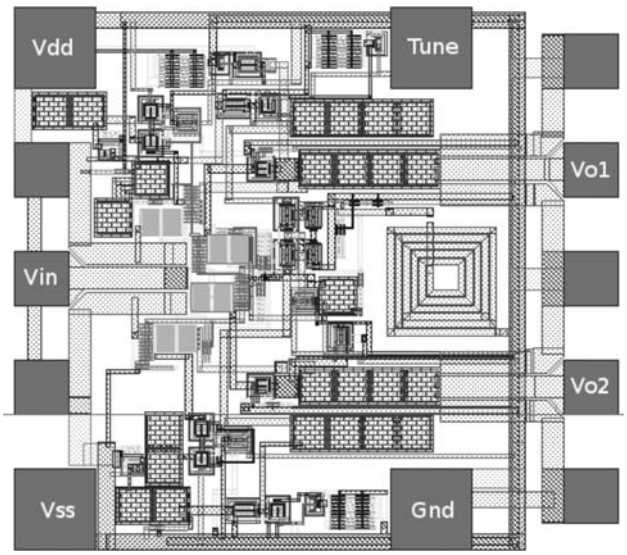


Fig. 12 Layout of feedback quadrature generator

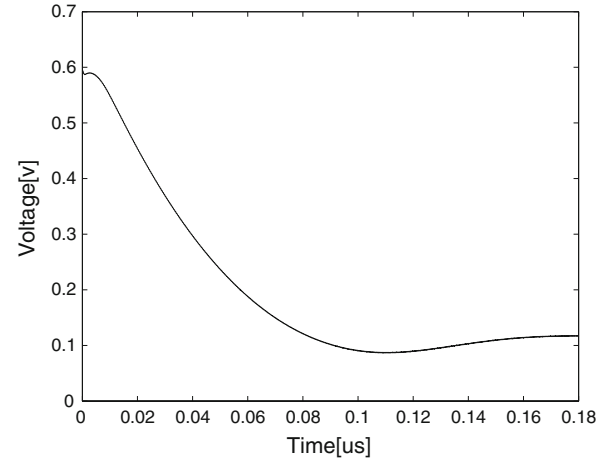
that adjusts the varactor's capacitance is is shown in Fig. 13a.

As the circuit starts up, a typical underdamped response is clearly seen with both the feedback voltage and the resulting changes in the amplitudes of the output signals. After a period of approximately 0.14 μs, the system settles into a steady state producing the final compensated response. A second set of time domain results showing the two quadrature outputs are shown in Fig. 13b. From this figure, it is clear that the amplitude of the output is modified as the feedback loop changes the varactors value. A zoomed in view of the final steady state conditions where both amplitudes have settled and are now equal are shown in Fig. 13c.

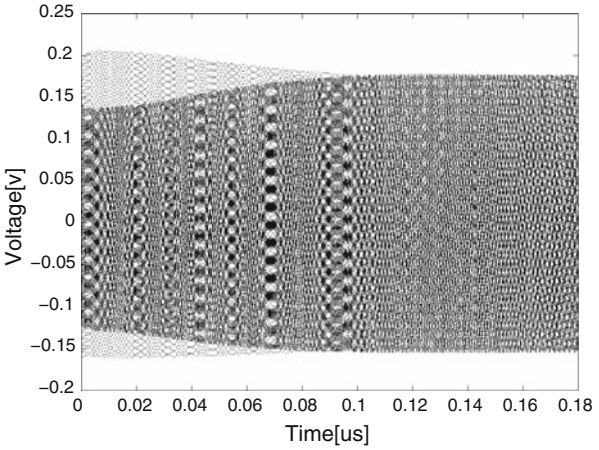
3.2 Swept simulation results

As the system requires a settling time, a time domain simulation was performed at each frequency point and the forward gain was determined for both outputs. The resulting difference with respect to frequency is found in Fig. 14.

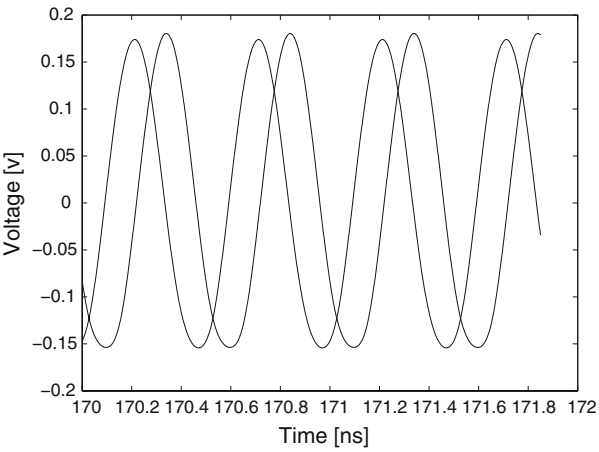
Because there are two signal paths, it is crucial that they both perform the same operation to both signals. Any amount of mismatch can be detrimental to their ability to cancel out the amplitude error in the feedback system. A Monte-Carlo analysis was therefore performed on the circuit to observe the effects of transistor mismatch. The analysis was performed on the entire circuit using the TSMC statistical models. The results of the analysis shows minimal impact of transistor mismatch. The observed 1-sigma standard deviation with 30 trials simulating transistor mismatch at 1 and 6 GHz were found to be 6.8 and 37 μV respectively.



(a) DC feedback path that for the varactor



(b) Resulting amplitude adjustment at the output of the system



(c) Zoomed in view of the steady state

Fig. 13 Simulated time domain results at 2 GHz depicting the feedback settling time of the quadrature generator

The measured difference between the two output signals are shown in Fig. 14. The system produces quadrature outputs over the range of 1–6 GHz with a phase error of 5° or less. The amplitude error remains within ±2 dB over the same frequency span. The overall insertion loss for both outputs is 9.5 dB.

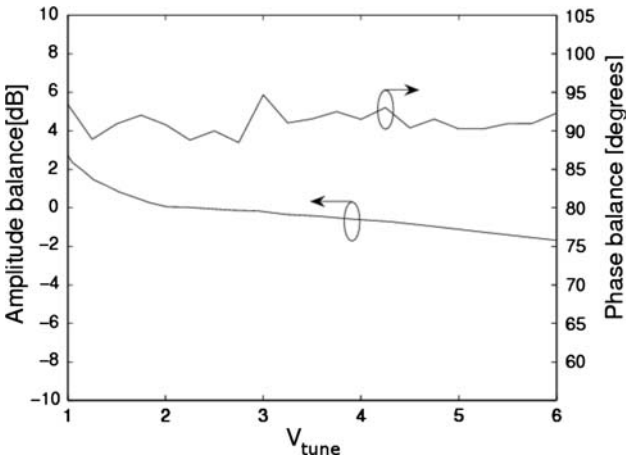


Fig. 14 Measured amplitude balance

The entire chip used about 84 mW of dc power. While this level of power consumption can appear to be on the high end, the power draw must be seen in the context of the performance of the chip. This circuit can generate quadrature outputs over a 5 GHz span from 1 to 6 GHz, which is works out to a fractional bandwidth of 140%, and this would be very difficult to achieve with a single LC-tuned quadrature VCO. Yet, there are ways to reduce the dc power dissipation. One approach would be to reduce the peak-to-peak voltage of the RF input signal, which would allow one to bring down the required voltage headroom in the buffers used in the chip, thus leading to lower bias current levels and ultimately lower power consumption.

4 Conclusions

In this paper a quadrature wideband generator compensated through a feedback network is presented. The basic RC-CR network used in many circuits lack the ability to function over a large frequency range. This new circuit demonstrates the ability to compensate for an amplitude imbalance through the use of a novel amplitude detector to determine and compare the amplitudes of the two branches. The amount of compensation is then fed back into the control voltages of the varactors and the result is that this circuit now has the ability to significantly extend the bandwidth of the original RC-CR network. The experimental results show a device that can maintain quadrature signals with a phase imbalance of $<5°$ from 1 to 6 GHz and with an amplitude balance of ±2 dB over the same range.

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Carlos E. Saavedra (S'92–M'98–SM'05) received his Ph.D. degree in Electrical Engineering from Cornell University, Ithaca, NY, in 1998. From 1998 to 2000 he was with Millitech Corporation, South Deerfield, MA, where he designed millimeter-wave transmitter and receiver circuits for 31 GHz local-to-multipoint distribution systems and 38 GHz point-to-point radio systems. Since August 2000, he has been with the Department of Electrical and Computer Engineering at Queen's University, Kingston, Ontario, Canada, where he is now Associate Professor. His research activities are in the field of microwave integrated circuits and systems, including frequency multipliers, mixers, operational transconductance amplifiers, filters, and phase-locked loops. His teaching interests are in the area of electronic circuits for communications applications. Dr. Saavedra is a reviewer for several international journal publications including the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, Electronics Letters, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. He has also been in the technical programming committee of several past international conferences. In the year 2001 he was awarded the Excellence in Teaching Award at Queen's University by the Electrical Engineering Class of 2002. He is a member of Eta Kappa Nu and Tau Beta Pi, and he is a registered Professional Engineer (P. Eng.) in the province of Ontario, Canada.