A FULLY INTEGRATED S-BAND VECTOR PHASE SHIFTER IN CMOS TECHNOLOGY

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ABSTRACT

In this paper a 90° variable phase shifter operating at 2.3 GHz is presented. This circuit uses a combination of variable gain amplifiers and an analog summation circuit to to control the magnitude of each vector and sum them together. Experimental results show a 93.7° variable phase shift range while maintaining a 0.08 dB amplitude error. The insertion loss is -4 dB and the input and output reflection are -22.6 dB and -10 dB. The device measures 0.20 mm^2 without bonding pads.

1. INTRODUCTION

An important technique for implementing a variable phase shifter is the vector summation method [1] [2] [3] [4] [5]. In this approach, quadrature (orthogonal) vectors are added together and depending on the magnitude of these constituent vectors then different phase angles can be produced in the resulting output vector.

If space is not a concern such as in hybrid microwave circuits using packaged devices and microstrip transmission lines, then the quadrature vector generation circuit and the summation circuit can be easily implemented with passive power splitters and combiners such as branchline couplers. However, these passive structures are not economical nor practical in MMIC implementations, specially at the lower end of the microwave frequency range (1.0 GHz to 5.0 GHz) precisely because the wavelengths are very large in relation to typical die sizes. The common solution to this problem has been to replace passive couplers with their LC equivalents in MMIC's to save space, yet the risk is that fabrication tolerances on the inductors will significantly shift the center frequency of the coupler and hence of the phase shifter itself.

In this paper, an ultra-compact MMIC phase shifter using the vector summation approach is presented. Its key innovation is in its vector addition mechanism. At microwave frequencies it is not simple to design an accurate voltage summation circuit as it is at baseband with the aid of operational amplifiers. Our approach has been to use three differential pairs to ultimately implement a summation operation as depicted in Fig. 1. The advantage of this method is that it only requires 6 identical transistors, leading to very accurate vector addition and a high degree of immunity to process variations.

2. CIRCUIT DESCRIPTION

The block diagram for the circuit is found in Fig 1. Following a similar layout of previous vector sum phase shifters, the circuit consists of four parts. The first section is a quadrature generator that produces the required two vectors. This is then followed by two variable gain amplifiers (VGA) which are able to control the magnitude of each vector. An analog summation circuit in the next stage is then used to sum the components together. Finally a buffer circuit is used to drive the 50Ω load at the output.

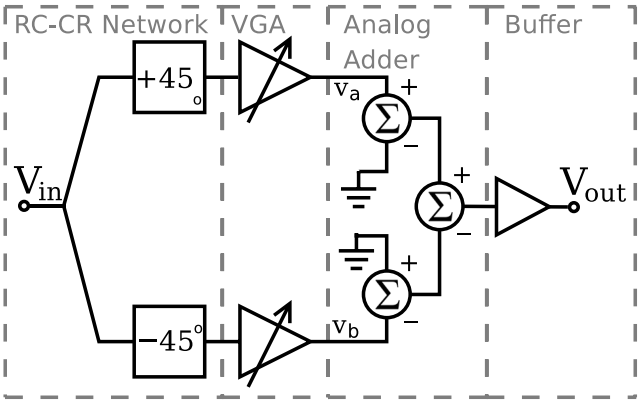

Fig. 1. Block diagram for vector phase shifter

As mentioned previously, since the use of microstrip type structures would be prohibitively large at this frequency, the use of active elements is used instead. For the quadrature generator, instead of a branch line hybrid coupler, the use of an RC-CR type circuit is used. The Wilkinson divider is replaced with an analog summation circuit based on a set of differential amplifiers.

2.1. Quadrature generator

In order to generate the two vectors, the use of a quadrature generator in the form of an RC-CR network is employed and is shown in Fig 2a). This quadrature generator produces two vectors over a wide bandwidth at $+45°$ and $-45°$(Fig 2b)). The magnitude of each vector, however, is frequency dependent and they are equal only when $\omega = 1/RC$. In the case of this circuit, the frequency of operation has been set to 2.3 GHz.

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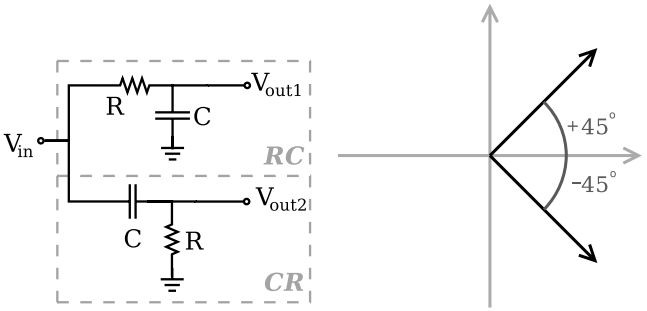
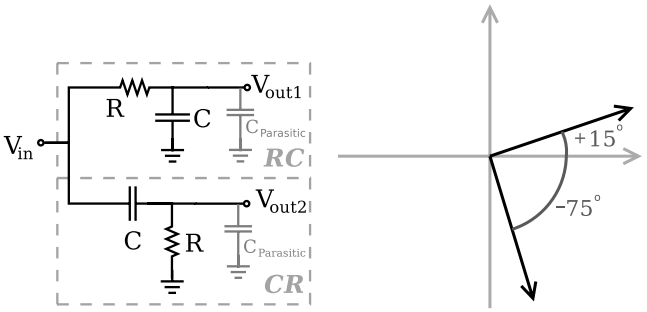


(a) Ideal RC-CR network (b) Resulting vectors



(c) Loaded RC-CR network (d) Resulting vectors

Fig. 2. Quadrature generator networks and associated vectors

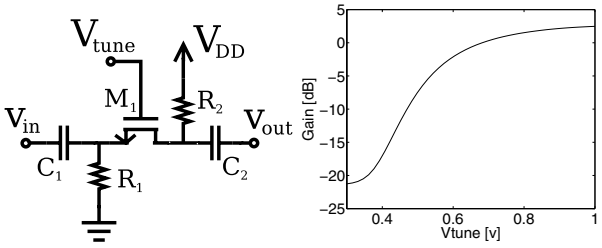
As the outputs of this quadrature generator are connected to a set of VGAs, there are certain loading effects that occur. These loading effects can be approximated with a parasitic capacitance to ground in the form of $C_{parasitic}$. This extra capacitance is reflected in schematic found in Fig 2c). Because of the loading capacitance, this affects the phase of the resulting vectors. The resulting circuit with the parasitics factored in can generatre vectors with phases of $+15°$ and $-75°$ as shown in Fig 2d). Note that regardless of what type of loading is placed at the outputs, the circuit is still able to maintain exact quadrature seperation.

2.2. Variable Gain Amplifer

The variable gain amplifier found in this circuit is of the common gate type and the schematic is found in Fig 3a). The gate of the amplifier is varied to produce the varying gain. The common gate architecture was chosen because the excess phase shift through thus VGA is minmal as the gain of the amlifier varies. The open circuit gain with respect to the gate voltage is found in Fig 3b). The use of open circuit gain was used to reflect the high impedance nature of the next stage. The gain is able to be varied from 2.2 to -21 dB, thus allowing the magnitude of the vectors to be controlled over a wide range.

2.3. Analog Summation Circuit

The creation of a direct analog summation posses some difficulty as no single circuit posess the ability to directly produce



(a) (b) Open circuit gain

Fig. 3. Simulated results for the variable gain amplifier

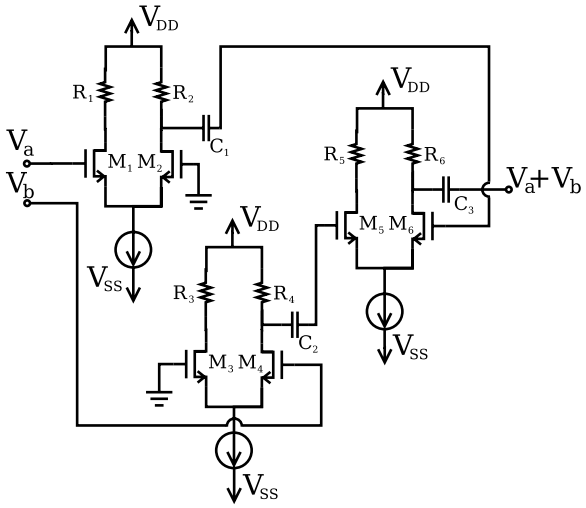


Fig. 4. Analog summation circuit

an adder [6] [7]. The implementation of analog subtractors however, are readily avaliable. Therefore in this paper, a set of analog subtractors are cascaded together to produce an equivalent summation circuit (i.e. $v_a - (-v_b) = v_a + v_b$). The basic schematic of the analog summer is found in Fig 4.

Three differential pairs form the equivalent analog subtractors. Although it is possible to construct this same circuit using only two differential pairs, the extra differential pair was used in order to keep the circuit balanced and symmetrical. The common use of active loading in the form of current mirrors instead of resistors was not used as these are known to produce extra phase shifts due to parasitic capacitance loading.

2.4. Final Circuit

The final circuit's schematic is found in Fig 5. The use of a simple matching network was used to improve the input reflection. In addition, a buffer circuit consisting of a common drain type amplifier was used to help drive the low impedance load at the output.

An S-parameter simulation was performed in SpectreRF to determine the forward gain. Each VGA was turned on one at a time. In each instance, the gate tuning voltage was

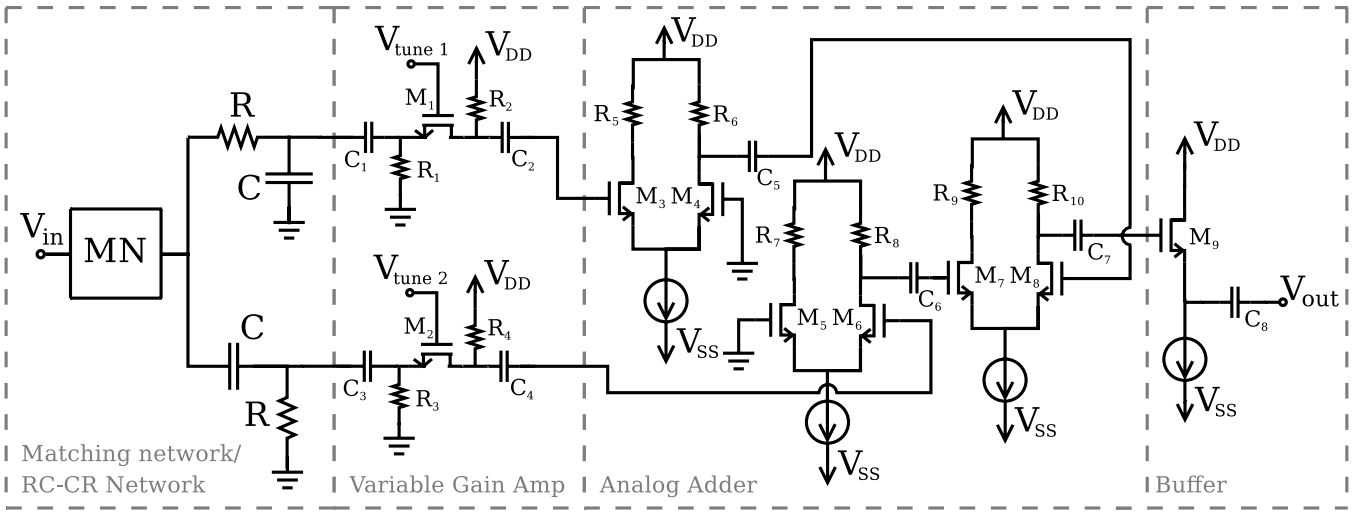


Fig. 5. Schematic of complete circuit

changed to produce the varying gain at the output. Fig 6 shows the results of two seperate simulations for both VGAs and their resulting vectors at the output of the circuit.

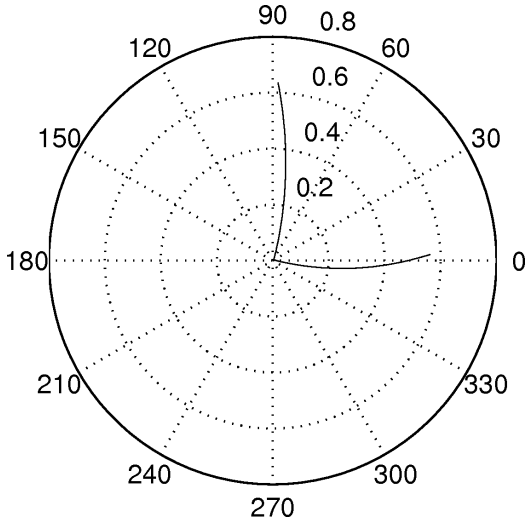


Fig. 6. Simulated vectors produced by each amplifier at the output of the circuit

The phase of each of these vectors are very different from the original $+45^\circ$ and -45° produced at the quadrature generator. This is a result of added phase through each part of the circuit. From simulation, the addition of the VGA skewed the original vectors at the outputs of the quadrature generator by -30°. At the output of the VGAs, the amplifiers are found to shift the phase by a constant $+25^\circ$. After the combination of the analog summer and the common drain buffer, the phase is further shifted by another $+50^\circ$. Thus the total phase shift throughout the circuit is $+45^\circ$, which moves the original $+45^\circ$ and -45° vectors to 0° and 90°.

3. MEASURED RESULTS

The device was manufactured using CMOS 0.18 μm technology and a micro-photograph of the device is shown in Fig 7. The core circuit measures 0.20 mm^2 and 0.42 mm^2 including the bonding pads. On-wafer probing using CPW probes in combination with a VNA was used to measure the S-parameters. The input and output reflection was measured to be -22.6 dB and -10 dB.

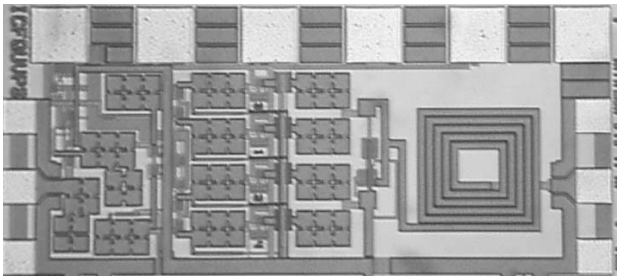


Fig. 7. Micro-photograph of vector phase shifter

The variable gain amplifier's tuning voltages were controlled separately to adjust the vectors. The combination of both vectors were used to produce the varying phase while maintaining a constant output power. A polar plot of the forward gain was then produced using the results of the forward gain measurements are are shown in Fig 8. The phase shift is found to vary from -6.6° to 87.1°, producing a total of 93.7° phase shift.

A plot depicting the insertion loss is found in Fig 9. From this figure, it is clear that the resulting magnitude can be kept to within a very low error. In the case of this circuit, the amplitude error does not increase more than 0.08 dB. In commercial production, tuning of the control voltages will be supplemented with a combination of a DAC and a microprocessor that will produce the corresponding control voltages for the

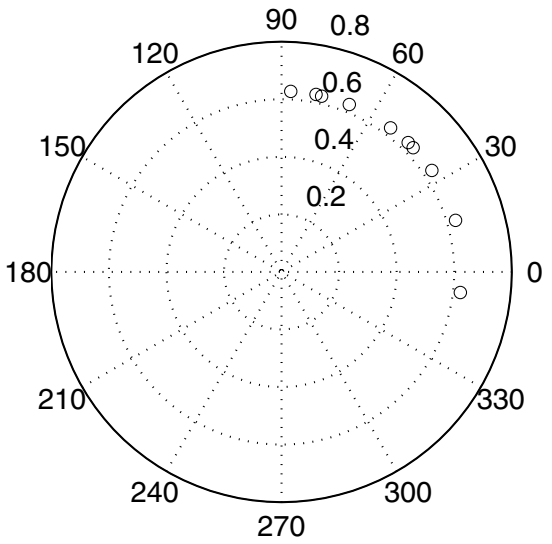


Fig. 8. Polar plot of measured results

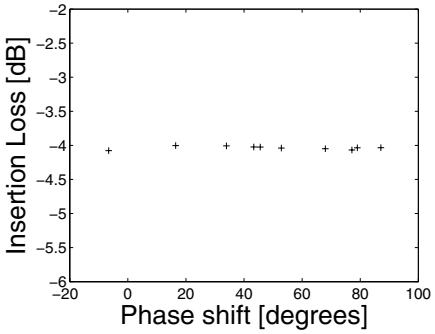


Fig. 9. Insertion loss versus phase

required phase.

The circuit power handling was determined using a signal generator and corresponding spectrum analyzer. The input referred 1 dB compression point was determined to be 1.5 dBm.

4. CONCLUSIONS

A variable phase shifter operating at 2.3 GHz is presented in this paper. By using active devices instead of passive microstrips, this circuit is able to achieve complete compact MMIC integration. A quadrature generator followed by two variable gain amplifers are used to produce and control the two vectors. The use of an analog summer is then used to sum the signals together. The device was then manufactured in CMOS 0.18 um technology. The experimental results show a full 93.7° phase shift. Because the control voltages were manually controlled, a very low amplitude error of 0.08 dB was found. The power consumption was found to be 88.2 mW. The insertion loss was determined to be -4 dB and the input and output reflection are found to be -22.6 dB and -10 dB.

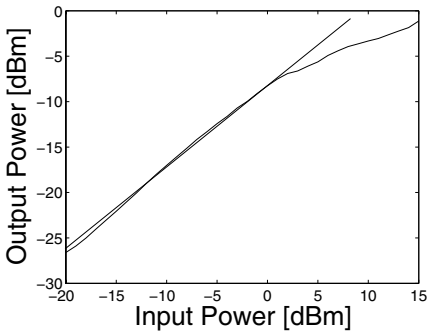


Fig. 10. Measured 1 dB compression point

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