A Divide-by-Three Regenerative Frequency Divider Using a Subharmonic Mixer

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***Abstract*—A regenerative frequency divider topology is used with a $\times 2$ subharmonic mixer to realize a divide-by-three frequency divider. The circuit accepts input signals in the range of 5.2 GHz to 5.5 GHz and produces signals from 1.73 GHz to 1.83 GHz. Measured results show a maximum conversion gain of 0 dB and at least a 30 dB suppression of all undesired harmonic components at the output. The circuit core consumes 44 mW of dc power and ideas are provided on how to reduce the power draw. The chip was fabricated on a standard 0.13-μm CMOS process and it occupies an area of 1.0 mm^2 including bonding pads.**

***Index Terms*—CMOS analog integrated circuits, divide-by-3, frequency divider, monolithic microwave integrated circuit (MMIC), regenerative divider.**

I. Introduction

A classic analog frequency divider configuration is the regenerative system shown in Figure 1 [1]. In its simplest form, the regenerative divider consists of a mixer and a low-pass filter. If the input signal to this circuit has a frequency f_{in} then there are two steady-state outputs of the mixer, $\frac{1}{2}f_{in}$ and $\frac{3}{2}f_{in}$. The low-pass filter attenuates the $\frac{3}{2}f_{in}$ signal thus leaving the $\frac{1}{2}f_{in}$ for the output and for feedback. In practical implementations of the regenerative frequency divider technique an amplifier may also be required after the filter to provide the necessary gain around the feedback loop to continuously regenerate the output signal.

To increase the division ratio of the circuit under discussion, a frequency multiplier can be inserted in the feedback path. Alternatively, the fundamental mixer in Fig. 1 can be replaced with a subharmonic mixer [2], [3]. For the latter approach to work the feedback signal must be connected to the $\times n$ multiplication port of the subharmonic mixer.

While many designs for even-order $(1/2^n)$ frequency dividers exist there are comparatively fewer designs for odd-order divider circuits. In recent times, however, there has been renewed interest in circuits with odd-order division ratios [4]–[7].

A regnerative divide-by-three frequency divider is described in this paper that relies on a subharmonic mixer. An additional innovative aspect of this design is the use of a tuned amplifier stage to provide gain in the feedback path to facilitate the regeneration process that also filters out the undesired tone generated by the mixer. To demonstrate the concept, a chip was designed and fabricated using a standard 0.13-μm CMOS process and test results are reported.

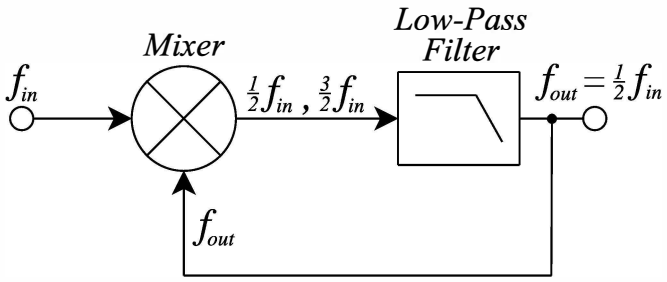

Fig. 1. Block diagram of a regenerative frequency divider.

II. Circuit Description

The concept of the proposed divide-by-three frequency divider is based on Miller's regenerative topology. In a typical regenerative frequency divider, a fundamental mixer, a low-pass filter and an amplifier (as needed) are used to produce a divide-by-two operation. To obtain odd-order division using the regenerative approach, a frequency multiplier is used in the feedback path of the circuit before the mixer, which is the approach taken in [4], [5]. In this paper a different approach is taken which simplifies the circuit and leads to savings in chip area. In our design solution we incorporate the multiplier circuit into the mixer by using a subharmonic mixer [8], [9].

Shown in Figure 2 is the block diagram of the divide-by-three circuit proposed in this work. The most significant change of this circuit compared to the traditional regenerative divider shown in Figure 1 is the use of a $2\times$ subharmonic mixer in place of the fundamental mixer. If the two inputs to the subharmonic mixer are f_{in} and f_{out}, as shown in Figure 2 then at the output of the mixer are two frequencies, $f_{in}+2f_{out}$ and $f_{in} - 2f_{out}$. The downconverted term is amplified by the tuned amplifier while the upconverted term is attentuated, leaving (ideally) only the downconverted component at the output. Therefore, $f_{in}-2f_{out} = f_{out}$, which shows the desired output, $f_{out} = \frac{1}{3}f_{in}$.

As mentioned above, the low-pass filter in Figure 1 has been changed to an amplifier that is tuned to the $\frac{1}{3}f_{in}$ frequency to ensure that the $\frac{5}{3}f_{in}$ frequency has significantly lower power

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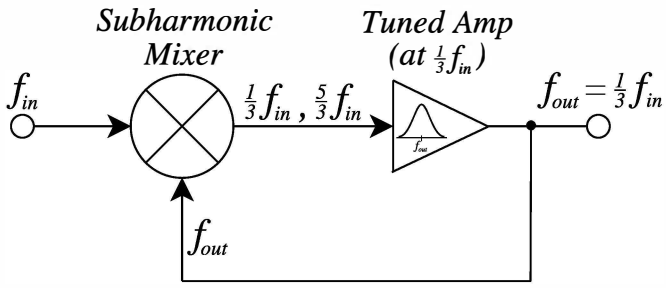

Fig. 2. Block diagram of the proposed divide-by-three frequency divider.

at the output (and in the feedback path to the subharmonic mixer). The use of this amplifier can improve the output power at $\frac{1}{3}f_{in}$, but also ensures that there is sufficient gain around the loop to ensure start-up of the circuit.

The divide-by-three circuit is based on a single-balanced version of the $2\times$ double-balanced subharmonic mixer described in [9], as shown in Figure 3. This circuit, which is essentially half of the $2\times$ subharmonic mixer discussed in [9], requires only a differential LO input as opposed to the quadrature LO input required for the double-balanced subharmonic mixer. In this application, the differential outputs of the tuned amplifier are connected to the LO input transistors, M1 & M2 (see Figure 2). Transistors M1 & M2 produce the doubled frequency, which is then mixed with the RF input to produce an output at the drains of the RF transistors with frequency $f_{RF} \pm 2f_{LO}$.

To implement the tuned amplifier shown in Figure 2, a differential pair was used with an LC load. The output of the subharmonic mixer will be used as input to the differential amplifier and the output of the tuned amplifier will be fed to the gates of the LO transistors shown in Figure 3.

The schematic for the entire circuit is shown in Figure 4 (biasing not shown). It consists of the single-balanced subharmonic mixer shown in Figure 3 with the differential input signal (v_{IN0} and v_{IN180}) applied to the gates of M3 & M4 along with the tuned amplifier (M5 & M6) and output buffers to drive the 50 Ω load from either the measurement equipment or the input impedance of the next stage in the circuit. An inductor is used above the LO transistors in order to increase the conversion gain of the subharmonic mixer [10]. DC blocking capacitors are used between the mixer output and the amplifier input and also between the output of the amplifier and the LO transistors in order for optimal bias points to be used. The bias point for the LO frequency doubling transistors is somewhat sensitive and simulations showed that the optimal point is at $V_{SS} + V_t$ where V_{SS} is the negative supply voltage and V_t is the FET threshold voltage. Assuming ideal FETs that do not conduct any current when the gate-source voltage is less than threshold voltage the selection of this bias voltage will produce an absolute value signal that clearly has most of its power at twice the frequency of the signal applied to the gates of M1 & M2. The current source shown for the tuned differential amplifier is implemented using a standard current

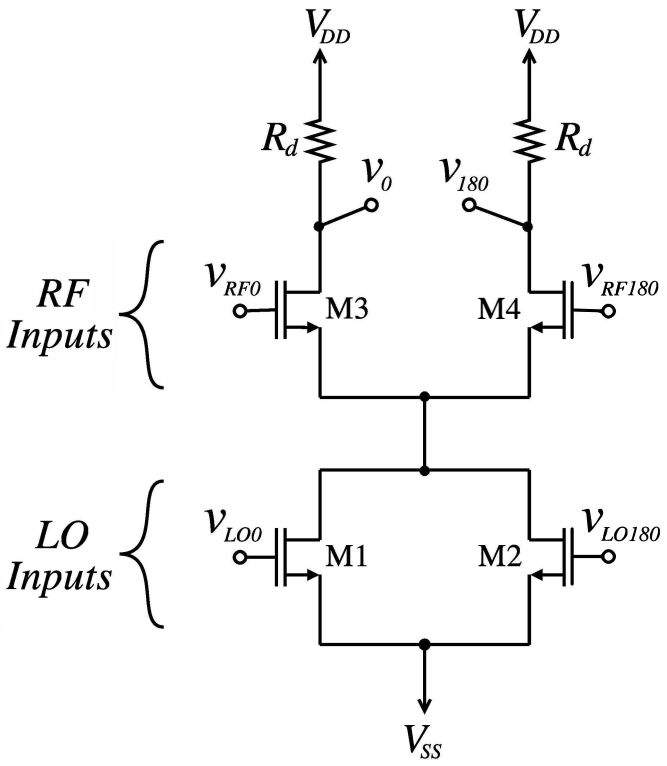

Fig. 3. Single-balanced $2\times$ subharmonic mixer circuit.

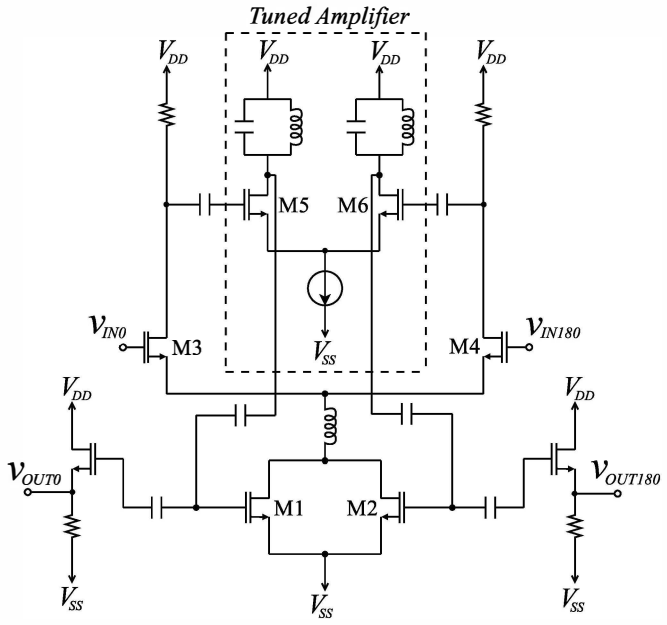

Fig. 4. Simplified schematic of the proposed frequency divider (biasing not shown).

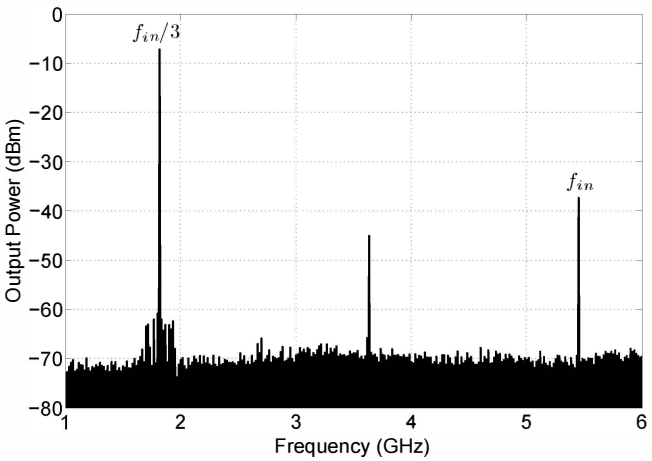

Fig. 5. Measured frequency divider output spectrum with a -7 dBm input at 5.4 GHz.

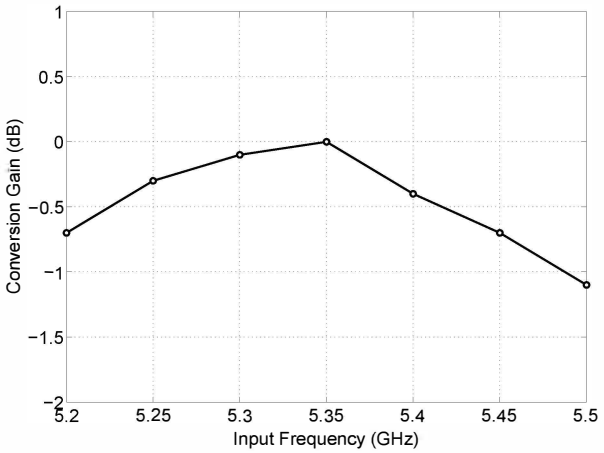

Fig. 6. Measured frequency divider conversion gain for various input frequencies (-7 dBm input power).

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III. Experimental Results

To evaluate the performance of the proposed divide-by-3 frequency divider, measurements were performed using a probe station with differential coplanar waveguide probes. The supply voltages were set to 1.5 V and -0.8 V for V_{DD} and V_{SS}, respectively, and differential input and output signals were used, as shown in Figure 4. With an input power of -7 dBm at 5.4 GHz, the output spectrum is shown in Figure 5. The output spectral component at 1.8 GHz ($\frac{1}{3}f_{in}$) is clearly the strongest at approximately -7 dBm, which is a conversion gain of approximately 0 dB. The fundamental signal power at the output is -37 dBm and therefore the fundamental suppression is 30 dB. All other harmonics at the output are suppressed by at least 35 dB.

To evaluate the performance of the circuit with various input frequencies, a constant input power of -7 dBm was used and the output spectrum was observed. As discussed previously, the bandwidth of the circuit is limited by the LC tank shown in Figure 4 and outside this input frequency range no output at the divide-by-three frequency will be obtained. The measured bandwidth for a -7 dBm input power is shown in Figure 6. With an input power of -7 dBm the circuit operates from 5.2 GHz to 5.5 GHz with varying levels of output power at the desired divide-by-3 spectral component. The conversion gain of the divide-by-three frequency divider has a minimum of -1.1 dB at 5.5 GHz and a maximum of 0 dB at a 5.35 GHz input frequency. This increased output power can be attributed to the peak tank Q-factor at 5.35 GHz. Since this is a regenerative topology, the output power at the divide-by-3 frequency is relatively constant and does not increase proportionally to the input signal power.

The initial power of the $\frac{1}{3}f_{in}$ signal at the output of the subharmonic mixer is a function of both the power of the input signal as well as the power of the feedback signal at

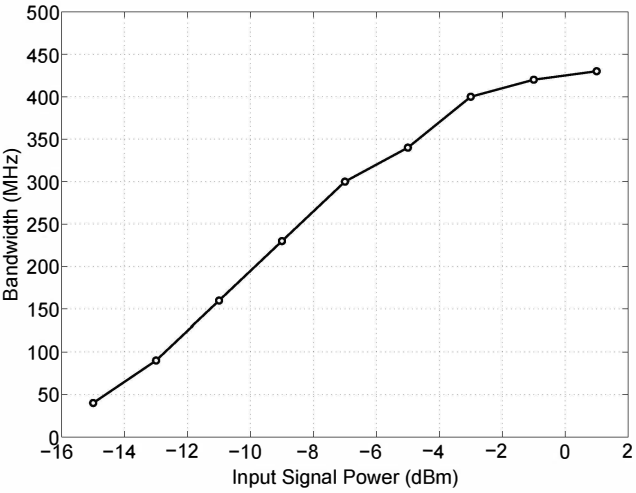

Fig. 7. Measured frequency divider bandwidth for various input power levels.

the other subharmonic mixer input port. Since regenerative dividers require that the gain around the loop be greater than unity, it follows that the circuit will cease operation at some point as the input power is decreased. Similarly, the bandwidth of the divider will increase as the input power increases since the $\frac{1}{3}f_{in}$ signal at the subharmonic mixer output will be stronger and will compensate for the lower amplifier gain away from the centre frequency of the amplifier. Figure 7 shows the bandwidth attainable for various input power levels. In order for this circuit to operate, the minimum input power level is -15 dBm and a maximum bandwidth of 430 MHz can be obtained for an input power of 1 dBm.

The phase noise of the input signal at 5.4 GHz was measured as well as the output signal at 1.8 GHz. From theory, it would be expected that the divide-by-3 output signal would have a $20log(n)$ phase noise improvement, where $n = 3$ (a phase noise improvement of approximately 9.54 dB). At a

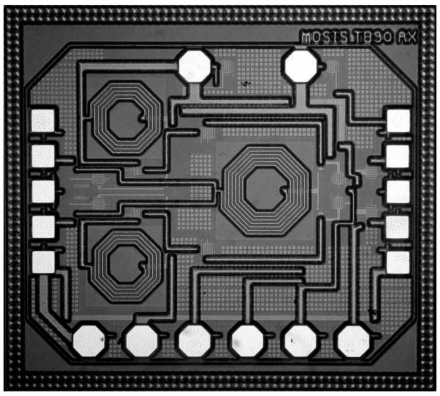

Fig. 8. Frequency divider chip photograph.

100 kHz offset, the input signal phase noise at 5.4 GHz is -112.6 dBc/Hz and at the 1.8 GHz frequency divider output the phase noise is -122.1 dBc/Hz. The difference between input and output phase noise is 9.5 dB, which is very close to the theoretical value.

The dimensions of this integrated circuit are 1000 μm $\times$ 1000 μm (1.0 mm^2) including bonding pads and a photograph of the chip is shown in Figure 8. The power consumption for the divider core circuit is 44 mW and for the entire circuit including the output buffers it is 55 mW. The dc power draw can be reduced by using a passive subharmonic mixer instead of the active one used here. Since the passive mixer will have conversion loss then it would be necessary to boost the gain of the tuned amplifier circuit to compensate of the absense of the conversion gain provided by the active mixer.

IV. Conclusion

An analog frequency divider was presented in this paper that can divide the frequency of an input signal by a factor of three as opposed to the much more common even-order division ratios. The proposed circuit uses a subharmonic mixer instead of a fundamental mixer in a regenerative divider topology along with a tuned amplifier in CMOS 0.13 μm technology. The circuit achieved a maximum conversion gain of 0 dB and a bandwidth of up to 430 MHz. All harmonic components at the output were more than 30 dB below the desired output signal.

V. Acknowledgments

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