CMOS Subharmonic Downconverter using an LNTA Front-End

Fan Jiang[1] and Carlos E. Saavedra[2]

[1]Formerly with Queen's University, now with Ericsson Canada Inc., Ottawa, Ontario, Canada
[2] Dept. of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada

***Abstract*—To mitigate the higher noise figure (NF) of CMOS-based subharmonic mixers (SHMs) relative to their diode-based counterparts, this paper proposes the use of a low-noise transconductance amplifier (LNTA) ahead of the mixing core. The LNTA has a noise-cancelling topology that enables the mixer to have a high conversion gain and low NF over the RF input band of 4.5 GHz to 8.5 GHz. A chip was fabricated on a standard 130 nm CMOS process to validate the concept and measurement results reveal that the mixer can yield a conversion gain of 14.5±1.5 dB and a double-sideband noise figure of 9.25±1.25 dB over the RF band. The mixer's IP_{1dB} is -10.8 dBm and its IIP_3 is -3.7 dBm while its OP_{1dB} is +6.5 dBm and its OIP_3 is +13.8 dBm. The circuit core occupies an area of 0.49 mm^2 on the silicon die.**

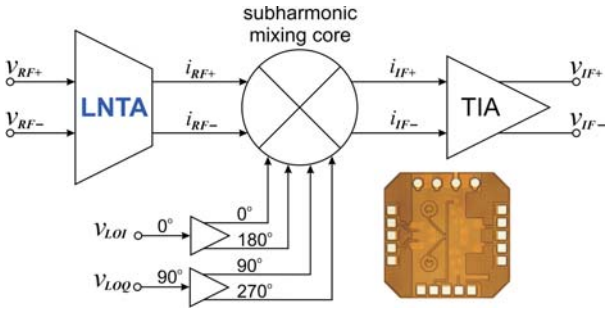

Fig. 1. The block diagram of the proposed SHM using an LNTA at the RF input port. A microphotograph of the fabricated chip is also shown.

I. Introduction

While SHMs have been used for decades by the radio astronomy instrumentation community for millimeter-wave and submillimeter-wave receivers [1], [2], it is relatively recently that the benefits of SHMs have started to employed in silicon-based RFICs. To fill the gap in the availability of CMOS-based SHMs for telecom applications, a number of new SHM designs have been reported in the literature over the past decade in both passive [3]–[5] and active versions [6]–[9].

In a SHM the LO signal is internally multiplied inside the circuit by a factor of 2 or multiples thereof. From this, a couple of important benefits follow: first, SHMs allow designers to reduce the LO frequency by half, or a corresponding fraction, which eases the implementation of the LO circuit itself. Second, when used for direct downconversion, SHMs significantly reduce the dc offset at the IF output port caused by LO self-mixing. These benefits of using an SHM, however, come at the cost of a lower conversion gain and a higher NF relative to a fundamental-mode mixer.

This paper presents a concept to reduce the NF and improve the conversion gain of SHMs by placing a wideband LNTA at the RF front-end. Experimental test results on the fabricated chip taken at an IF of 140 MHz show that the SHM has a conversion gain of 14.5±1.5 dB and a double-sideband noise figure (DSB NF) of 9.25±1.25 dB for RF input frequencies ranging from 4.5−8.5 GHz. The NF performance of the mixer presented in this paper surpasses by more than 3 dB the NF performance of the mixer in [10] which also uses an RF transcondcutance amplifier with a cross-coupled topology.

II. RFIC Design

The block diagram of the proposed passive ×2 SHM is shown in Fig. 1. The LNTA converts the differential RF input signal into a differential current which is then fed to the mixing core. The mixer requires four orthognal LO signals which are produced by passing a quadrature LO signal through a pair of active baluns. At the IF output a differential TIA is used to convert the differential output current back into a differential voltage.

Fig. 2a contains the schematic diagram of the differential LNTA where R_s is the source resistance and R_L is the equivalent load impedance seeing into nodes Y and Z, including the impedance of the active load and the input impedance of the next stage (passive mixing core). Fig. 2b shows the thermal noise sources that are the dominant contributors to the amplifier's noise factor. The CG transistors M_1 and M_3 help to provide a wideband input match to the amplifier since the impedance looking into their sources is approximately $1/g_m$. The CS transistors M_2 and M_4 are cross-connected to give a higher transconductance as well as to cancel the noise of the CG transistors. For a perfectly balanced amplifier devoid of parasitics $g_{m1} = g_{m3} = g_{m,CG}$ and $g_{m2} = g_{m4} = g_{m,CS}$, its

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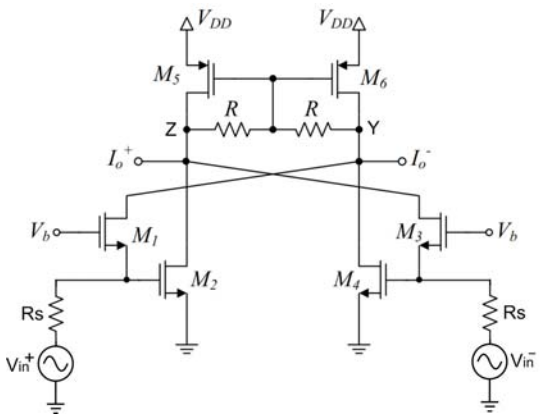
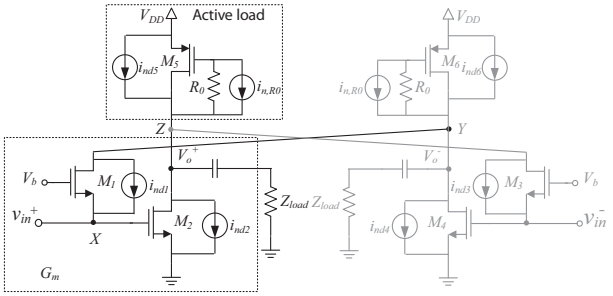


(a)



(b)

Fig. 2. The differential LNTA: (a) schematic diagram, without dc biasing and (b) noise circuit model.

overall transconductance is on the order of $g_{m,CG} + g_{m,CS}$.

Noise cancellation in this amplifier occurs as follows: the noise current i_{nd1} from device M_1 produces a noise voltage $v_{nx} = R_s i_{nd1}$ at node X due to the source resistance and a noise voltage $v_{ny} = -R_L i_{nd1}$ at node Y due to the load resistance R_L. At node Z the noise voltage is $v_{nz} = -g_{m2} R_L v_{nx}$. The noise voltage at the differential output port is

$$v_{nz} - v_{ny} = i_{n1}(1 - g_{m2} R_s) R_L \tag{1}$$

which leads to the simple condition that g_{m2} should be set to $1/R_s$ for maximum noise cancellation. Following an analysis approach similar to that of [11], the noise factor of the LNTA is found to be

$$\begin{aligned} F &= 1 + \frac{\overline{|i_{n1}|^2}(g_{m2} R_s - 1)^2}{4kT R_s^{-1}(R_s \parallel Z_{in,eff})^2 G_{m,eff}^2} \\ &\quad + \frac{r_n g_{m2} + r_p g_{m5} + R_0^{-1}}{R_s^{-1}(R_s \parallel Z_{in,eff})^2 G_{m,eff}^2}. \end{aligned} \tag{2}$$

where

$$Z_{in,eff} \approx \frac{r_{o1} + R_L}{1 + (g_{m1} + g_{mb1}) r_{o1}} \tag{3}$$

$$G_{m,eff} \approx \frac{1 + (g_{m1} + g_{mb1}) r_{o1}}{r_{o1} + R_L} + \frac{g_{m2} r_{o2}}{r_{o2} + R_L}, \tag{4}$$

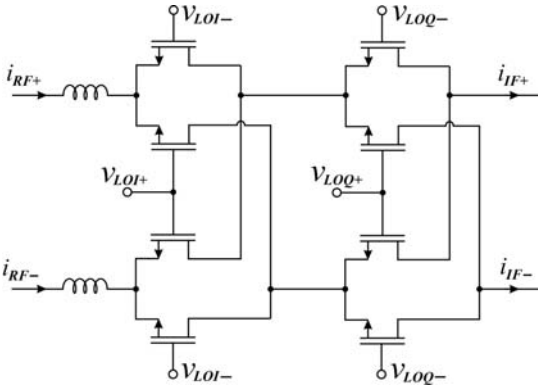


Fig. 3. Schematic of the subharmonic passive mixing core (biasing not shown).

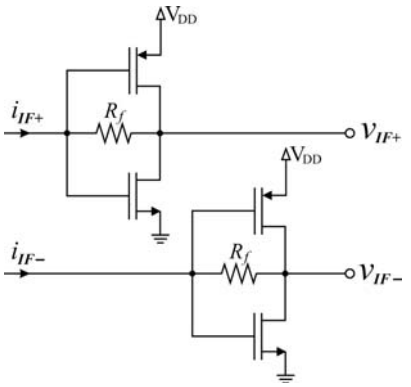


Fig. 4. Schematic of the implemented transimpedance amplifier.

and r_n and r_p are process-dependent parameters, r_{o1} and r_{o2} are the small-signal output resistances of M_1 and M_2, respectively, and the g_{mb} terms model the body effect. The second term in Eq.3 is eliminated when $g_{m2} = 1/R_s$ as described earlier. The equation is further simplified if the input impedance is matched to the source impedance by making $Z_{in,eff} = R_s$, which results in

$$F = 1 + 4\frac{r_n g_{m2} + r_p g_{m5} + R_0^{-1}}{R_s G_{m,eff}^2}. \tag{5}$$

For a detailed derivation of Eqs. 3 and 5 see [12]. While flicker and substrate noise are not included in the above analysis, both of these can also be referred to the output of the transistor and can also be mitigated through the cancellation technique [13].

The subharmonic mixing core is shown in Figure 3. Series inductors are used in the RF path for gain peaking and better bandwidth performance. The mixing core has a pair of cascaded switching networks [3] driven by qudrature LO signals that chop the RF currents twice, thereby producing the subharmonic behavior. Mathematically, if $v_{LO,I}(t) = \cos(\omega_{LO} t)$ and $v_{LO,Q}(t) = \sin(\omega_{LO} t)$, it is simple to see how the RF

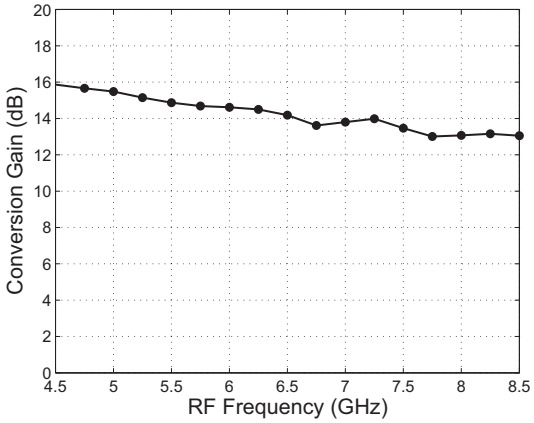


Fig. 5. Measured conversion gain versus RF frequency.

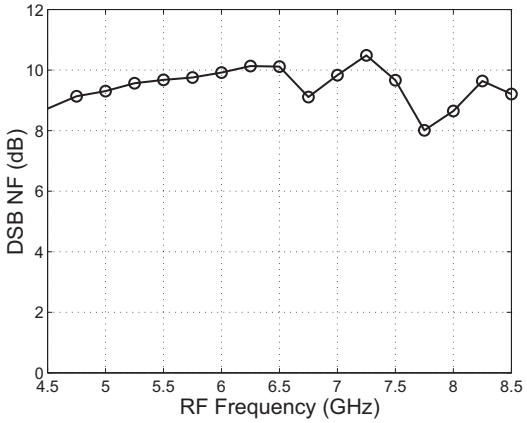


Fig. 6. Measured noise figure versus RF frequency.

signal is downconverted by $2\times\omega_{LO}$:

$$i_{IF}(t) = i_{RF}(t)\cos(\omega_{LO}t)\sin(\omega_{LO}t) \quad (6)$$

$$= \frac{1}{2}i_{RF}(t)\sin(2\omega_{LO}t). \quad (7)$$

The differential quadrature LO signals for the mixer core were produced using a two-step process. First, an off-chip hybrid coupler was used to generate a 0° and a 90° signal and, second, a pair of on-chip active baluns were used to produce the phasors $A_{LO}\angle 0^\circ$, $A_{LO}\angle 180^\circ$, $A_{LO}\angle 90^\circ$ and $A_{LO}\angle 270^\circ$.

The current-driven mixing core is best loaded by a low input impedance transimpedance amplifier to reduce the voltage swing at the source and drain of the switching transistors. In this work, the simple CMOS inverter amplifier with resistive feedback shown in Fig. 4 is used to implement the TIA because it is compact and it consumes low amounts of dc power.

III. Experimental Results

The SHM was fabricated using IBM's 8RF-DM 130 nm CMOS process. The chip has a total area of 1 mm^2 including bond pads and a core circuit area of 0.49 mm^2. A microphotograph of the chip is included in Fig. 1. The mixer draws 43.5 mW of dc power from a 1.5 V supply. Off-chip components (e.g. power splitters, baluns) used for test were first characterized individually and their losses were later de-embedded from the on-wafer test results. The tests were carried out over an RF input frequency range of 4.5 GHz to 8.5 GHz and the LO signal was swept in lock-step with the RF signal from 2.18 GHz to 4.18 GHz to keep the IF frequency constant at 140 MHz.

The conversion gain is plotted in Fig. 5 and starts at a maximum of 16 dB at 4.5 GHz and drops to 13 dB at 8.5 GHz. Meanwhile, the DSB NF ranges from 8 dB to 10.5 dB over the same RF frequency band. A plot of the mixer's NF versus frequency is shown in Fig. 6

An RF input power sweep at a test frequency of 5 GHz shows that the $\mathrm{IP}_{1\mathrm{dB}}$ of the mixer is -10.8 dBm and the $\mathrm{OP}_{1\mathrm{dB}}$ is +6.5 dBm. The third-order intermodulation distortion performance of the SHM was characterized by means of a two-tone test in which the tones were centered at 5 GHz and spaced 1 MHz apart. The two-tone test shows that the mixer has an IIP_3 of -3.7 dBm and an OIP_3 of +13.8 dBm.

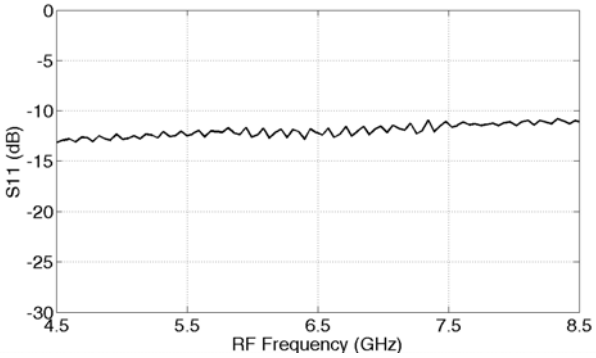


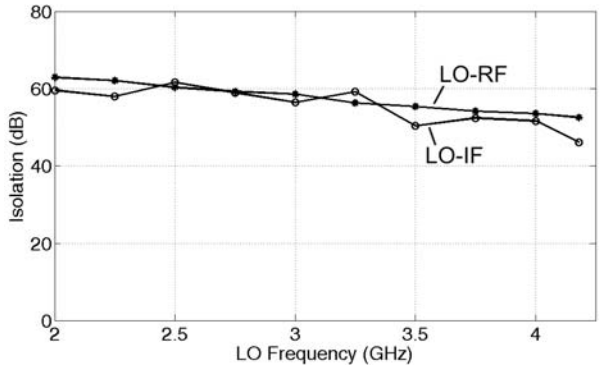
Fig. 7. Measured reflection coefficient at the RF input port.

The measured reflection coefficient at the RF input port is shown in Fig. 7 and is in the range of -11 dB to -13 dB over the band. Lastly, the various port to port isolations were measured and the results are plotted in Fig. 8.

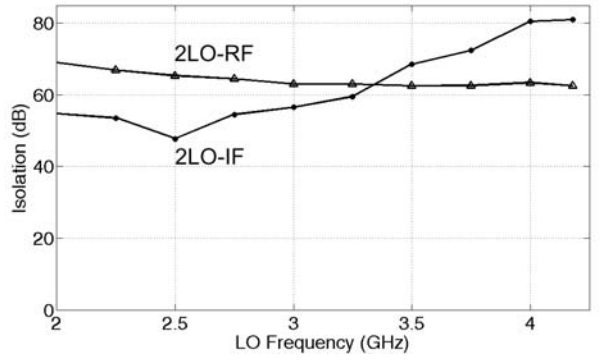
A performance comparison between the proposed chip and other relavant works is shown in Table I.

IV. Conclusion

A broadband low-noise passive subharmonic mixer was proposed in this paper. The noise-cancelling LNTA provides broadband matching along with improved transconductance. The current-driven passive mixing core is loaded by the small input impedance of the transimpedance amplifier, which allows a highly linear performance. Measured results show that the proposed mixer possesses excellent broadband and low-noise performance.



(a)



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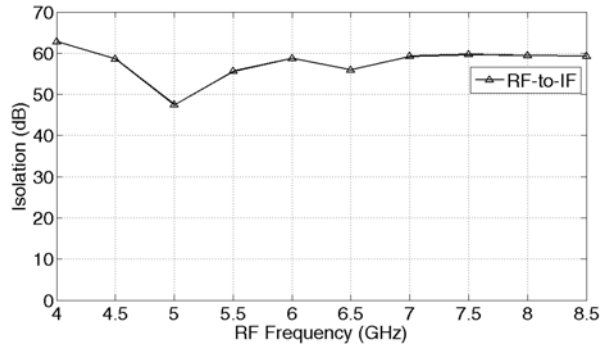

(c)

Fig. 8. Measured isolations: (a) LO-to-(RF,IF) (b) 2LO-to-(RF,IF) and (c) RF-to-IF.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

Parameter	**[4]**	**[3]**	**[14]**	**This Work**
RF freq. (GHz)	24	24	2.2	4.5 to 8.5
conv. gain (dB)	30.5	3.2	4.5	16 (max)
NF_{DSB} (dB)	6.7 (min)	10	11	8 (min)
$S_{11,RF}$(dB)	-15	-15	-30	-10
IP_{1dB} (dBm)	-24	-12.7	-10	$-10.8^{\dagger}$
IIP_3 (dBm)	-13	-	0	$-3.7^{\dagger}$
V_{DD} (V)	1.2	1.6	1.2	1.5
P_{dc} (mW)	78	21.8	13.7	43.5
core area (mm^2)	1.4	0.59	-	0.49
CMOS node (nm)	65	130	130	130

†measured at 5 GHz

ACKNOWLEDGMENT

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